# Aadi Desai

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## Education

**Imperial College London**                                                                                    *Oct 2019 – Jun 2023*

Master of Engineering in Electronics and Computer Engineering | **First Class with Honours**

## Skills

Rust, Go, Git, Cloudflare Workers, TypeScript, Python, C++, PostgreSQL, Docker Compose, Solidity, F#, SystemVerilog

## Projects

**IRC-style Chat Server and Terminal Client** GitHub: supleed2/go-chat                      *Dec 2023 – Jan 2024*

- Built a chat server and client, providing a terminal user interface using the Elm architecture
- Types are imported to client and server code, maintaining a single source-of-truth for communication
- Clients connect to the server using WebSockets, and exchange messages via JSON
- Server maintains recent chat history for multiple rooms, rooms can be created / destroyed on-demand
- Go learning project, including WebSockets, Goroutines and Channels for message passing
- Used mutexes to avoid race-conditions and concurrency bugs when shared data can be written to

**Automated Verification Discord Bot** GitHub: supleed2/nanobot                                  *Jul 2023 – Aug 2023*

- Developed a Discord bot for member onboarding, built on the Poise framework and the Shuttle platform
- Replaces manual checks for Imperial student status, as requests were often missed during busy periods
- Running in production for the last year, allowing members to join quickly and independently
- Leverages Cloudflare Pages + Functions to query the university API without storing sensitive login credentials
- Rust learning project in a real-world environment, with active users providing feedback

**Final Year Project: FPGA Accelerator for StackSynth** GitHub: supleed2/EIE4-FYP           *Oct 2022 – Jun 2023*

- Created a LiteX + SystemVerilog project to generate audio on a custom OrangeCrab FPGA accelerator board
- Intended for use in the 3rd Year Embedded Systems module of the Imperial Electrical Engineering course
- LiteX wrapper module connecting the custom designs and existing IP, e.g. the integrated RISC-V CPU, VexRiscV
- Designed SystemVerilog modules which are instantiated in the LiteX wrapper: a CAN-bus receiver to accept messages from connected StackSynth boards, a 64-channel 48kHz configurable wave sample generator
- Includes C++ demo software for the integrated CPU, to be replaced with student-written coursework code

## Experience

**Digital Design Engineer – Nordic Semiconductor**                                                    *Apr 2022 – Sep 2022*

- Developed open-source tooling for syntax highlighting and configurable style / syntax linting of SystemVerilog
- Updated SystemVerilog simulation designs to use only synthesizable constructs, for Verilator compatibility
- Gathered feedback from colleagues for improvements to the editor tooling, such as linting rules to add

**VEX EDR International Robotics Competition**                                                         *Sep 2017 – May 2018*

- Designed and built components for our school team's robot, compensating for unreliable parts such as DC motors and encoders, using Proportional-Integral-Derivative feedback loop controllers
- Won awards in regional competition rounds securing a finalist position during the UK national event, for the international event held in Kentucky USA, where we represented the UK
- Robots from opposing teams compete in the assigned game both autonomously and controlled by a driver

**Store Volunteer – St Luke's Hospice**                                                                 *Nov 2014 – Apr 2018*

- Managed a local charity store, including sales floor, initially as part of the Duke of Edinburgh (DofE) Award
- Trained and lead new volunteers, continuing after DofE ended as the experience was rewarding