EC600U Series QuecOpen Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-09-26	Manli CHEN/ Frank WANG/ Ailsa WANG	Creation of the document
1.0	2021-12-20	Manli CHEN/ Frank WANG/ Ailsa WANG	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the EC600U series QuecOpen® module and its air interface and hardware interfaces which are connected with your applications.

This document helps you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up wireless applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such a model is currently unavailable.
[…]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] means all four SDIO_DATA pins SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

EC600U series QuecOpen is an LTE Cat 1 module, which supports LTE-FDD, LTE-TDD, and GSM/GPRS network data connection. It provides voice functionality to meet your specific application demands as well as Bluetooth and Wi-Fi Scan [1] functions. EC600U series QuecOpen includes two models: EC600U-CN QuecOpen and EC600U-EU QuecOpen, from which you can choose according to the region or the operator. The following table shows the frequency bands of the module.

Table 2: Frequency Bands

Mode	Frequency Bands of EC600U-CN QuecOpen	Frequency Bands of EC600U-EU QuecOpen
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41
GSM	-	850/900/1800/1900 MHz
Bluetooth and Wi-Fi Scan [1]	2.4 GHz	2.4 GHz

With a compact profile of 22.9 mm × 23.9 mm × 2.4 mm, the module can meet almost all requirements for M2M applications such as automation, metering, tracking systems, security systems, routers, wireless POS terminals, mobile computing devices, PDA phones, and tablet PCs.

EC600U series QuecOpen is a SMD type module which can be embedded into applications through its 148 pins, including 76 LCC pins and 72 LGA pins.

[1] EC600U series QuecOpen module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional (both supported or not), please contact Quectel Technical Supports for details.

2.2. Key Features

The following table describes the detailed features of the module.

Table 3: Key Features

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	**EC600U-EU QuecOpen:** ● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 **EC600U series QuecOpen:** ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	● Supports up to non-CA Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Max. transmission data rates: LTE-FDD: 10 Mbps (DL) /5 Mbps (UL) LTE-TDD: 8.96 Mbps (DL) /3.1 Mbps (UL)
GSM Features (Only for EC600U-EU QuecOpen)	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS-1/CS-2/CS-3/CS-4 ● Max. transmission data rates: 85.6 kbps (DL) /85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS protocols ● Supports PAP and CHAP protocols, which are usually used for PPP connection
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
(U)SIM Interfaces	● Supports USIM/SIM card: 1.8/3.0 V
Audio Features	● Supports two analog audios input and three analog audios output channels ● GSM: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Supports one digital audio interface

USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, and firmware upgrade ● Supports USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.14, Android 4.x–11.x, etc.
UART Interfaces	● **Main UART:** Used for AT command communication and data transmission Baud rates: up to 921600 bps, 115200 bps by default Supports RTS and CTS hardware flow control ● **Debug UART:** Used for log output Baud rate: 921600 bps Cannot be used as a general-purpose serial port ● **UART2 and UART3:** Baud rates: up to 921600 bps, 115200 bps by default Supports RTS and CTS hardware flow control
I2C Interface	● Supports one I2C interface
SPI Interface	● Supports only master mode
Camera Interface	● Provides one camera interface supporting cameras up to 0.3 MP; I/O pins only support 1.8 V ● Supports the two-data-line transmission of SPI
External Flash Interface	● Supports external flash chip and file system
LCM Interface	● Supports LCM interface in SPI mode
Matrix Keypad Interface	● Supports 5 × 6 matrix keypad
ADC Interface	● Supports four ADC interfaces
SDIO Interface*	● Supports one SDIO 1.1 interface and can be used for external WLAN chip
SD Card Interface	● Supports one interface compliant with SD 2.0 specification and can be used for external SD card
USB_BOOT Interface	● Supports one download control interface
AT Commands	● Compliant with *3GPP TS 27.007*, *27.005* and Quectel enhanced AT commands
Network Indication	● Two pins NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interface	● Main antenna interface (ANT_MAIN) ● Bluetooth/Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● 50 Ω impedance

Position Fixing	● Supports Wi-Fi Scan
Physical Characteristics	● Size: (22.9 ±0.15) mm × (23.9 ±0.15) mm × (2.4 ±0.2) mm ● Weight: approx. 2.6 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [2] ● Extended temperature range: -40 °C to +85 °C [3] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● Via USB interface or FOTA
RoHS	● All hardware components are fully compliant with *EU RoHS Directive*

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[2] Within the operating temperature range, the module meets 3GPP specifications.
[3] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

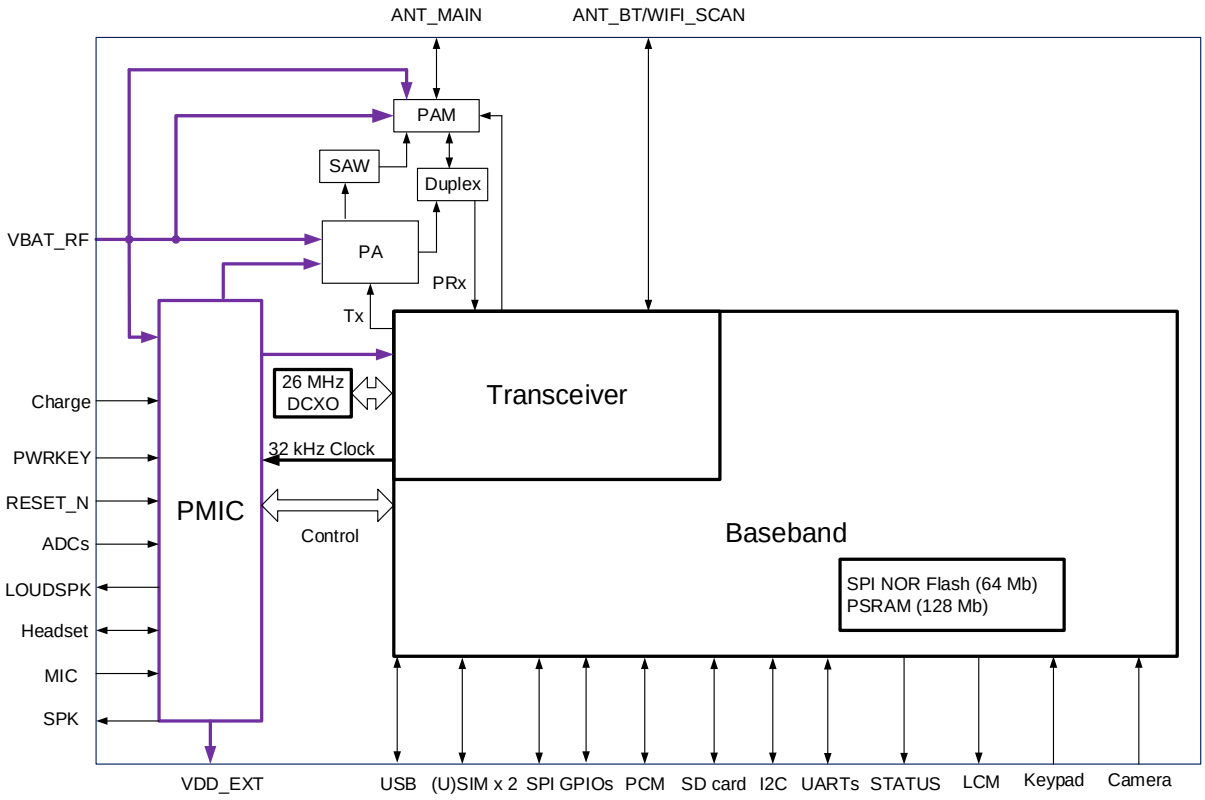


Figure 1: Functional Diagram

2.4. EVB

To help you develop applications with the module, Quectel provides an evaluation board (LTE OPEN EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The module is equipped with 76 LCC pins and 72 LGA pins that can be connected to cellular application platform. The following interfaces are described in detail in subsequent chapters.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI interface
- PCM and I2C interfaces
- External flash interface
- Analog audio interfaces
- LCM interface
- Matrix keypad interface
- Charging control interface*
- SD card interface
- SDIO interface*
- ADC interfaces
- PSM interface*
- Status indication
- USB_BOOT interface
- Camera interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

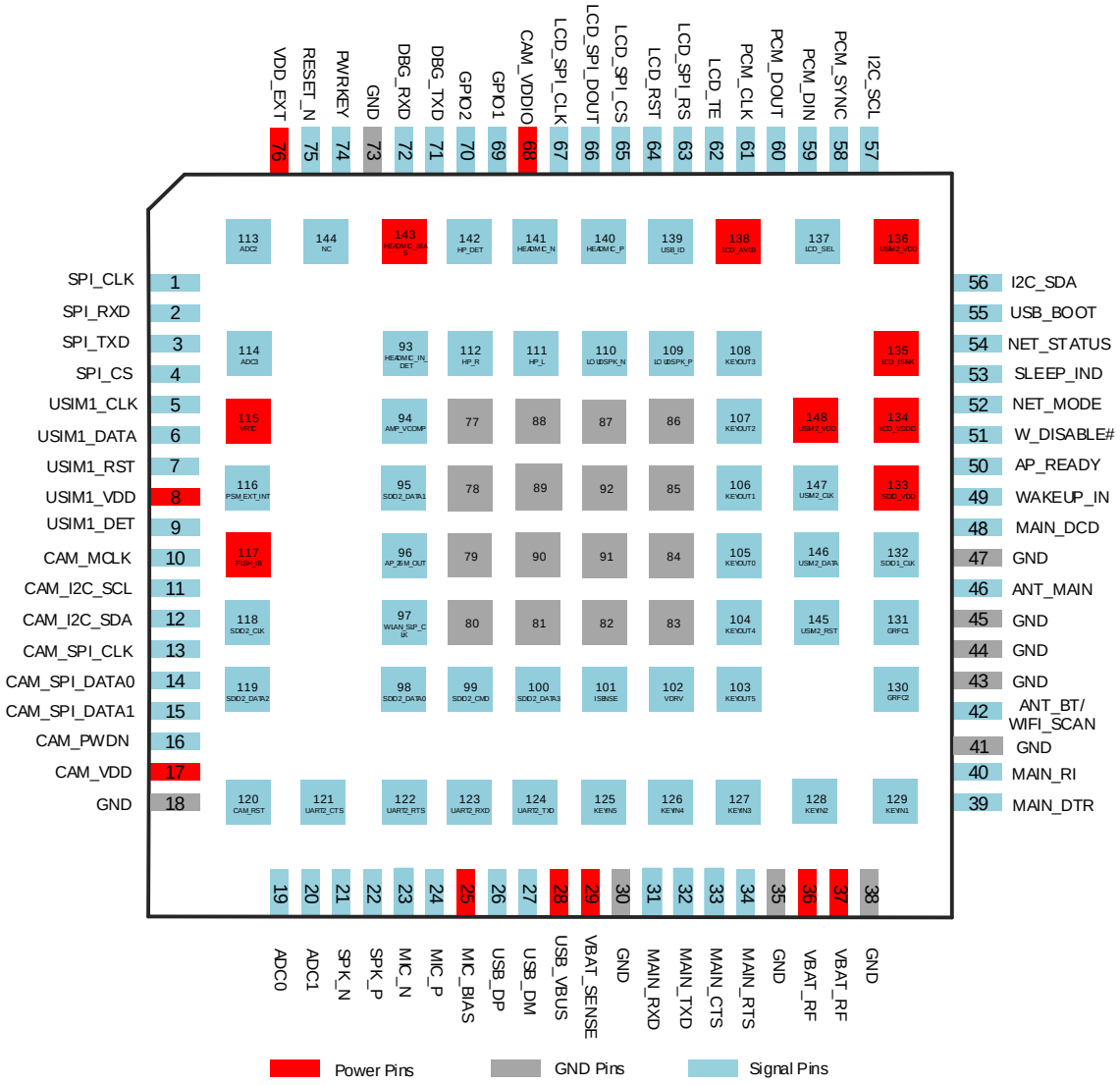


Figure 2: Pin Assignment (Top View)

NOTE

1. Pins USB_BOOT and KEYIN1 cannot be pulled up before startup.
2. Keep the NC pin unconnected; all GND pins should be connected to ground.
3. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2 interface are used, pins 51–53 must be kept unconnected; if the pins 51–53 are used, that is, the (U)SIM2 interface is not used, the pins 145–147 must be kept unconnected.

4. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Supports for more information about how to use (U)SIM2.
5. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.3. Pin Description

The following tables show the pin definition and description of the module.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_RF	36, 37	PI	Power supply for module's baseband	Vmax = 4.3 V Vmin = 3.3 V	It must be provided with sufficient

			part and RF part	Vnom = 3.8 V	current of 2.3 A at least.
VBAT_SENSE	29	AI	Acts as the pin for battery voltage and charging current detection when charging function is used; otherwise acts as power supply pin for the module.		Whether or not the charging function is used, this pin must be connected to the VBAT power supply, otherwise the module will not be powered on normally.
GND	18, 30, 35, 38, 41, 43–45, 47, 73, 77–92				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	76	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Used with a 2.2 μF bypass capacitor. If unused, keep it open.
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	75	DI	Resets the module	V_{IL}max = 0.5 V	VBAT power domain. If unused, keep it open. Active low.
PWRKEY	74	DI	Turns on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
Network Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	52	DO	Indicates whether the module has registered on LTE network	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NET_STATUS	54	DO	Indicates the module's network	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	

			activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	26	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. If unused, keep them open.
USB_DM	27	AIO	USB differential data (-)		
USB_ID*	139	DI	Reserved		Internally pulled up to 1.8 V by default. Keep it open.
USB_VBUS	28	AI	USB connection detection	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	9	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM1_VDD	8	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported and can be identified by the module automatically.
USIM1_DATA	6	DIO	(U)SIM1 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V	

				V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	5	DO	(U)SIM1 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	7	DO	(U)SIM1 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_VDD	136, 148	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported and can be identified by the module automatically. It is recommended to use pin 148 as the power supply and keep pin 136 unconnected.
USIM2_DATA	146	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	147	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V	

				V_{OH}min = 2.55 V	
USIM2_RST	145	DO	(U)SIM2 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	40	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
MAIN_DCD	48	DO	Main UART data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_CTS	33	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_RTS	34	DI	DTE request to send signal to DCE (connect to DTE's RTS)	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DTR	39	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_TXD	32	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_RXD	31	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	72	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.

DBG_TXD	71	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_RXD	123	DI	UART2 receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
UART2_TXD	124	DO	UART2 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART2_CTS	121	DO	DTE UART2 clear to send (connect to DTE's CTS)	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART2_RTS	122	DI	DTE UART2 request to send (connect to DTE's RTS)	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC3	114	AI	General-purpose ADC interfaces	Voltage range: 0 V to VBAT	A 1 kΩ resistor must be connected in series when in use. If unused, keep them open.
ADC2	113	AI			
ADC1	20	AI			
ADC0	19	AI			
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LOUDSPK_P	109	AO	Loudspeaker differential output (+)		If unused, keep them open.
LOUDSPK_N	110	AO	Loudspeaker differential output (-)		
AMP_VCOMP	94		Headset dedicated ground. It should be traced between the left and right channels, and		

			connected to the GND of the headset jack, and then a via directly to the main GND layer.		
HP_L	111	AO	Headset left channel output		
HP_R	112	AO	Headset right channel output		
HEADMIC_P	140	AI	Headset analog input (+)		
HEADMIC_N	141	AI	Headset analog input (-)		
HEADMIC_BIAS	143	PO	Bias voltage output for headset	Vo = 2.2–3.0 V Vnom = 2.6 V	
HP_DET	142	DI	Headset plug detection		
HEADMIC_IN_DET	93	DI	Headset audio input and headset audio input plug detection		
SPK_P	22	AO	Analog audio differential output (+)		Used for receiver interface. If unused, keep them open.
SPK_N	21	AO	Analog audio differential output (-)		
MIC_BIAS	25	PO	Bias voltage output for microphone	Vo = 2.2–3.0 V Vnom = 2.2 V	
MIC_P	24	AI	Microphone analog input (+)		
MIC_N	23	AI	Microphone analog input (-)		
I2C and PCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	57	OD	I2C serial clock		Pull each of them up to 1.8 V power with an external resistor. If unused, keep them open.
I2C_SDA	56	OD	I2C serial data		
PCM_DIN	59	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain.

				V_{IH}min = 1.26 V V_{IH}max = 2.0 V	If unused, keep them open.
PCM_DOUT	60	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Only supports slave mode.
PCM_SYNC	58	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
PCM_CLK	61	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	4	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open. Only supports master mode.
SPI_TXD	3	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_RXD	2	DI	SPI master mode input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_CLK	1	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_TE	62	DI	LCD tearing effect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
LCD_RST	64	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SEL	137	DO	Reserved	$_{OL}$max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_CS	65	DO	LCD chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_CLK	67	DO	LCD clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

LCD_SPI_RS	63	DO	LCD register select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_DOUT	66	DIO	LCD data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_ISINK	135	PI	Sink current input. Backlight adjustment.	Imax = 200 mA Current is configurable.	It is driven by the current sink method and connected to the backlight cathode; the brightness can be adjusted with current control. If unused, keep it open.
LCD_VDDIO	134	PO	LCD digital power	Vnom = 1.8 V	LCD power supply. If unused, keep them open.
LCD_AVDD	138	PO	LCD analog power	Vnom = 3.0 V	
Matrix Keypad Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
KEYIN1	129	DI	Matrix keypad input 1		1.8 V power domain. If unused, keep them open.
KEYIN2	128	DI	Matrix keypad input 2		
KEYIN3	127	DI	Matrix keypad input 3		
KEYIN4	126	DI	Matrix keypad input 4		
KEYIN5	125	DI	Matrix keypad input 5		
KEYOUT0	105	DO	Matrix keypad output 0		
KEYOUT1	106	DO	Matrix keypad output 1		
KEYOUT2	107	DO	Matrix keypad output 2		
KEYOUT3	108	DO	Matrix keypad output 3		

KEYOUT4	104	DO	Matrix keypad output 4		
KEYOUT5	103	DO	Matrix keypad output 5		
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_BT/ WIFI_SCAN	42	AIO	The shared interface for Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω impedance. If unused, keep it open.
ANT_MAIN	46	AIO	Main antenna		50 Ω impedance.
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	55	DI	Control pin for the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved.
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	10	DO	Master clock of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CAM_I2C_SCL	11	OD	I2C clock of camera		Pull each of them up to 1.8 V power domain with an external resistor.
CAM_I2C_SDA	12	OD	I2C data of camera		

					If unused, keep them open.
CAM_SPI_CLK	13	DI	SPI clock of camera	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	14	DI	SPI data0 of camera	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
CAM_SPI_DATA1	15	DI	SPI data1 of camera		
CAM_PWDN	16	DO	Power down of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CAM_RST	120	DO	Reset of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CAM_VDD	17	PO	Analog power supply of camera	Vnom = 2.8 V	Power supply of camera. If unused, keep them open.
CAM_VDDIO	68	PO	Digital power supply of camera	Vnom = 1.8 V	

Flash Light Driver Interface*

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
FLSH_IB	117	PI	Current sink input	Imax = 240 mA Current is configurable.	Connected to the cathode of a light emitting diode when in use. If unused, keep it open.

RF Control Interface*

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC2	130	DO	Generic RF Control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
GRFC1	131	DO	Generic RF Control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

GPIO Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO1	69	DIO	General-Purpose Input/Output		1.8 V power domain. If unused, keep
GPIO2	70	DIO	General-Purpose		

			Input/Output		them open.

Charging Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ISENSE	101	AI	Charging current detection		If unused, keep it open.
VBAT_SENSE	29	AI	Battery voltage and charging current (combines with ISENSE) detection		Whether or not the charging function is used, the pin must be connected to the VBAT power supply, otherwise the module will not be powered on normally.
VDRV	102	AO	Charging control pin. Used for driving the MOS tube in the external charging circuit to adjust the charging current.		If unused, keep it open.

SDIO Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO2_CLK	118	DO	SDIO2 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
SDIO2_CMD	99	DO	SDIO2 command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO2_DATA0	98	DIO	SDIO2 data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SDIO2_DATA1	95	DIO	SDIO2 data bit 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	

SDIO2_DATA2	119	DIO	SDIO2 data bit 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SDIO2_DATA3	100	DIO	SDIO2 data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	49	DI	Wakes up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
AP_READY	50	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SLEEP_IND	53	DO	Indicates the module's sleep mode	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	51	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
AP_26M_OUT*	96	DO	Reserved. 26 MHz clock output.		If unused, keep it open.
VRTC*	115	PI	Power supply for RTC	Vnom = 3 V V_O = 2.8–3.2 V	If unused, keep it open.
WLAN_SLP_CLK*	97	DO	WLAN sleep clock		If unused, keep it open.
PSM_EXT_INT*	116	DI	External interrupt	VRTC power	Active high.

			pin. Wakes up the module from PSM when being pulled high externally.	domain	If unused, keep it open.
SDIO1_CLK	132	DO	SD card clock		If unused, keep it open.
SDIO_VDD	133	PO	SD card IO power		If unused, keep it open.
NC Pin					
Pin Name	**Pin No.**				**Comment**
NC	144				Keep it open.

NOTE

1. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2 interface are used, pins 51–53 must be kept unconnected; if the pins 51–53 are used, that is, the (U)SIM2 interface is not used, the pins 145–147 must be kept unconnected.
2. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Supports for more information about how to use (U)SIM2.
3. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.4. Specific Multiplex Interface Function Description

Table 6: Multiplex Interface Function Description

External Flash Interface					
Pin Name	**Pin No.**	**I/O**	**Multiplex Function**	**DC Characteristics**	**Description**
PCM_SYNC	58	DO	SPI_FLASH1_CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	External NOR flash chip select
PCM_CLK	61	DO	SPI_FLASH1_CLK		External NOR flash clock

PCM_DIN	59	DIO	SPI_FLASH1_SIO_0	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	External NOR flash data bit 0
PCM_DOUT	60	DIO	SPI_FLASH1_SIO_1		External NOR flash data bit 1
GPIO1	69	DIO	SPI_FLASH1_SIO_2		External NOR flash data bit 2
GPIO2	70	DIO	SPI_FLASH1_SIO_3		External NOR flash data bit 3
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Multiplex Function**	**DC Characteristics**	**Description**
SDIO_VDD	133	PO	-		SD card IO power
SDIO1_CLK	132	DO	-		SD card clock
MAIN_DCD	48	DO	SDIO1_CMD		SD card command
MAIN_DTR	39	DIO	SDIO1_DATA0		SDIO1 data bit 0
MAIN_RI	40	DIO	SDIO1_DATA1		SDIO1 data bit 1
WAKEUP_IN	49	DIO	SDIO1_DATA2		SDIO1 data bit 2
AP_READY	50	DIO	SDIO1_DATA3		SDIO1 data bit 3
I2C_SDA	56	DI	SD_DET		SD card hot-plug detect

NOTE

1. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.
2. See ***document [2]*** for details about pin multiplexing of the module.

3.5. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Modes	Details	
Normal Operation	Idle	Software is active. The module remains registered on the network, and is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode where the RF function is invalid.	
Sleep Mode	In this mode, the current consumption of the module is reduced to a low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from the network normally.	
Power down Mode	In this mode, the module's power supply is cut off by its power management unit (PMU). The software is inactive and the serial interfaces are inaccessible, while the VBAT_RF pins are still powered.	

3.6. Power Saving

3.6.1. Sleep Mode

The module is able to reduce its current consumption to an ultra-low value in the sleep mode. The following chapters describe power saving procedures of the module.

3.6.1.1. UART Application Scenario

If the host communicates with the module via UART interface, the following preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

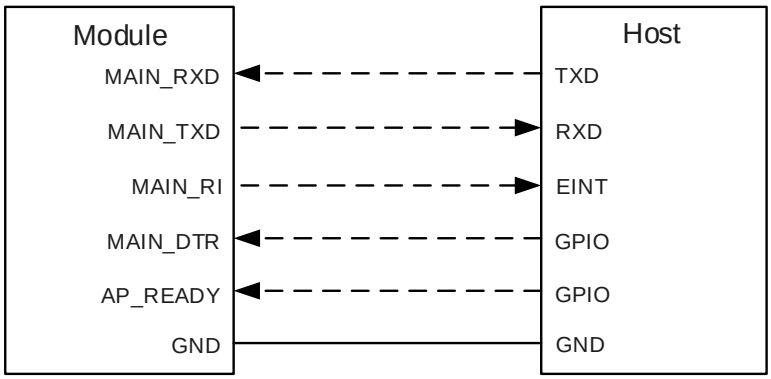


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.24*** for details about MAIN_RI behaviors.

3.6.1.2. USB Application with USB Remote Wakeup Function*

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

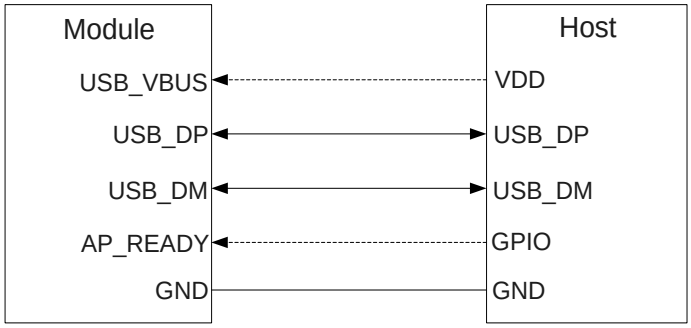


Figure 4: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module sends remote wake-up signals to wake up the

host via the USB bus.

NOTE

USB suspend is supported on the Linux system but not on the Windows system.

3.6.1.3. USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function*

If the host supports USB suspend/resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

In this case, three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

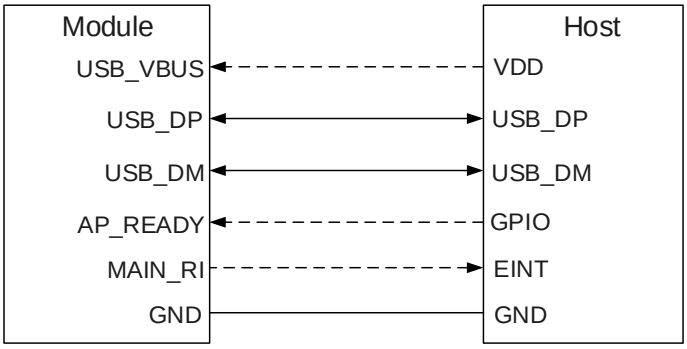


Figure 5: Sleep Mode Application with MAIN_RI

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin. See ***Chapter 3.24*** for details about MAIN_RI behaviors.

NOTE

USB suspend is supported on the Linux system but not on the Windows system.

3.6.1.4. USB Application without USB Suspend Function*

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter into sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

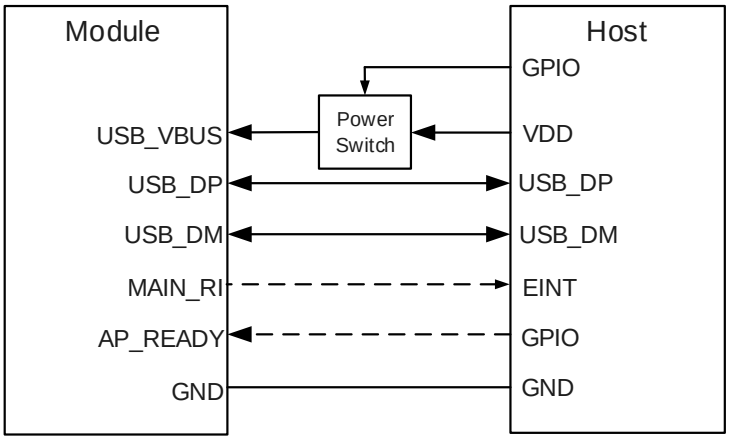


Figure 6: Sleep Mode Application without Suspend Function

You can wake up the module by switching on the power switch to supply power to USB_VBUS.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host.
2. When using MAIN_DTR and MAIN_RI (pins 39 and 40), please note that the two pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.6.2. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. You can set this mode via the following ways.

Hardware:

The pin W_DISABLE# is pulled up by default. Its control function for airplane mode, which is disabled by default in software, can be enabled through **AT+QCFG="airplanecontrol",1**. When such a control function is enabled, you can drive it to low level to make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides the choice of functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** RF function is disabled (airplane mode).

3.7. Power Supply

3.7.1. Power Supply Pins

The power supply pins are used to connect an external power, supplying power to the RF and baseband circuits of the module.

Table 8: Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	36, 37	Power supply for the module's baseband part and RF part	3.3	3.8	4.3	V
VBAT_SENSE	29	Acts as the pin for battery voltage and charging current detection when charging function is used; otherwise acts as power supply pin for the module	3.3	3.8	4.3	V
GND	18, 30, 35, 38, 41, 43–45, 47, 73, 77–92					

NOTE

Whether or not the charging function is used, VBAT_SENSE must be connected to the VBAT power supply, otherwise the module will not be powered on normally.

3.7.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure the input voltage never drops below 3.3 V. The following figure shows the voltage drop during burst transmission.

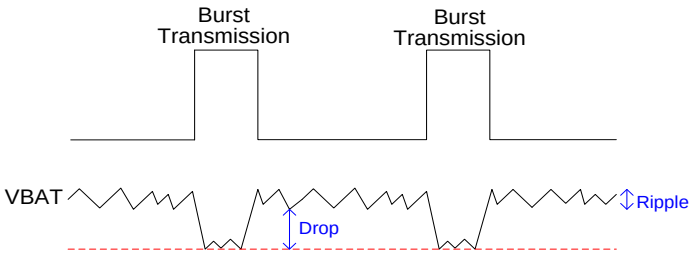


Figure 7: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use bypass capacitors of about 100 µF with low ESR (ESR = 0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_SENSE and VBAT_RF pins. When the external power supply is connected to the module, VBAT_SENSE and VBAT_RF need to be routed in star structure. The width of the VBAT_RF trace should not be less than 2.5 mm. When used as a power supply pin (that is, charging function is not used), the width of the VBAT_SENSE trace should not be less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to avoid the surge, use a TVS diode of which reverse working voltage is 4.7 V and peak pulse power is up to 2550 W. The following figure shows the reference circuit with and without charging function.

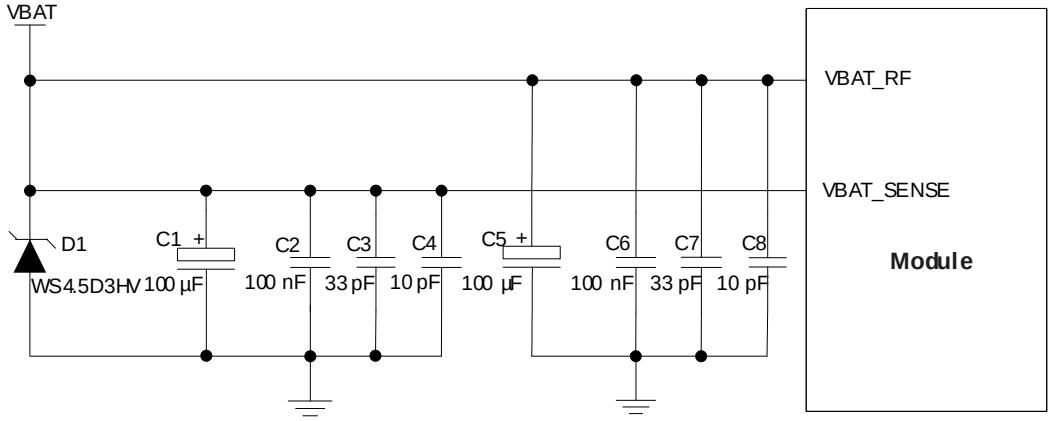


Figure 8: Power Supply (without Charging Function)

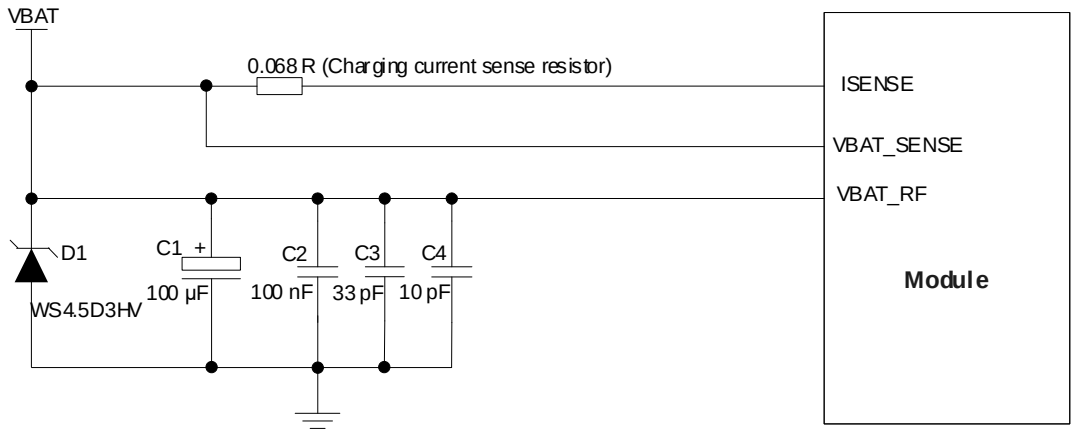


Figure 9: Power Supply (with Charging Function)

3.7.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current of 2.0 A at least for EC600U-CN QuecOpen and 3.0 A at least for EC600U-EU QuecOpen. If the voltage drop between the input and output is not too high, use an LDO to supply power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), use a buck converter as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

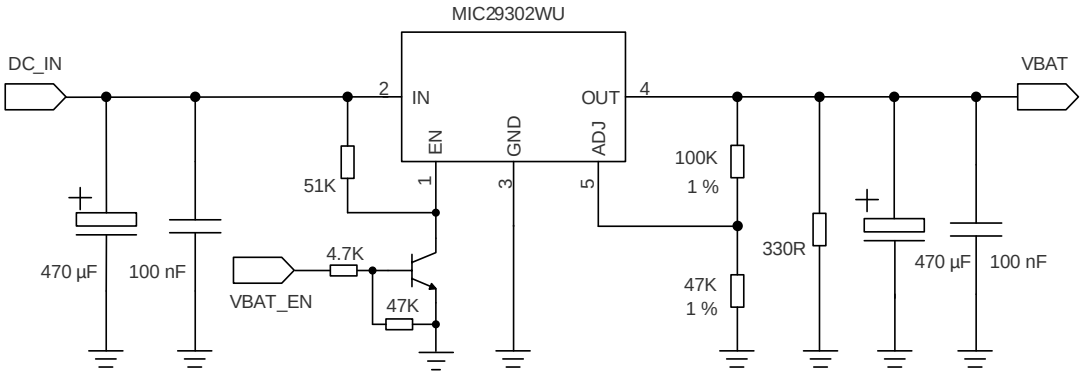


Figure 10: Reference Circuit of Power Supply

3.8. Turn on/Turn off/Reset

3.8.1. Turn on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	74	DI	Turns on/off the module	VBAT power domain

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

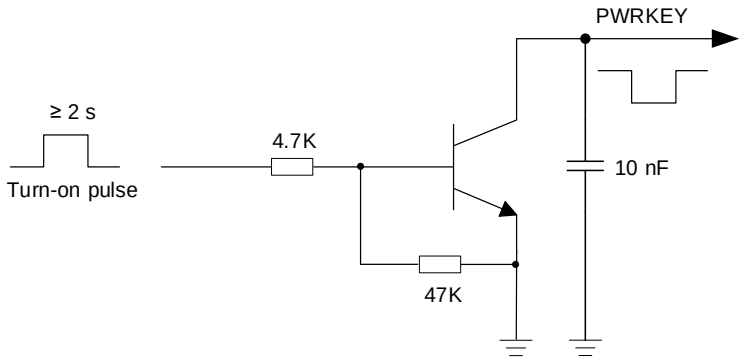


Figure 11: Turning on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the key, electrostatic strike may be generated from finger. Therefore, you must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

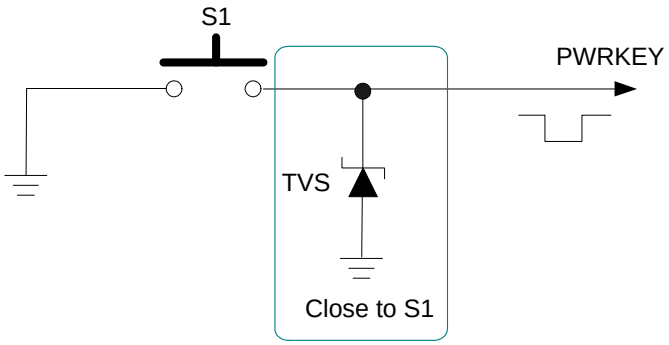


Figure 12: Turning on the Module Using Button

The power-up scenario is illustrated in the following figure.

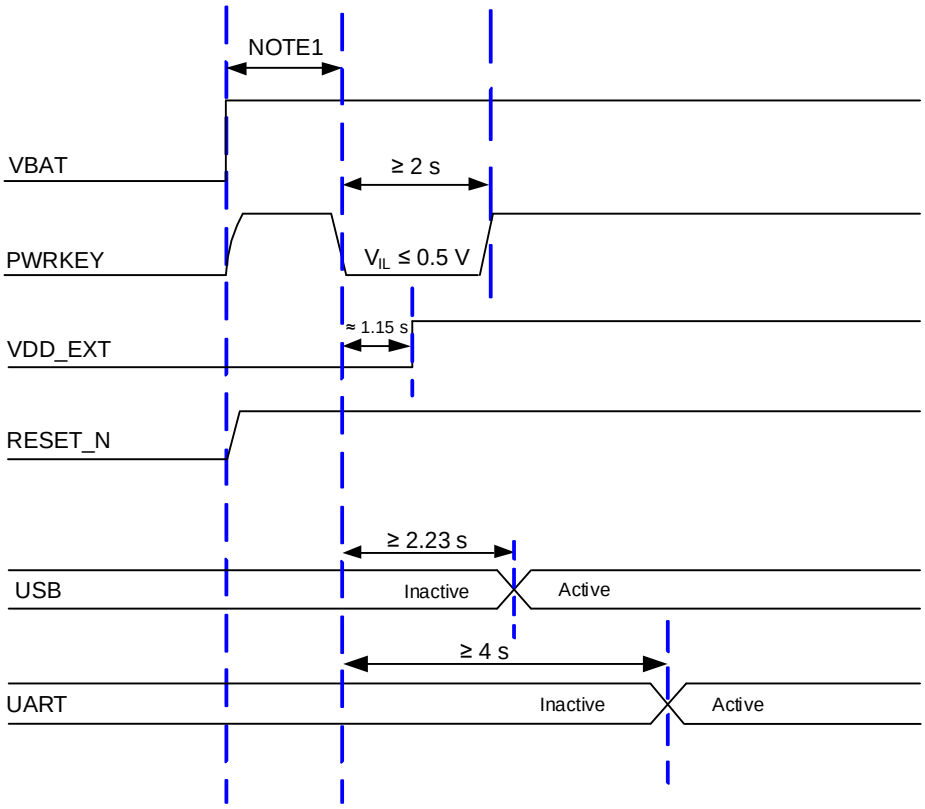


Figure 13: Power-up Timing

NOTE

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can have direct vias to GND with a recommended 1 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

3.8.2. Turn off

The following procedures can be used to turn off the module.

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

3.8.2.1. Turn off with PWRKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY. After this, the module executes power-down procedure. The power-down scenario is illustrated in the following figure.

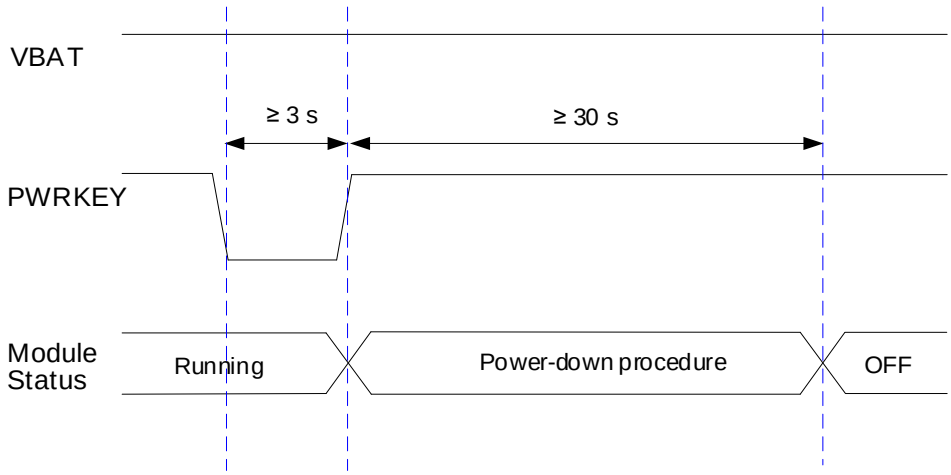


Figure 14: Power-down Timing

3.8.2.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

See ***document [3]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When the PWRKEY pin has been kept pulled down directly to GND, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and power up the module again. Therefore, we recommend that you can use a control circuit to drive the PWEKEY high/low to turn on/off the module instead of keeping the PWRKEY connected to GND.
3. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.8.3. Reset

The RESET_N pin can be used to reset the module. You can reset the module by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	75	DI	Resets the module	VBAT power domain. Active low.

The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or button to control the RESET_N.

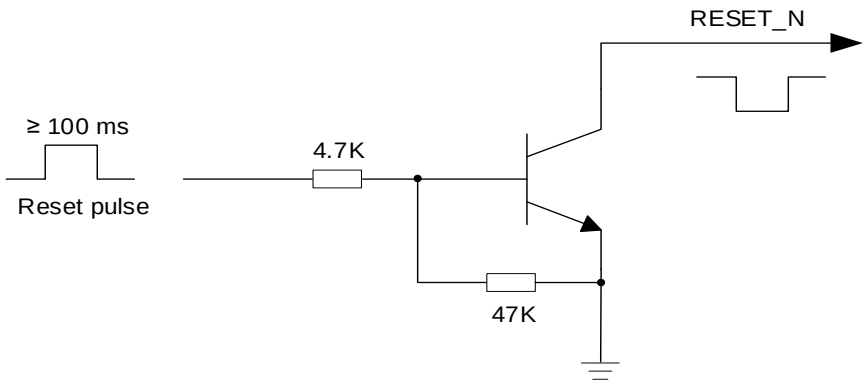


Figure 15: Reference Circuit of RESET_N by Using Driving Circuit

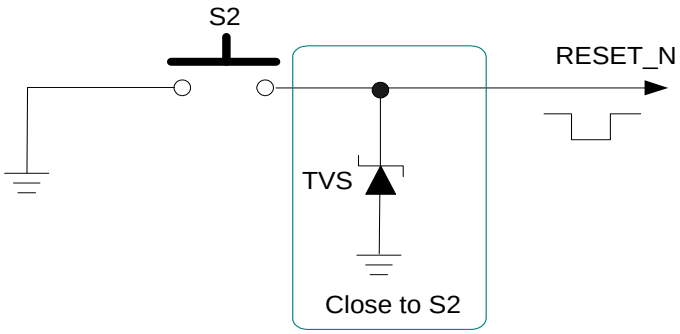


Figure 16: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

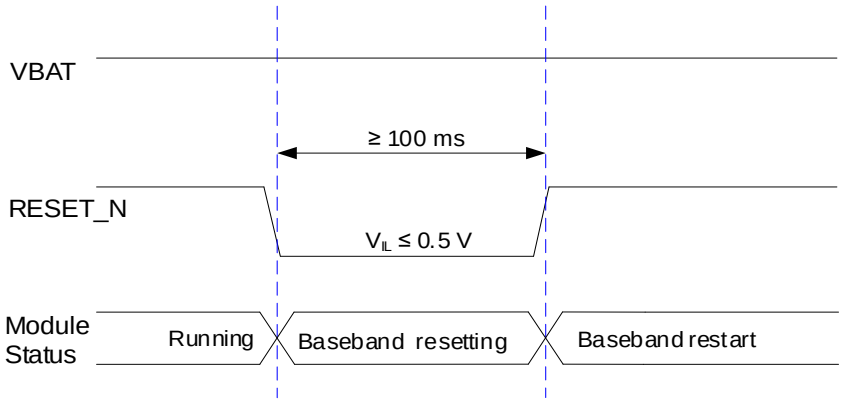


Figure 17: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin.

3.9. (U)SIM Interfaces

The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Either1.8 V or 3.0 V (U)SIM card is supported.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	9	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_VDD	8	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	6	DIO	(U)SIM1 card data	
USIM1_CLK	5	DO	(U)SIM1 card clock	
USIM1_RST	7	DO	(U)SIM1 card reset	

USIM2_VDD	136, 148	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. It is recommended to use pin 148 as power supply and keep pin 136 unconnected.
USIM2_DATA	146	DIO	(U)SIM2 card data	
USIM2_CLK	147	DO	(U)SIM2 card clock	
USIM2_RST	145	DO	(U)SIM2 card reset	

The module supports the card hot-plug detection of (U)SIM1 interface via the USIM1_DET pin and both high- and low-level detections are supported. By default, the function is disabled, and see **AT+QSIMDET** in ***document [3]*** for more details. The (U)SIM2 interface does not support the card hot-plug detection function.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

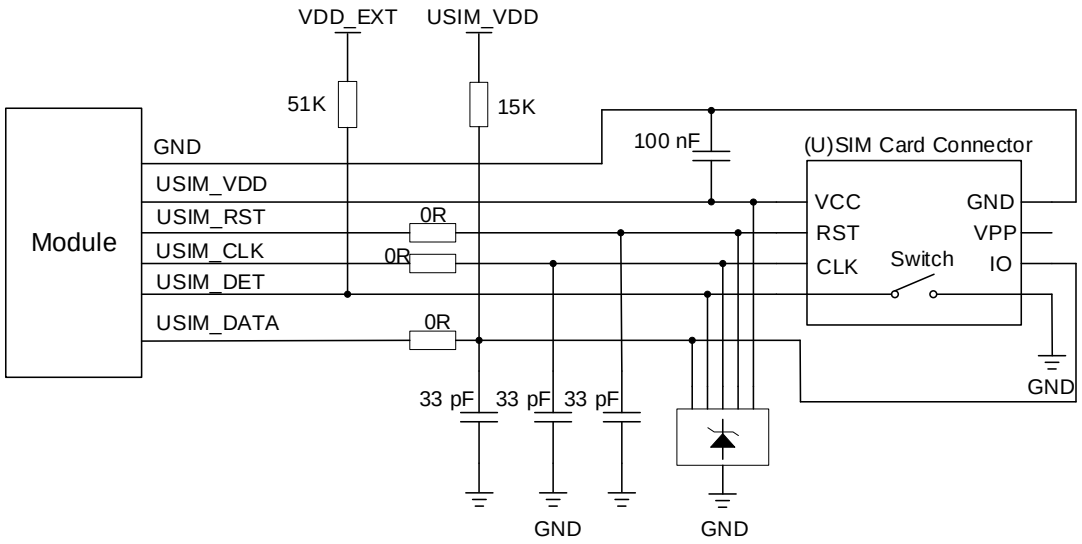


Figure 18: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the (U)SIM card detection function is not needed, keep USIM1_DET disconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

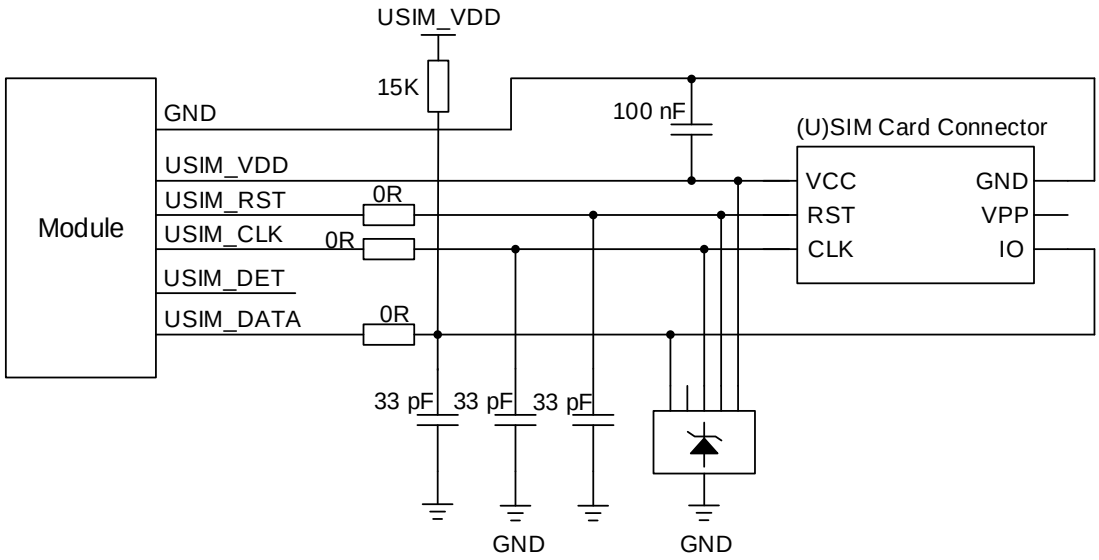


Figure 19: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure that the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

NOTE

1. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2 interface are used, pins 51–53 must be kept unconnected. If the pins 51–53 are used, that is, the (U)SIM2 interface is not used, the pins 145–147 must be kept unconnected.
2. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for

using dual (U)SIM operation. Please consult Quectel Technical Supports for more information about how to use (U)SIM2.

3.10. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve in the slave mode. It is used for AT command communication, data transmission, software debugging, and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	26	AIO	USB differential data (+)	Requires differential impedance of 90 Ω.
USB_DM	27	AIO	USB differential data (-)	
USB_VBUS	28	AI	USB connection detection	Typ. 5.0 V Min. 3.5 V
USB_ID*	139	DI	Reserved	Internally pulled up to 1.8 V by default. If unused, keep it open.

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

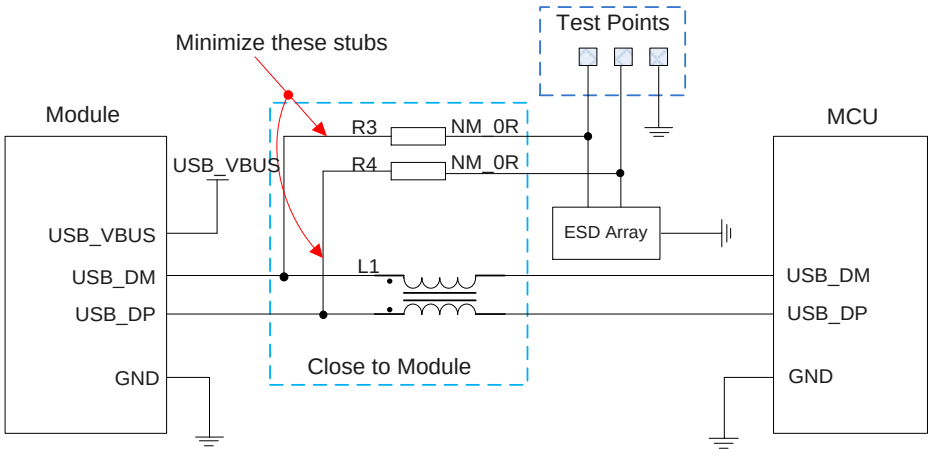


Figure 20: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R3, and R4 must be placed close to the module, and resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential trace is 90 Ω.
- To preserve signal quality, do not route signal traces under or near crystals, oscillators, magnetic devices and RF signal traces.
- Pay attention to the selection of the ESD component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

3.11. UART Interfaces

The module provides four UART interfaces: main UART, debug UART, UART2 and UART3. UART3 is multiplexed from other pins and see ***document [2]*** for specific pin numbers. Features of the four UART interfaces are described below.

- Main UART interface supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default setting is 115200 bps. This interface is used for data transmission and AT command communication. It supports RTS and CTS hardware flow control.
- Debug UART interface supports 921600 bps baud rate. It is used for log output.
- UART2 and UART3 interfaces support the same baud rates as the Main UART interface. They both support RTS and CTS hardware flow control.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	40	DO	Main UART ring indication	1.8 V power domain. If unused, keep them open.
MAIN_DCD	48	DO	Main UART data carrier detection	
MAIN_CTS	33	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	

MAIN_RTS	34	DI	DTE request to send signal to DCE (connect to DTE's RTS)
MAIN_DTR	39	DI	Main UART data terminal ready
MAIN_TXD	32	DO	Main UART transmit
MAIN_RXD	31	DI	Main UART receive

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	72	DI	Debug UART receive	1.8 V power domain. If unused, keep them open.
DBG_TXD	71	DO	Debug UART transmit	

Table 15: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Description	Comment
UART2_RXD	123	DI	UART2 receive	1.8 V power domain. If unused, keep them open.
UART2_TXD	124	DO	UART2 transmit	
UART2_CTS	121	DO	DTE UART2 clear to send (connect to DTE's CTS)	
UART2_RTS	122	DI	DTE UART2 request to send (connect to DTE's RTS)	

The module provides 1.8 V UART interfaces. Use a level shifter if the application is equipped with a 3.3 V UART interface. A level shifter TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

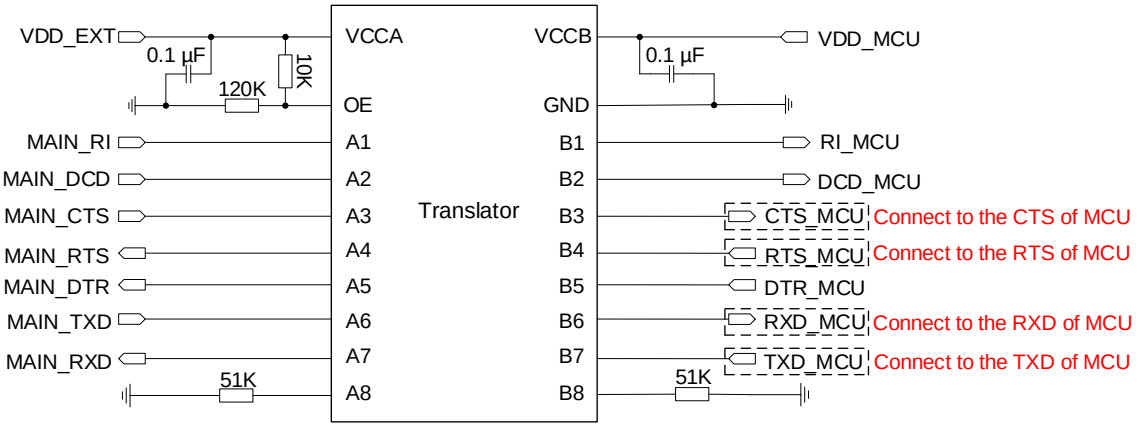


Figure 21: Reference Circuit with Translator Chip

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

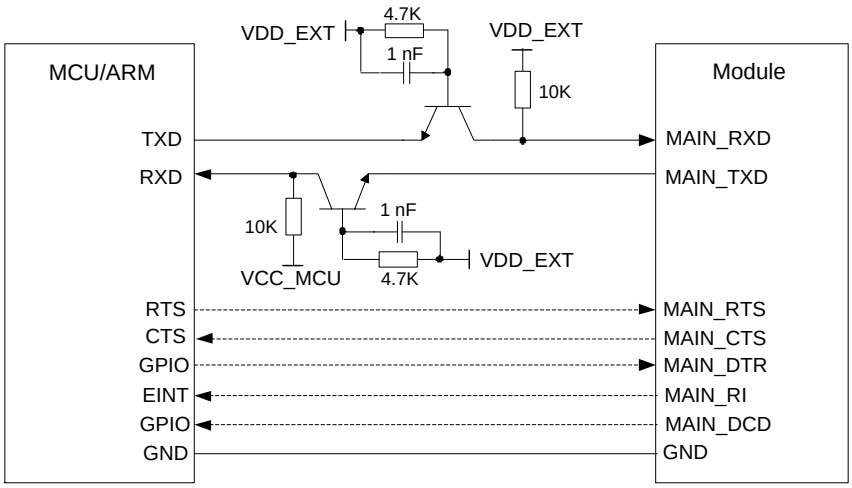


Figure 22: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.
3. When using pins 39, 40, and 48, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.12. SPI Interface

The module provides one SPI interface that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 16: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	4	DO	SPI chip select	1.8 V power domain. If unused, keep them open.
SPI_TXD	3	DO	SPI master mode output	
SPI_RXD	2	DI	SPI master mode input	
SPI_CLK	1	DO	SPI clock	

3.13. I2C and PCM Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface for an external codec IC. The PCM interface of the module only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally.

Table 17: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	57	OD	I2C serial clock	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
I2C_SDA	56	OD	I2C serial data	
PCM_DIN	59	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	60	DO	PCM data output	
PCM_SYNC	58	DI	PCM data frame sync	
PCM_CLK	61	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

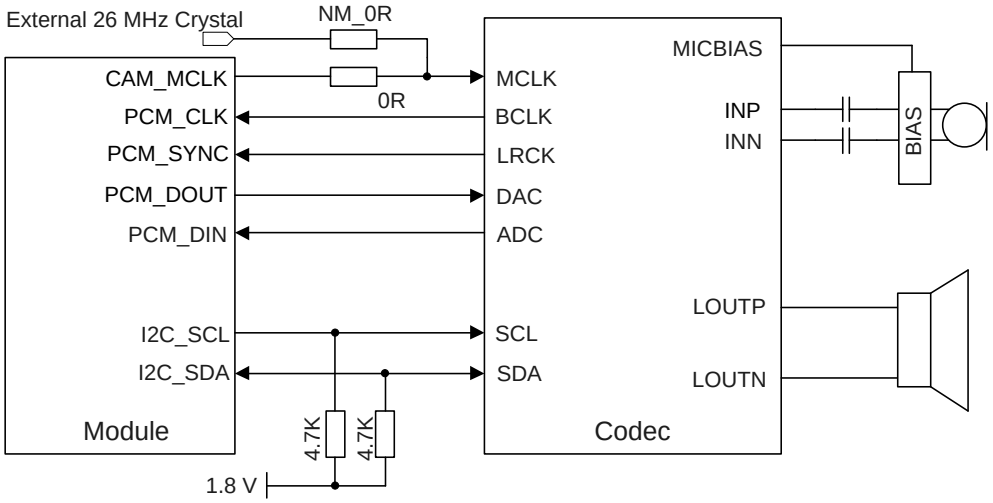


Figure 23: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

3.14. External Flash Interface

The module supports an external flash chip, and the external flash interface is multiplexed from other pins. Pin assignments are detailed in the figure below.

Table 18: External Flash Interface Multiplex Function Description

Pin Name	Pin No.	I/O	Multiplex Function	DC Characteristics	Description
PCM_SYNC	58	DO	SPI_FLASH1_CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	External NOR flash chip select
PCM_CLK	61	DO	SPI_FLASH1_CLK		External NOR flash clock
PCM_DIN	59	DIO	SPI_FLASH1_SIO_0	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	External NOR flash data bit 0
PCM_DOUT	60	DIO	SPI_FLASH1_SIO_1		External NOR flash data

				V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	bit 1
GPIO1	69	DIO	SPI_FLASH1_SIO_2		External NOR flash data bit 2
GPIO2	70	DIO	SPI_FLASH1_SIO_3		External NOR flash data bit 3

Pins 58–61 can be multiplexed into a general SPI interface for external 4-wire NOR flash. Pins 58–61, 69, 70 can be multiplexed into a dedicated SPI interface for external 6-wire NOR flash. The differences between the two are as follows.

- When the dedicated SPI interface is used for external NOR Flash, it supports file system, wear leveling, and FOTA upgrade.
- When the general SPI interface is used for external NOR Flash, it only supports basic flash reading, writing, and erasing. It does not support file system and can only be used for storage purpose.

See ***document [4]*** for the design details of the two interface circuits.

NOTE

See ***document [2]*** for details about pin multiplexing of the module.

3.15. Analog Audio Interfaces

The module provides two analog input and three analog output channels. The pin definition is shown in the following table.

Table 19: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS	25	PO	Bias voltage output for microphone	If unused, keep them open.
MIC_P	24	AI	Microphone analog input (+)	
MIC_N	23	AI	Microphone analog input (-)	
HEADMIC_BIAS	143	PO	Bias voltage output for headset	
HEADMIC_P	140	AI	Headset analog input (+)	

HEADMIC_N	141	AI	Headset analog input (-)	
HP_L	111	AO	Headset left channel output	
HP_R	112	AO	Headset right channel output	
AMP_VCOMP	94		Headset dedicated ground. It should be traced between the left and right channels, and connected to the GND of the headset jack, and then a via directly to the main GND layer.	
HP_DET	142	DI	Headset plug detection	
HEADMIC_IN_DET	93	DI	Headset audio input and headset audio input plug detection	
LOUDSPK_P	109	AO	Loudspeaker differential output (+)	With an internal PA. When configured as Class AB, the maximum drive power is 500 mW at 8 Ω load; when configured as Class D, the maximum drive power is 800 mW at 8 Ω load. If unused, keep them open.
LOUDSPK_N	110	AO	Loudspeaker differential output (-)	
SPK_P	22	AO	Analog audio differential output (+)	Used for receiver interface. Without internal PA. The maximum drive power is 50 mW at 32 Ω load. If the output power cannot meet the demand, this pin can be used to drive an external PA. If unused, keep them open.
SPK_N	21	AO	Analog audio differential output (-)	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used) and headset.
- AO channels are differential output channels, which can be applied for output of loudspeaker, receiver and headset.
- The module's internal PA is configured as Class AB by default.

3.15.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF

interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

To reduce radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces should not be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.15.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

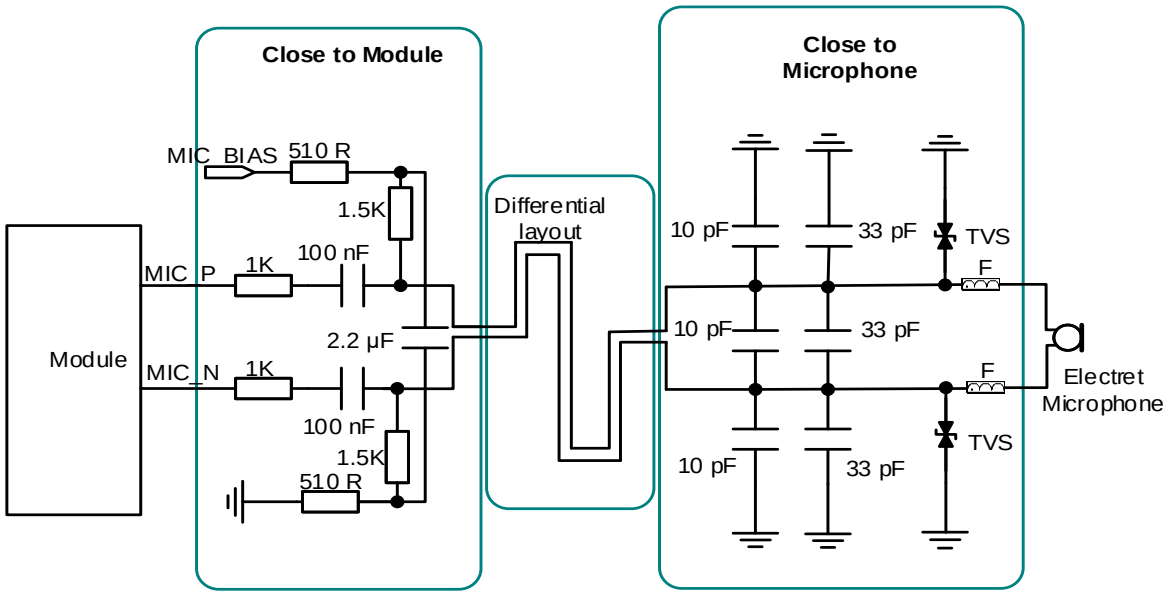


Figure 24: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

3.15.3. Loudspeaker Interface Design

The loudspeaker interface reference circuit is shown in the following figure.

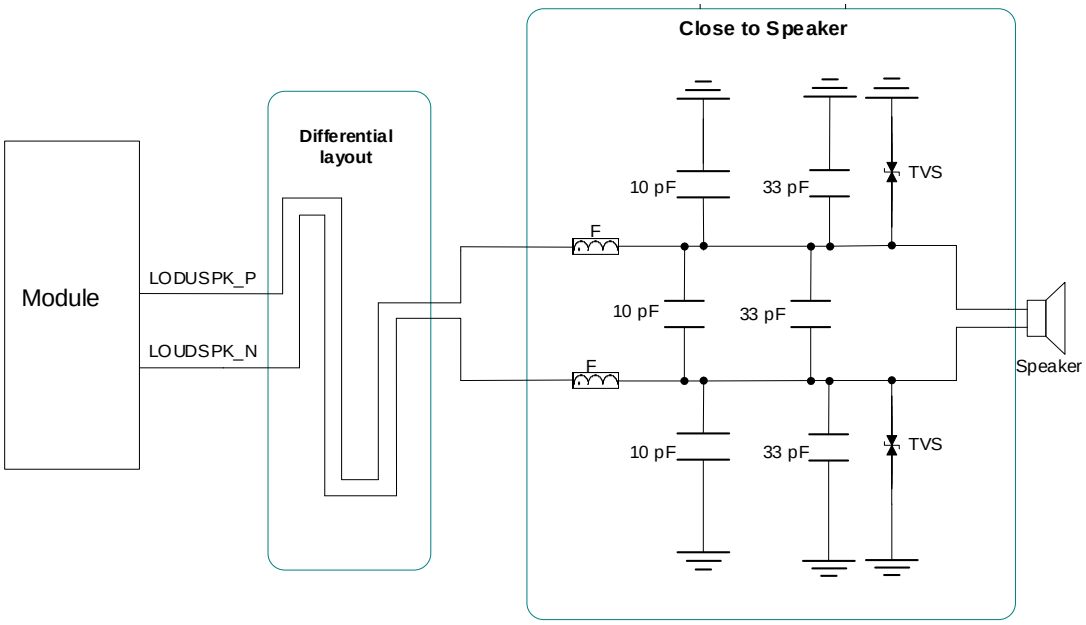


Figure 25: Reference Design for Loudspeaker Interface

3.15.4. Receiver Interface Design

The receiver interface reference circuit is shown in the following figure.

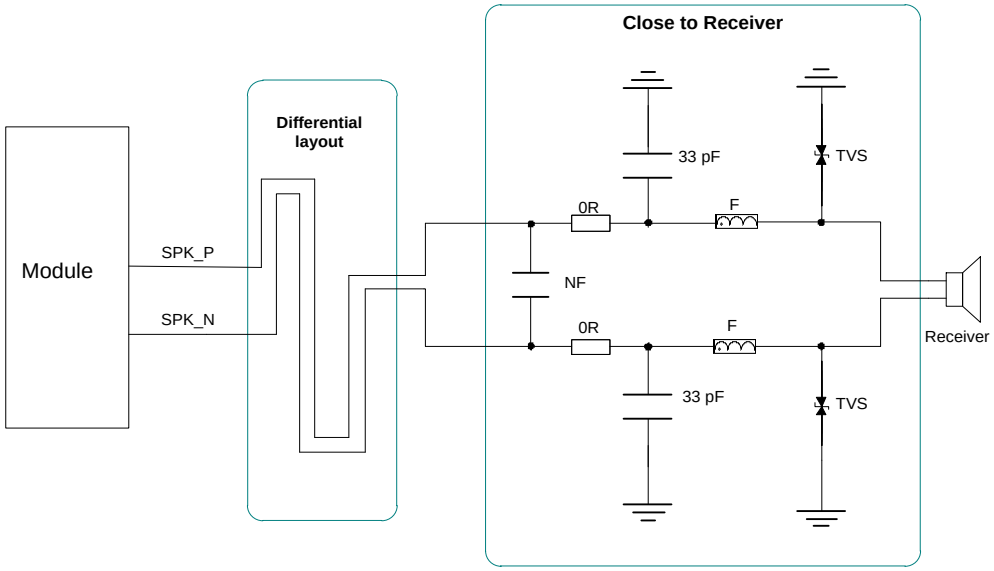


Figure 26: Reference Design for Receiver Interface

3.15.5. Headset Interface Design

The reference design for headset interface circuit compatible with CTIA and OMTP is shown in the following figure.

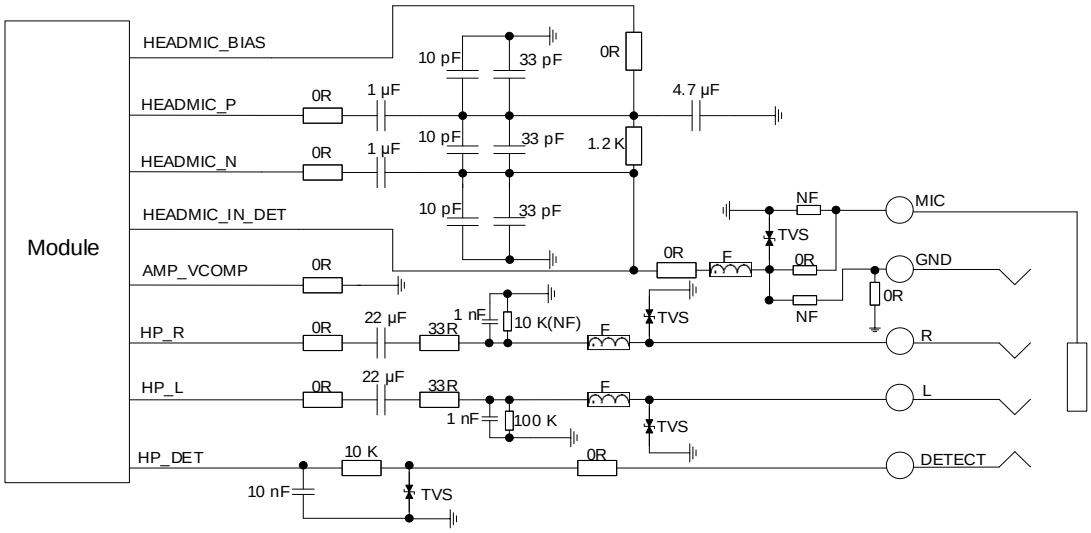


Figure 27: Reference Design for Headset Interface

3.16. LCM Interface

The LCM interface of the module supports the LCD display with a maximum resolution of 320 × 240, DMA transmission, as well as 16-bit RGB565 and YUV formats.

Table 20: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_TE	62	DI	LCD tearing effect	1.8 V power domain. If unused, keep them open.
LCD_RST	64	DO	LCD reset	
LCD_SEL	137	DO	Reserved	
LCD_SPI_CS	65	DO	LCD chip select	
LCD_SPI_CLK	67	DO	LCD clock	

LCD_SPI_RS	63	DO	LCD register select	
LCD_SPI_DOUT	66	DIO	LCD data	
LCD_ISINK	135	PI	Sink current input. Backlight adjustment.	It is driven by the current sink method and connected to the backlight cathode; the brightness can be adjusted with current control. Imax = 200 mA
LCD_VDDIO	134	PO	LCD digital power	LCD power supply. Vnom = 1.8 V. If unused, keep it open.
LCD_AVDD	138	PO	LCD analog power	LCD power supply. Vnom = 3.0 V. If unused, keep it open.

3.17. Matrix Keypad Interface

The module supports 5 × 6 matrix keypad interface. Besides, USB_BOOT and KEYOUT0 can be designed as a scan button. Press the button composed of USB_BOOT + KEYOUT0 before powering on the module, which will enter the download mode when it is turned on. See ***Chapter 3.25*** for details.

Table 21: Pin Definition of Matrix Keypad Interface

Pin Name	Pin No.	I/O	Description	Comment
KEYIN1	129	DI	Matrix keypad input 1	1.8 V power domain. If unused, keep them open.
KEYIN2	128	DI	Matrix keypad input 2	
KEYIN3	127	DI	Matrix keypad input 3	
KEYIN4	126	DI	Matrix keypad input 4	
KEYIN5	125	DI	Matrix keypad input 5	
KEYOUT0	105	DO	Matrix keypad output 0	
KEYOUT1	106	DO	Matrix keypad output 1	
KEYOUT2	107	DO	Matrix keypad output 2	
KEYOUT3	108	DO	Matrix keypad output 3	
KEYOUT4	104	DO	Matrix keypad output 4	

KEYOUT5	103	DO	Matrix keypad output 5

NOTE

Do not pull up KEYIN1 and USB_BOOT before turning on the module.

3.18. Charging Interface*

The module provides a charging interface that supports a minimum current of 300 mA and a maximum current of 1000 mA.

Table 22: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
VBAT_SENSE	29	AI	Battery voltage and charging current (combines with ISENSE) detection	Whether or not the charging function is used, this pin must be connected to the VBAT power supply, otherwise the module will not be powered on normally.
ISENSE	101	AI	Charging current detection	If unused, keep them open.
VDRV	102	AO	Charging control pin. Used for driving the MOS tube in the external charging circuit to adjust the charging current.	

To enhance the reliability and availability of the charging in your applications, please follow the criteria below in charging circuit design.

- The traces length between ISENSE and VBAT_SENSE from the module to the charging current detection resistor should be as short as possible, and they should be routed in a differential pair to avoid the influence of the trace impedance on the detection result.
- Pull out the VBAT_SENSE separately and connect it to one end of the charging current detection resistor (close to the positive electrode of the battery), and then connect the VBAT_RF to avoid affecting the detection of the battery voltage.
- The trace width of the charging path (from the USB_VBUS to the emitter electrode of the charging transistor, and from the collector of the charging transistor to the positive electrode of the battery) should not be less than 1.5 mm with sufficient margin.

- Charging circuit is a heat source when it is working. Pay attention to heat dissipation and keep it away from heat-sensitive devices.

3.19. SD Card Interface

The module provides an SD card interface compliant with SD 2.0 specification. The SD card interface is multiplexed from certain pins of the module. Pin assignments are detailed in the figure below.

Table 23: SD Card Multiplex Interface Pin Definition

Pin Name	Pin No.	I/O	Multiplex Function	Description	Comment
SDIO_VDD	133	PO	-	SD card IO power	It cannot be used for SD card power supply, but can be used for SDIO pull-up power supply only. If unused, keep it open.
SDIO1_CLK	132	DO	-	SD card clock	1.8/3.2 V power domain. If unused, keep them open.
MAIN_DCD	48	DO	SDIO1_CMD	SD card command	
MAIN_DTR	39	DIO	SDIO1_DATA0	SDIO1 data bit 0	
MAIN_RI	40	DIO	SDIO1_DATA1	SDIO1 data bit 1	
WAKEUP_IN	49	DIO	SDIO1_DATA2	SDIO1 data bit 2	
AP_READY	50	DIO	SDIO1_DATA3	SDIO1 data bit 3	
I2C_SDA	56	DI	SD_DET	SD card hot-plug detect	1.8 V power domain. If unused, keep it open.

The reference design circuit is shown in the figure below.

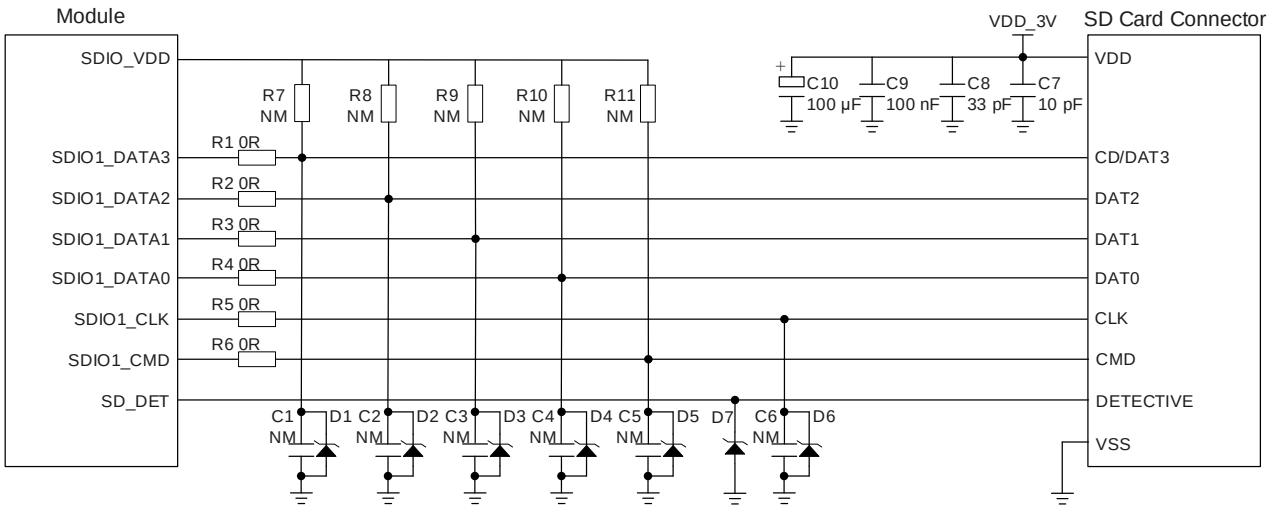


Figure 28: SD Card Interface Reference Design

To ensure good performance and reliability of the SD card, the following principles are recommended in the circuit design of the SD card interface.

- The voltage range of VDD_3V, power supply for the SD card, is 2.7–3.6 V and it should provide at least 800 mA current. SDIO_VDD, of which the maximum output current is 50 mA, is the module output power and can only be used for SDIO pull-up. SD card needs to be powered externally.
- To avoid the jitter of bus, it is necessary to reserve pull-up resistors R7–R11 on the SDIO signal traces. Value range of these resistors should be 10–100 kΩ and the recommended value is 100 kΩ. The pull-up power supply should be the SDIO_VDD of the module.
- To adjust signal quality, it is necessary to add resistors R1–R6 in series between the module and the SD card connector and the recommended value is 0 Ω. The bypass capacitors C1–C6 are reserved and not mounted by default. The resistors and capacitors should be placed close to the module when placing the PCB.
- For good ESD protection, it is recommended to add a TVS diode to each SD card pin, and place them as close to the SD card connector as possible. The parasitic capacitance of ESD components should be less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.
- Route SDIO signals with ground surrounded. The impedance of SDIO data trace should be kept at 50 Ω ±10 %.
- Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.
- Keep the trace length difference among SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD less than 1 mm and the total routing length should be less than 50 mm.

NOTE

1. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.
2. See ***document [2]*** for details about pin multiplexing of the module.

3.20. SDIO Interface*

The module provides an SDIO interface compliant with SDIO specification version 1.1. It can be used to connect an external WLAN chip.

Table 24: SDIO Interface Pin Description

Pin Name	Pin No.	I/O	Description	Comment
SDIO2_CLK	118	DO	SDIO2 clock	1.8 V power domain. If unused, keep them open.
SDIO2_CMD	99	DO	SDIO2 command	
SDIO2_DATA0	98	DIO	SDIO2 data bit 0	
SDIO2_DATA1	95	DIO	SDIO2 data bit 1	
SDIO2_DATA2	119	DIO	SDIO2 data bit 2	
SDIO2_DATA3	100	DIO	SDIO2 data bit 3	

The data transmission rate of the SDIO interface is very high. To ensure that the interface design complies with the SDIO 1.1 specification, it is recommended to follow the wiring principles below.

- Route SDIO signals with ground surrounded. The impedance of SDIO data trace should be kept at 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.
- Keep the trace length difference among SDIO2_CLK, SDIO2_DATA[0:3] and SDIO2_CMD less than 1 mm and the total routing length should be less than 50 mm.
- Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.

3.21. ADC Interfaces

The module provides four analog-to-digital converter (ADC) interfaces. You can use **AT+QADC=0** to read the voltage value on ADC0, **AT+QADC=1** the voltage value on ADC1, **AT+QADC=2** the voltage value on ADC2, and **AT+QADC=3** the voltage value on ADC3. See ***document [3]*** for more details.

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 25: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC3	114	General-purpose ADC interface	A 1 kΩ resistor must be connected in series when in use. If unused, keep them open.
ADC2	113	General-purpose ADC interface	
ADC1	20	General-purpose ADC interface	
ADC0	19	General-purpose ADC interface	

Table 26: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage at ADC3	0	-	VBAT	V
Voltage at ADC2	0	-	VBAT	V
Voltage at ADC1	0	-	VBAT	V
Voltage at ADC0	0	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

If the input voltage of ADC interfaces is designed with a voltage divider circuit, the resistance value of the external divider resistor must be less than 100 kΩ. Otherwise, the ADC measurement accuracy will be reduced significantly.

3.22. PSM Interface*

The module supports power saving mode (PSM). It enters the PSM through the following AT commands when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling up the PSM_EXT_INT pin externally or setting the timer by software will enable the module to exit PSM.

Table 27: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description	Comment
PSM_EXT_INT*	116	DI	External interrupt pin. Wakes up the module from PSM when being pulled high externally.	Active high. If unused, keep it open.

A reference circuit is shown in the following figure.

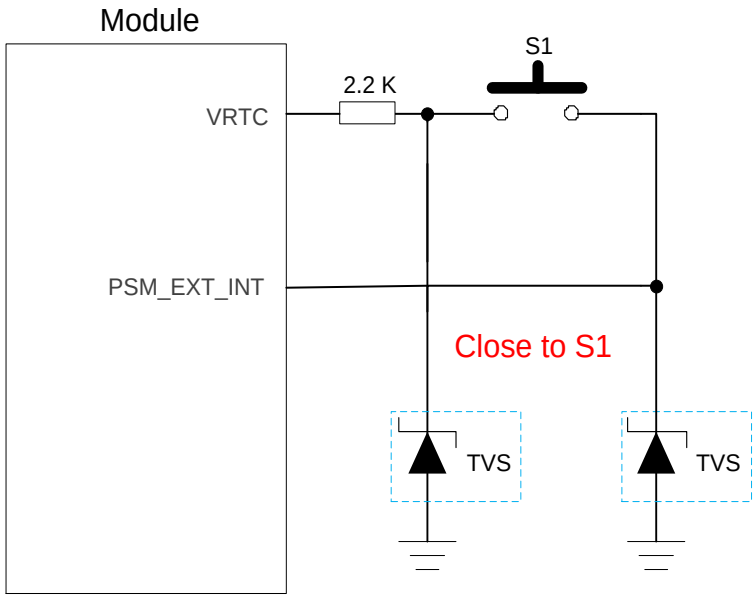


Figure 29: Reference Circuit of Waking up Module from PSM

3.23. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can drive the network status indicators. The following tables describe pin definition and logic level changes in different network status.

Table 28: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	52	DO	Indicates whether the module has registered on LTE network	1.8 V power domain. If unused, keep them open.
NET_STATUS	54	DO	Indicates the module's network activity status	

Table 29: Working State of Network Connection Status/Activity Indication

Pin Name	Status	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Registered on network and idle
	Flicker rapidly (63 ms low/62 ms high)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

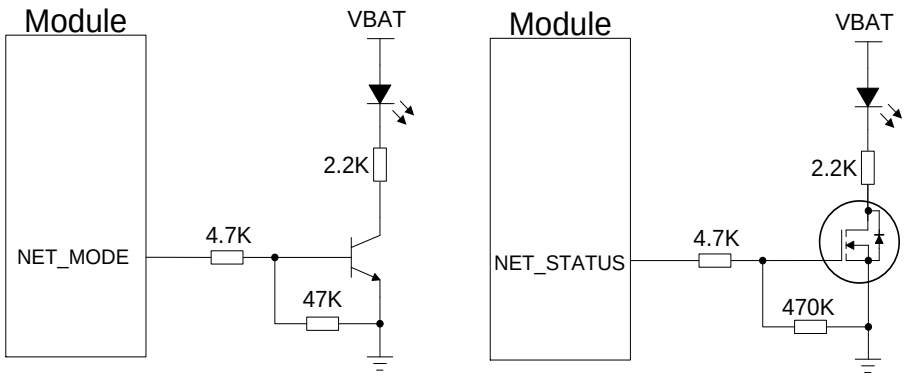


Figure 30: Reference Circuit of Network Status Indication

3.24. Behaviors of MAIN_RI

You can configure MAIN_RI behaviors with **AT+QCFG="risignaltype","physical"**. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 30: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behaviors can be changed via **AT+QCFG="urc/ri/ring"**. See ***document [3]*** for details.

NOTE

1. The **AT+QURCCFG** allows you to set the main UART, USB AT port, or USB modem port as the URC output port. The default setting is USB AT port.
2. When using MAIN_RI (pin 40), please note that the pin will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before it can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific

usage scenario and circuit design.

3.25. USB_BOOT Interface

The module provides a USB_BOOT interface. You can pull up USB_BOOT to VDD_EXT before power-up and the module will enter download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Alternatively, pressing the scan button of USB_BOOT + KEYOUT0 before the module is powered on will also enable the module to enter the download mode when it is turned on.

Table 31: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	55	DI	Control pin for the module to enter download mode	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

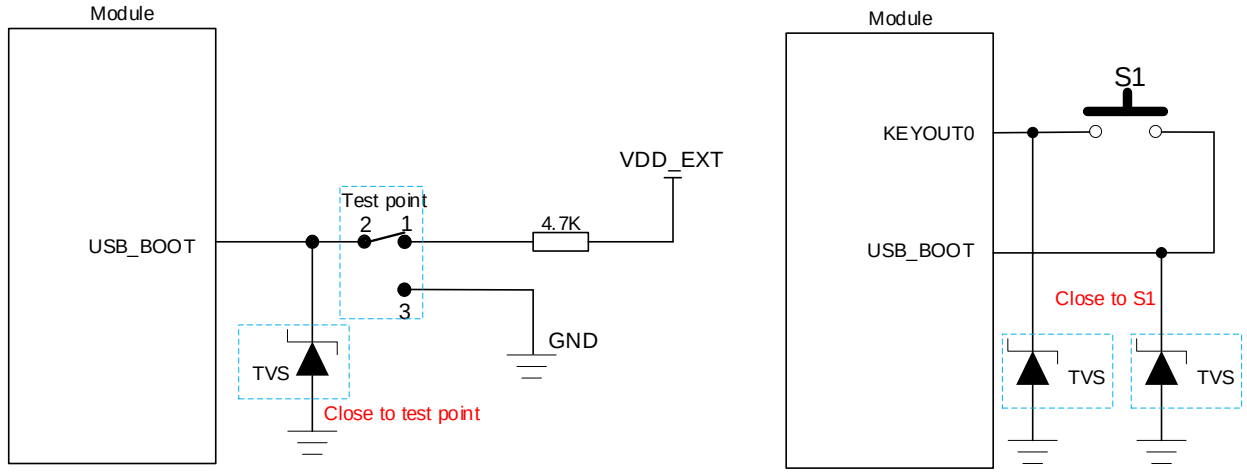


Figure 31: Reference Circuit of USB_BOOT Interface

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.

3.26. Camera Interface

The module provides one camera interface supporting cameras up to 0.3 MP and the 2-data-line transmission of SPI.

Table 32: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_I2C_SCL	11	OD	I2C clock of camera	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	12	OD	I2C data of camera	
CAM_MCLK	10	DO	Master clock of camera	1.8 V power domain. If unused, keep them open.
CAM_SPI_CLK	13	DI	SPI clock of camera	
CAM_SPI_DATA0	14	DI	SPI data0 of camera	
CAM_SPI_DATA1	15	DI	SPI data1 of camera	
CAM_PWDN	16	DO	Power down of camera	
CAM_RST	120	DO	Reset of camera	
CAM_VDD	17	PO	Analog power supply of camera	Power supply of camera. If unused, keep them open.
CAM_VDDIO	68	PO	Digital power supply of camera	

NOTE

If the camera interface is not required, the pins 11 and 12 can be used as an I2C interface to connect other peripherals.

4 Antenna Interfaces

The module provides a main antenna interface and a Bluetooth/Wi-Fi Scan antenna interface. The impedance of antenna ports is 50 Ω.

4.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna Interfaces

4.1.1. Pin Definition

Table 33: Pin Definition of Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_BT/ WIFI_SCAN	42	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω impedance. If unused, keep it open.
ANT_MAIN	46	AIO	Main antenna	50 Ω impedance.

4.1.2. Operating Frequency

Table 34: EC600U-EU QuecOpen® Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz

LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 35: EC600U-CN QuecOpen® Operating Frequencies

3GPP Band	Transmit	Receive	Unit
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

NOTE

Only EC600U-EU QuecOpen supports GSM frequency bands.

4.1.3. Reference Design of Antenna Interface

A reference design of ANT_MAIN pin and ANT_BT/WIFI_SACN pin are shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

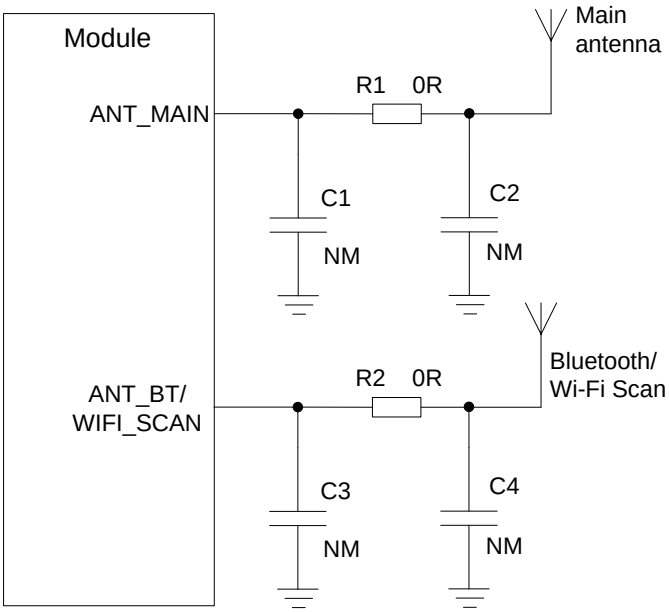


Figure 32: Reference Circuit of RF Antenna

NOTE

1. To improve the receiving sensitivity, ensure that the main antenna and the Bluetooth/Wi-Fi Scan receiving antenna are placed at a proper distance.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

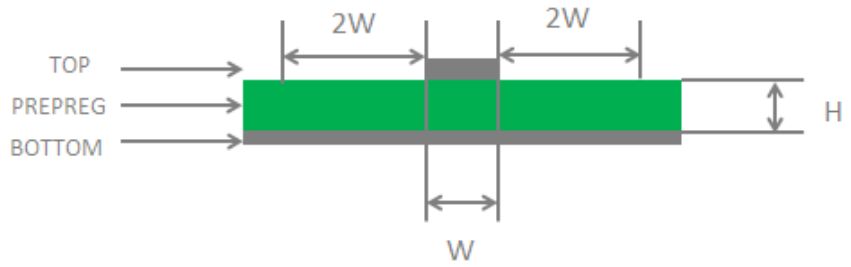


Figure 33: Microstrip Design on a 2-layer PCB

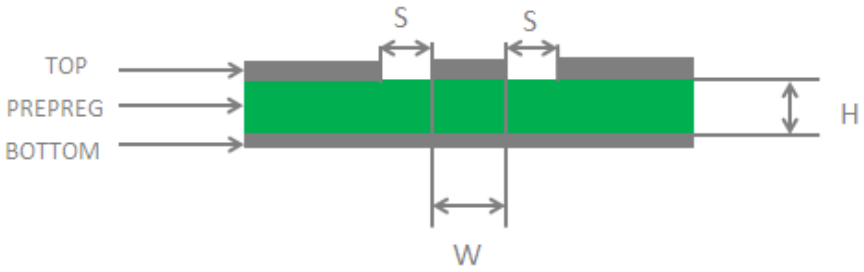


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

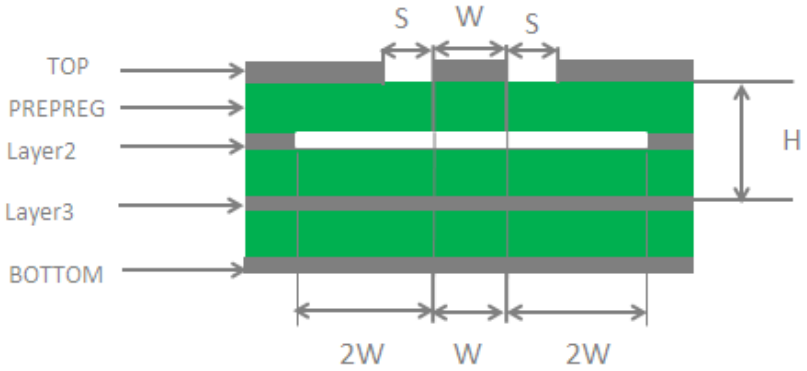


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

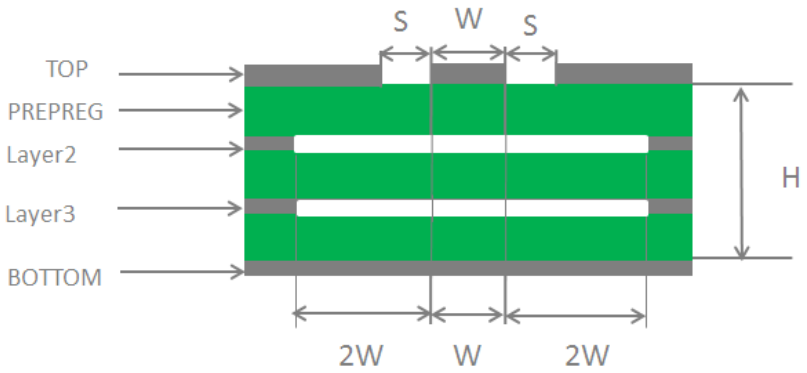


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

NOTE

1. The external LDO power supply can be used according to the active antenna type.
2. A VDD circuit is not required in the design for passive antenna.

4.2. Antenna Installation

4.2.1. Antenna Design Requirement

Table 36: Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB: LB (< 1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)

4.2.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

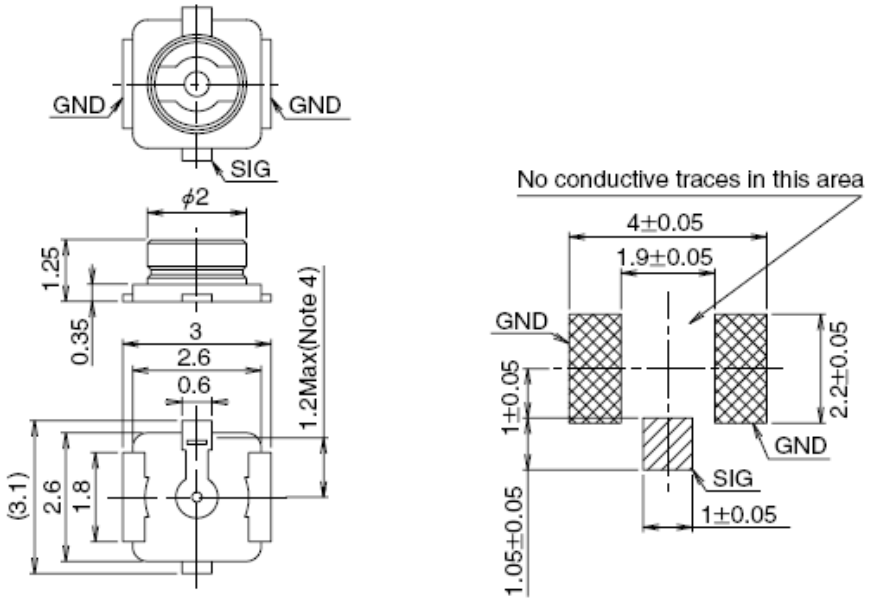


Figure 37: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

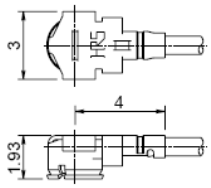
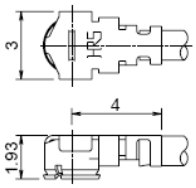
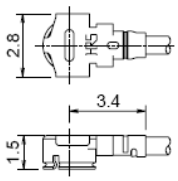
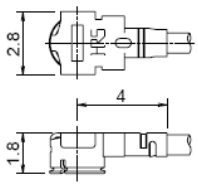
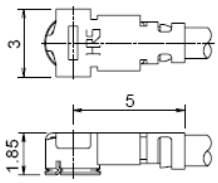
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

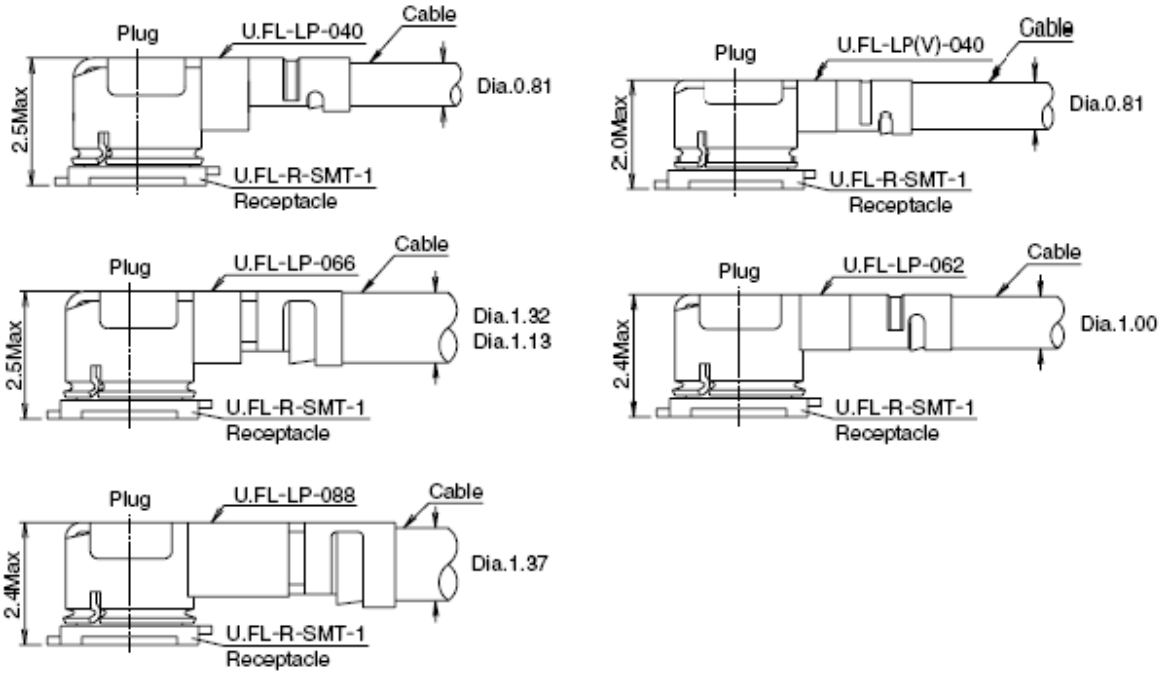


Figure 39: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

5 Reliability, Radio and Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_RF (EC600U-CN QuecOpen)	-	1.5	A
Peak Current of VBAT_RF (EC600U-EU QuecOpen)	-	2.5	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V
Voltage at ADC2	0	VBAT	V
Voltage at ADC3	0	VBAT	V

5.2. Power Supply Ratings

Table 38: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission		-	-	400	mV
I_{VBAT}	EC600U-EU QuecOpen peak supply current (during transmission slot)	Maximum power control level on EGSM900.	-	2.3	2.5	A
	EC600U-CN QuecOpen peak supply current (during transmission slot)		-	1.2	1.5	A
USB_VBUS	USB connection detection		3.5	5.0	5.25	V

5.3. Operating and Storage Temperatures

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	ºC
Extended Operation Range [5]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[4] Within the operating temperature range, the module meets 3GPP specifications.
[5] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

5.4. Power Consumption

Table 40: EC600U-CN QuecOpen® Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	33	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.29	mA
	AT+CFUN=4 (USB disconnected)	1.29	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.7	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.05	mA
	LTE-FDD @ PF = 64 (USB suspend)	3.56	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.68	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.59	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.6	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.49	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.69	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.49	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	12.34	mA
	LTE-FDD @ PF = 64 (USB connected)	27.78	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.46	mA
	LTE-TDD @ PF = 64 (USB connected)	27.88	mA
LTE data transfer	LTE-FDD B1 @ 22.88 dBm	624	mA
	LTE-FDD B3 @ 22.97 dBm	623	mA
	LTE-FDD B5 @ 23.07 dBm	552	mA
	LTE-FDD B8 @ 22.85 dBm	510	mA

	LTE-TDD B34 @ 22.80 dBm	287	mA
	LTE-TDD B38 @ 23.15 dBm	332	mA
	LTE-TDD B39 @ 22.95 dBm	277	mA
	LTE-TDD B40 @ 23.64 dBm	301	mA
	LTE-TDD B41 @ 22.70 dBm	343	mA

Table 41: EC600U-EU QuecOpen® Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	34	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.37	mA
	AT+CFUN=4 (USB disconnected)	1.37	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.87	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.37	mA
	EGSM900 @ DRX = 5 (USB suspend)	3.6	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.2	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.86	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.35	mA
	DCS1800 @ DRX = 5 (USB suspend)	3.6	mA
	DCS1800 @ DRX = 9 (USB disconnected)	2.2	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.68	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.06	mA
	LTE-FDD @ PF = 64 (USB suspend)	3.27	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.73	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.57	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.72	mA

	LTE-TDD @ PF = 64 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.52	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.74	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.58	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.21	mA
	EGSM900 @ DRX = 5 (USB connected)	28.67	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.9	mA
	LTE-FDD @ PF = 64 (USB connected)	28.38	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.85	mA
	LTE-TDD @ PF = 64 (USB connected)	28.34	mA
GPRS data transfer	GSM850 4DL/1UL @ 33.1 dBm	262	mA
	GSM850 3DL/2UL @ 30.9 dBm	397	mA
	GSM850 2DL/3UL @ 28.9 dBm	448	mA
	GSM850 1DL/4UL @ 26.7 dBm	464	mA
	EGSM900 4DL/1UL @ 32.5 dBm	254	mA
	EGSM900 3DL/2UL @ 30.9 dBm	386	mA
	EGSM900 2DL/3UL @ 28.9 dBm	440	mA
	EGSM900 1DL/4UL @ 26.8 dBm	464	mA
	DCS1800 4DL/1UL @ 29.4 dBm	169	mA
	DCS1800 3DL/2UL @ 27.9 dBm	249	mA
	DCS1800 2DL/3UL @ 25.8 dBm	273	mA
	DCS1800 1DL/4UL @ 23.7 dBm	286	mA
	PCS1900 4DL/1UL @ 29.8 dBm	183	mA
	PCS1900 3DL/2UL @ 27.9 dBm	267	mA
	PCS1900 2DL/3UL @ 25.8 dBm	296	mA

	PCS1900 1DL/4UL @ 23.7 dBm	315	mA
LTE data transfer	LTE-FDD B1 @ 22.99 dBm	693	mA
	LTE-FDD B3 @ 22.97 dBm	703	mA
	LTE-FDD B5 @ 23.86 dBm	627	mA
	LTE-FDD B7 @ 22.73 dBm	783	mA
	LTE-FDD B8 @ 22.73 dBm	702	mA
	LTE-FDD B20 @ 22.73 dBm	597	mA
	LTE-FDD B28 @ 22.73 dBm	655	mA
	LTE-TDD B38 @ 23.49 dBm	421	mA
	LTE-TDD B40 @ 23.77 dBm	391	mA
	LTE-TDD B41 @ 23.15 dBm	418	mA
GSM voice call	GSM850 PCL = 5 @ 33.0 dBm	293	mA
	GSM850 PCL = 12 @ 18.9 dBm	119	mA
	GSM850 PCL = 19 @ 5.2 dBm	91	mA
	EGSM900 PCL = 5 @ 32.4 dBm	269	mA
	EGSM900 PCL = 12 @ 19.1 dBm	121	mA
	EGSM900 PCL = 19 @ 5.5 dBm	82	mA
	DCS1800 PCL = 0 @ 29.4 dBm	185	mA
	DCS1800 PCL = 7 @ 16.1 dBm	96	mA
	DCS1800 PCL = 15 @ 0.9 dBm	79	mA
	PCS1900 PCL = 0 @ 29.8 dBm	199	mA
	PCS1900 PCL = 7 @ 16.1 dBm	98	mA
	PCS1900 PCL = 15 @ 0.9 dBm	79	mA

5.5. Tx Power

Table 42: EC600U-CN QuecOpen® RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 43: EC600U-EU QuecOpen® RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 6 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. Rx Sensitivity

Table 44: EC600U-CN QuecOpen® Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary + Diversity
LTE-FDD B1 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.6 dBm	-93.3 dBm

LTE-FDD B5 (10 MHz)	-99.4 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.5 dBm	-93.3 dBm
LTE-TDD B34 (10 MHz)	-99.2 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-99.1 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-99.0 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-99.1 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.7 dBm	-94.3 dBm

Table 45: EC600U-EU QuecOpen® Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
GSM850	-108.2 dBm	-102 dBm
EGSM900	-108.1 dBm	-102 dBm
DCS1800	-107.8 dBm	-102 dBm
PCS1900	-107.7 dBm	-102 dBm
LTE-FDD B1 (10 MHz)	-98.2 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.5 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.8 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.6 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-99.1 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99.3 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-97.6 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.5 dBm	-94.3 dBm

5.7. ESD Protection

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatics discharge characteristics of the module.

Table 46: Electrostatics Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

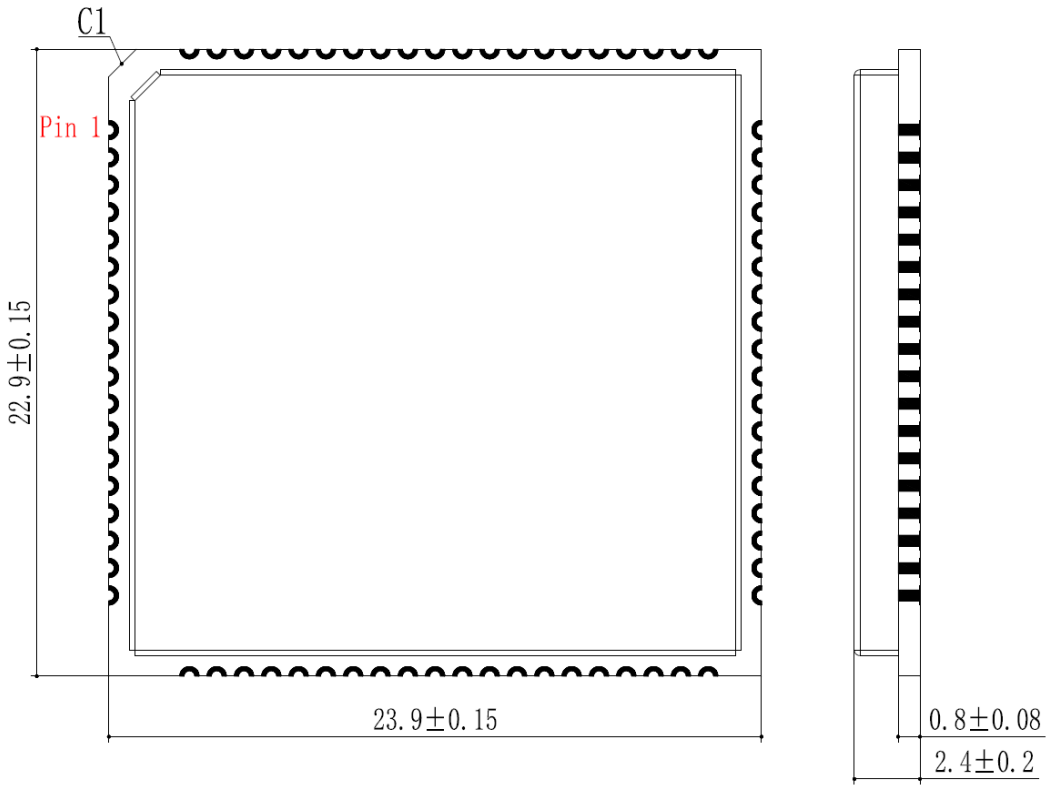


Figure 40: Module Top and Side Dimensions

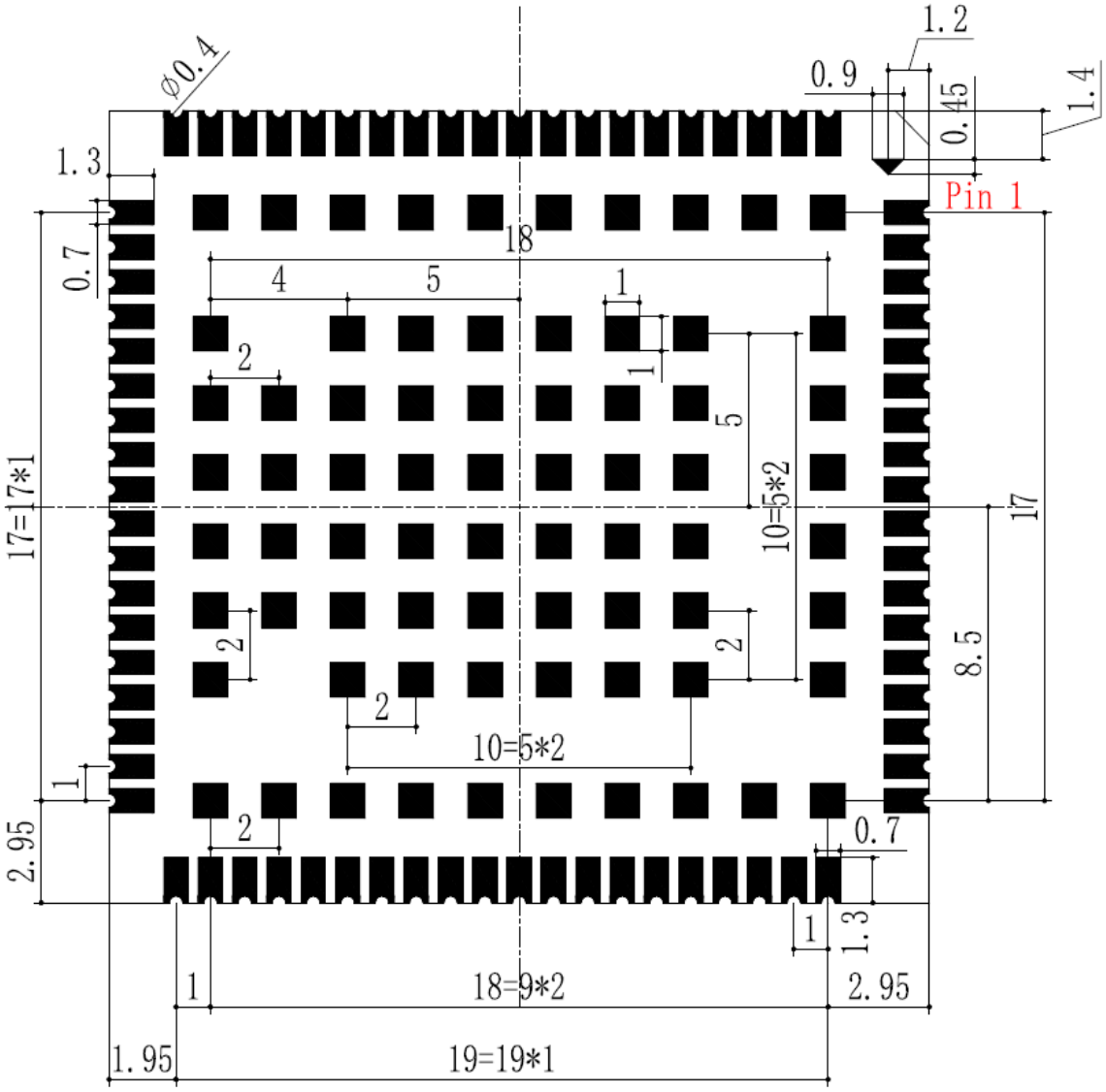


Figure 41: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

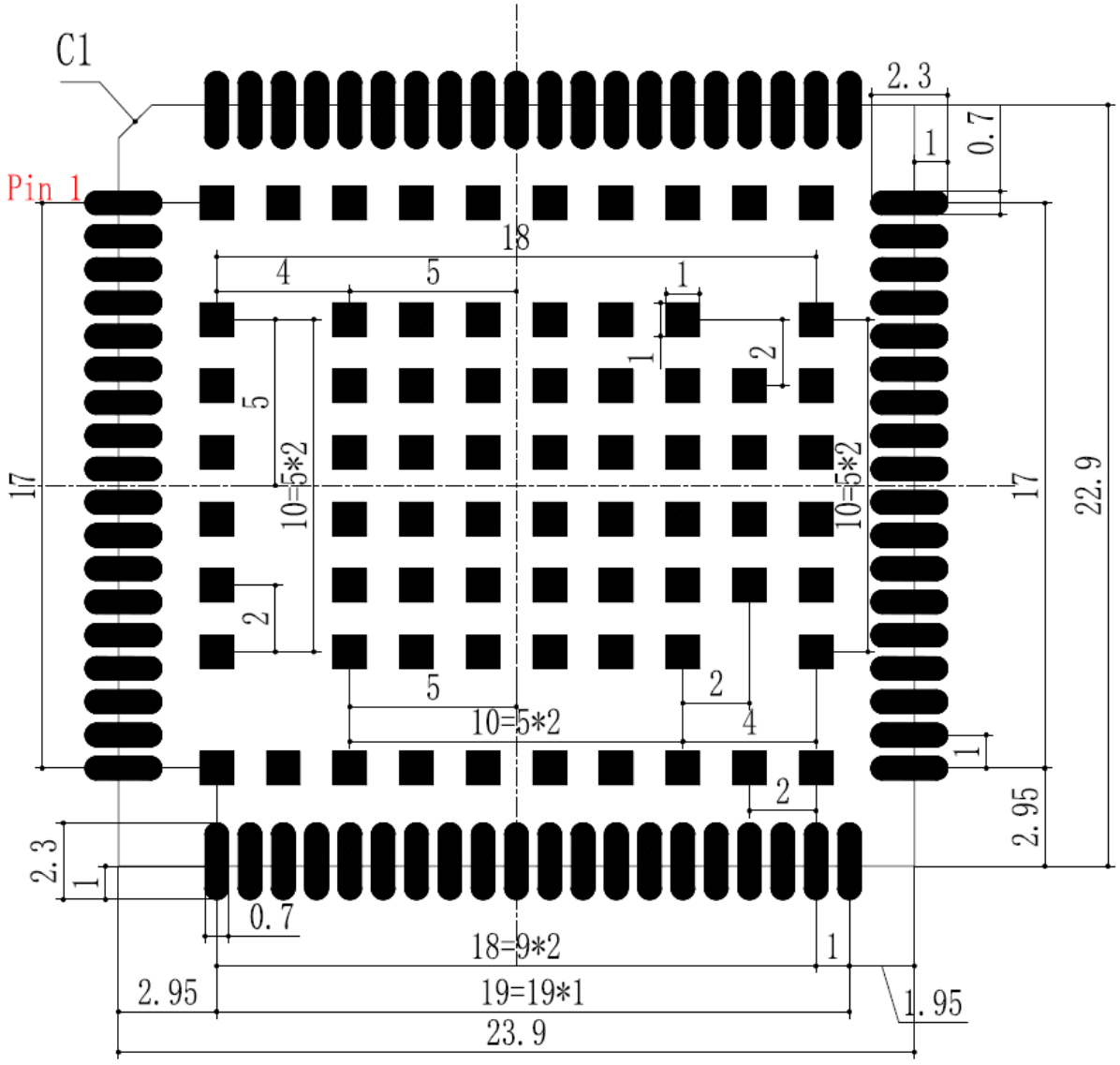


Figure 42: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

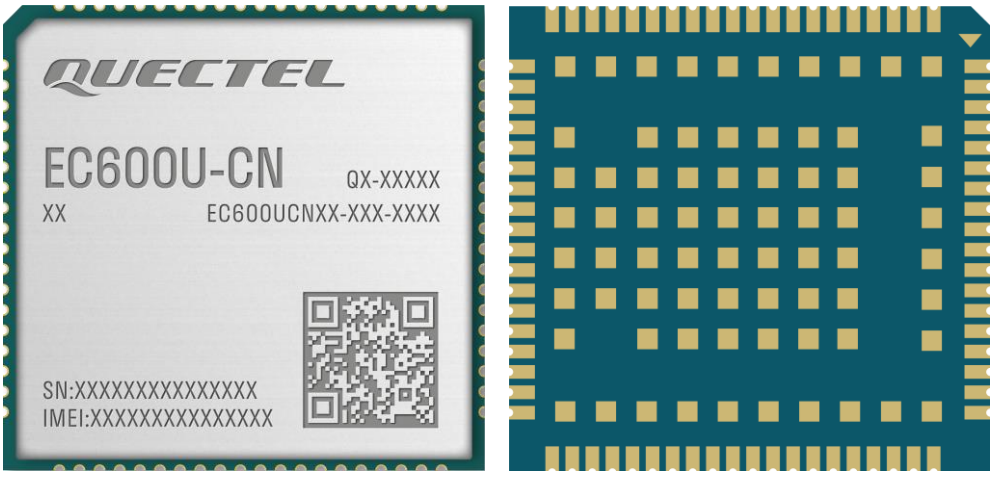


Figure 43: Top and Bottom Views of EC600U-CN QuecOpen®

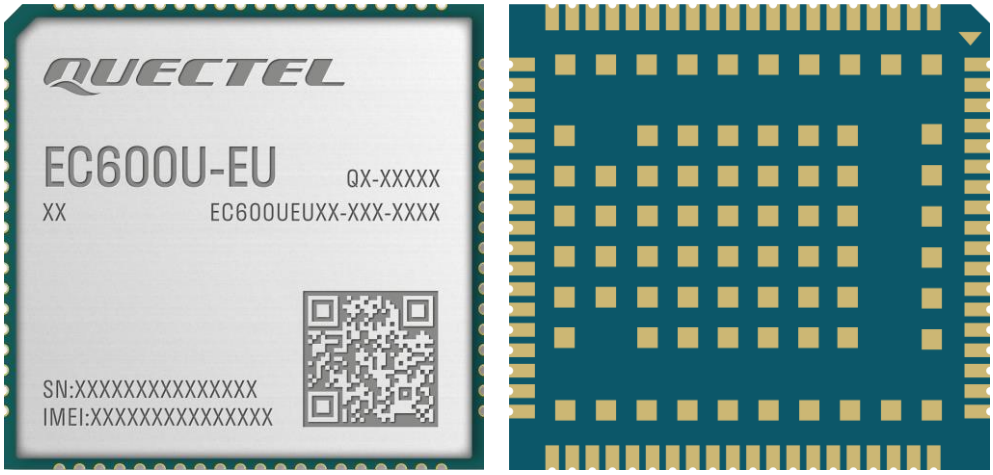


Figure 44: Top and Bottom Views of EC600U-EU QuecOpen®

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

Module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [6] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

put in a dry environment such as in a drying oven.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [6]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

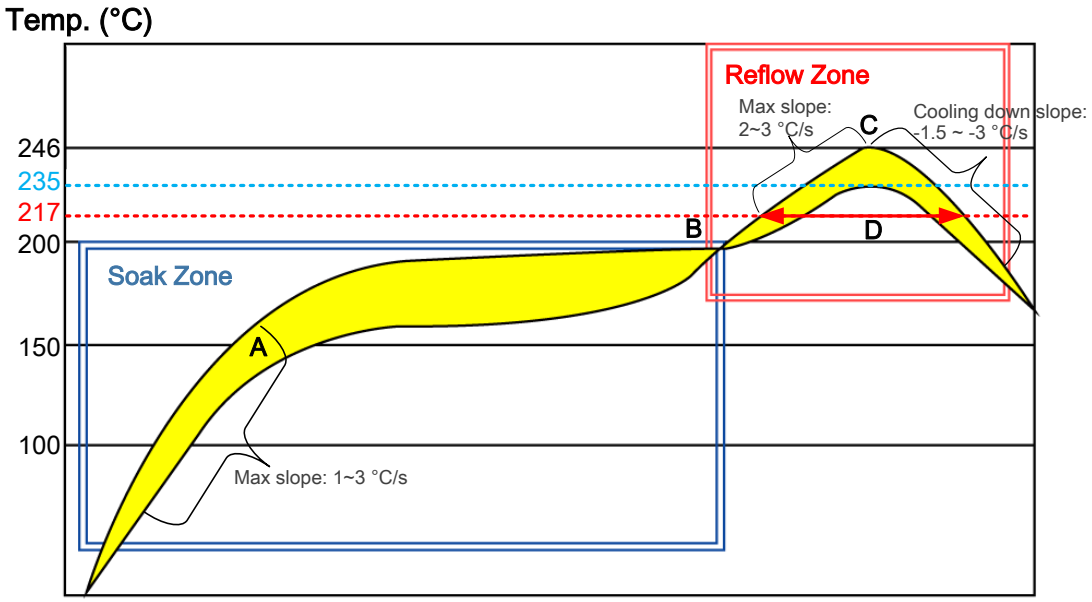


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 47: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

7.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

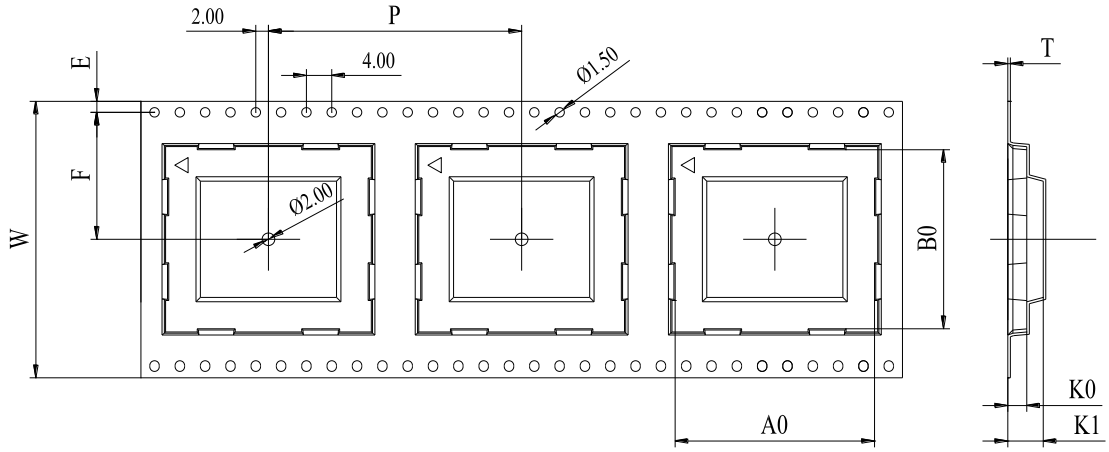


Figure 46: Carrier Tape Dimension Drawing

Table 48: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	24.4	23.4	3.1	6.5	20.2	1.75

7.3.2. Plastic Reel

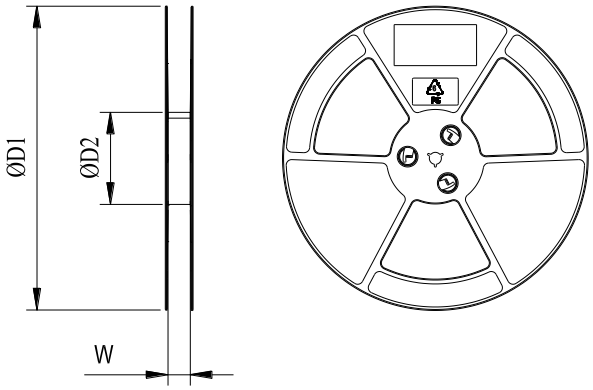
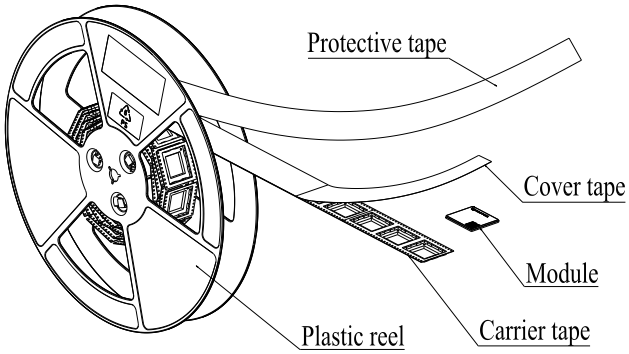


Figure 47: Plastic Reel Dimension Drawing

Table 49: Plastic Reel Dimension Table (Unit: mm)

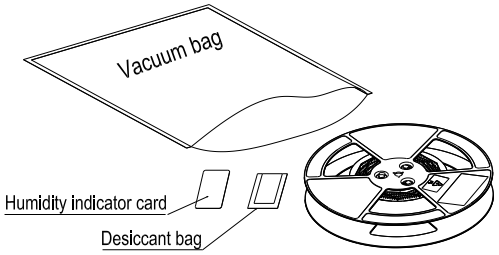
øD1	øD2	W
330	100	44.5

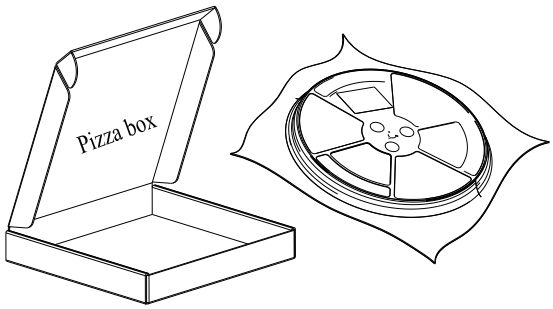
7.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

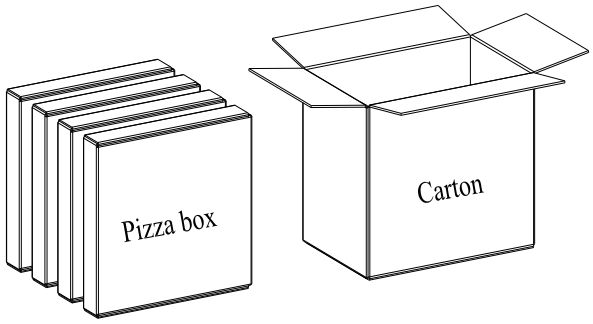


Figure 48: Packaging Process

8 Appendix References

Table 50: Related Documents

Document Name
[1] Quectel_LTE_OPEN_EVB_User_Guide
[2] Quectel_EC600U_Series_QuecOpen_GPIO_Configuration
[3] Quectel_ECx00U&EGx00U&EG915U_Series_AT_Commands_Manual_V1.0
[4] Quectel_EC600U_Series_QuecOpen_Reference_Design
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_SMT_User_Guide

Table 51: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-Rate
ADC	Analog-to-Digital Converter
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DCXO	Digital Controlled Crystal Oscillators
DL	Downlink
DMA	Direct Memory Access
DTE	Data Terminal Equipment

DTR	Data Terminal Ready
EGSM	Enhanced GSM
EMI	Electro-Magnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FDD	Frequency Division Duplex
FOTA	Firmware Over-The-Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL/FTP Secure
GSM	Global System for Mobile Communications
HB	High Band
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
LB	Low Band
LCC	Leadless Chip Carrier (package)
LCD	Liquid Crystal Display
LCM	LCD Module/liquid crystal monitor
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution

M2M	Machine to Machine
MB	Mid Band
MCU	Microcontroller Unit
ME	Mobile Equipment
MMS	Multimedia Messaging Service
MO	Mobile Originating/Originated
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
MT	Mobile Terminating/Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PA	Power Amplifier
PAP	Password Authentication Protocol
PAM	Power Amplifier Module
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PMIC	Power Management IC
PMU	Power Management Unit
POS	Point of Sale
PPP	Point-to-Point Protocol
P_{PP}	Peak Pulse Power
PSM	Power Saving Mode

PRx	Primary Receive
RF	Radio Frequency
RGB	Red, Green, Blue
RTS	Ready To Send/Request to Send
SAW	Surface Acoustic Wave
SMS	Short Message Service
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
Tx	Transmit/Transmission
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
Vnom	Nominal Voltage

V_O	Voltage Output
$V_{OH}max$	Maximum High-level Output Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
$V_{OL}min$	Minimum Low-level Output Voltage
V_{RWM}	Peak Reverse Working Voltage
VSWR	Voltage Standing Wave Ratio