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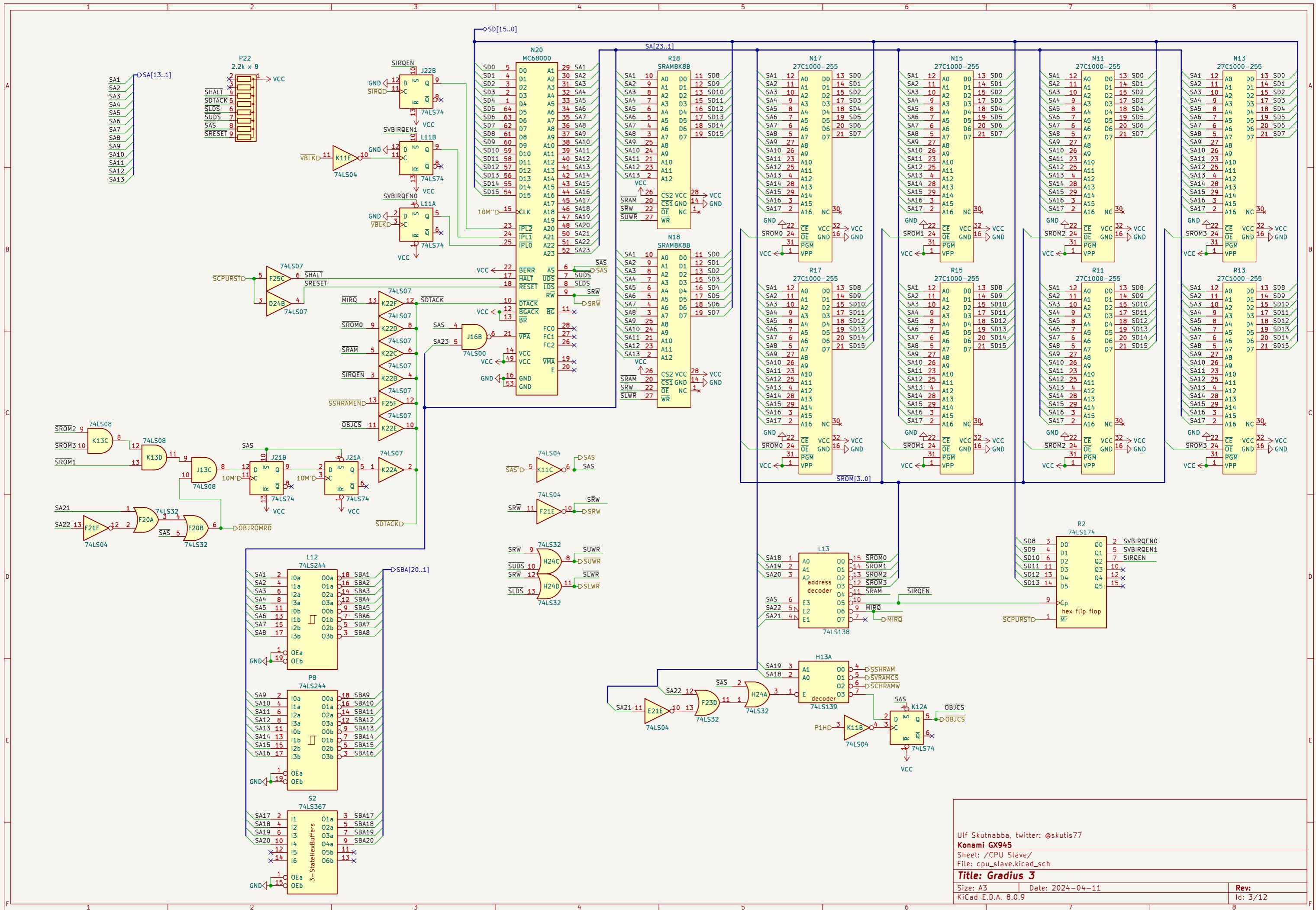
Konami GX945

Sheet: /CPU Master/
File: cpu_master.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11
KiCad E.D.A. 8.0.9

Rev: Id: 2/12



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Sheet: /CPU Slave/

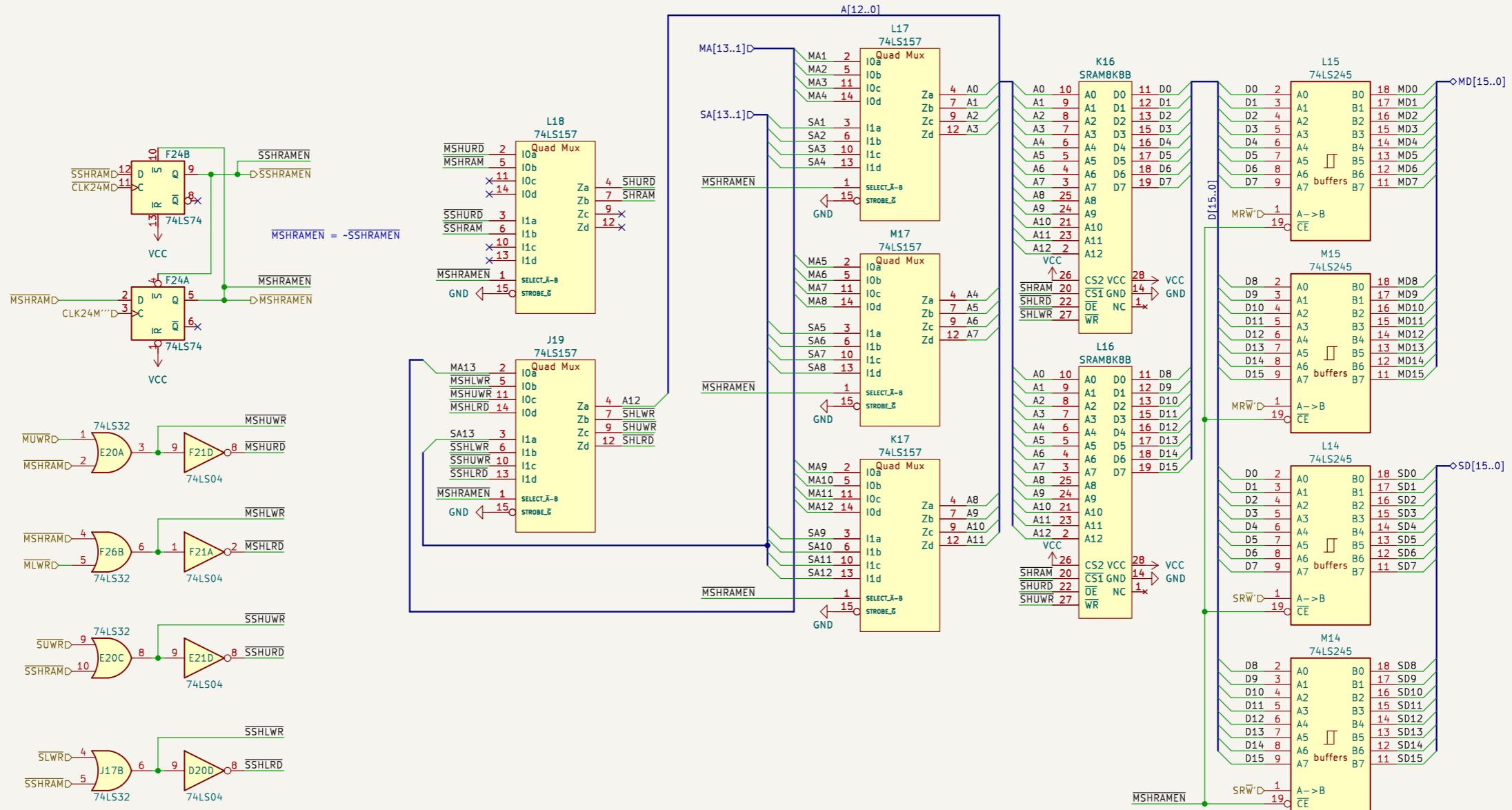
File: cpu_slave.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11

KiCad E.D.A. 8.0.9

Rev: 3/12



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Sheet: /Shared RAM/

File: shram.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11

KiCad E.D.A. 8.0.9

Rev:

Id: 4/12

1 2 3 4 5 6 7 8

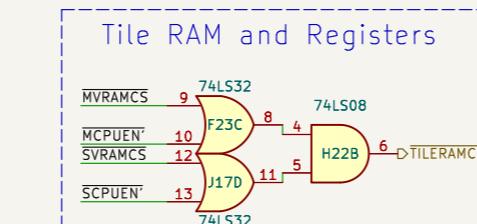
A



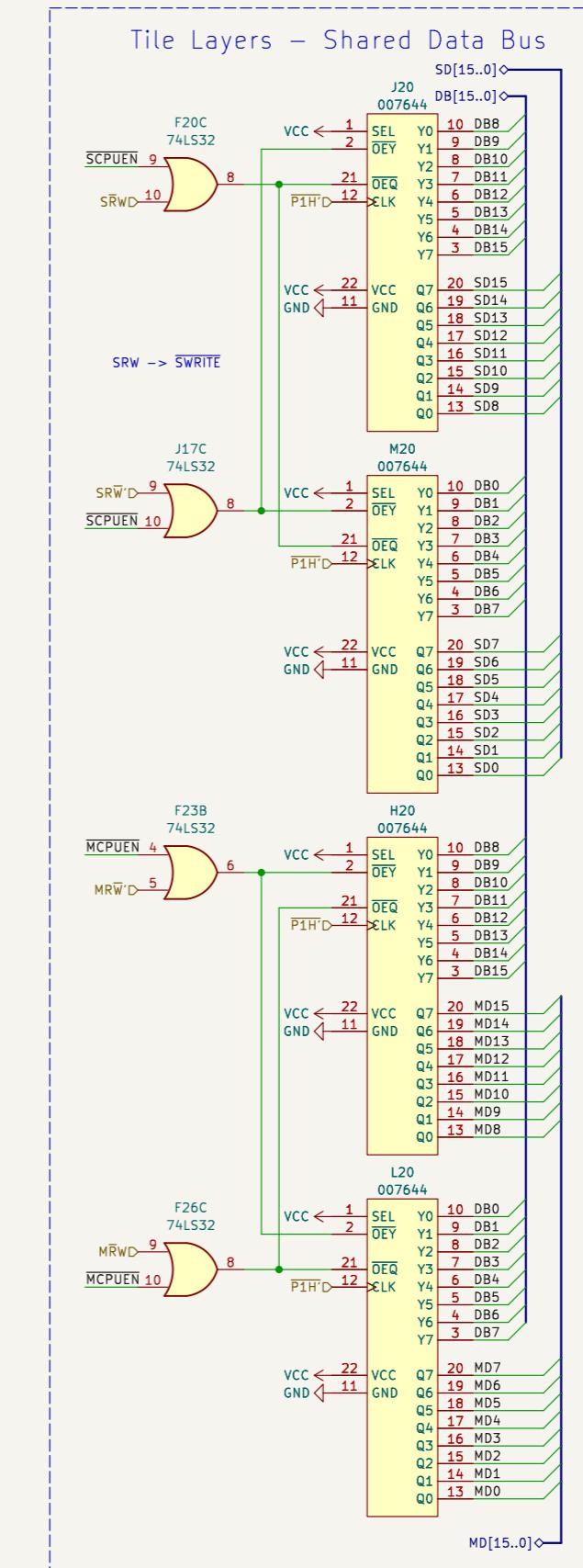
B



C



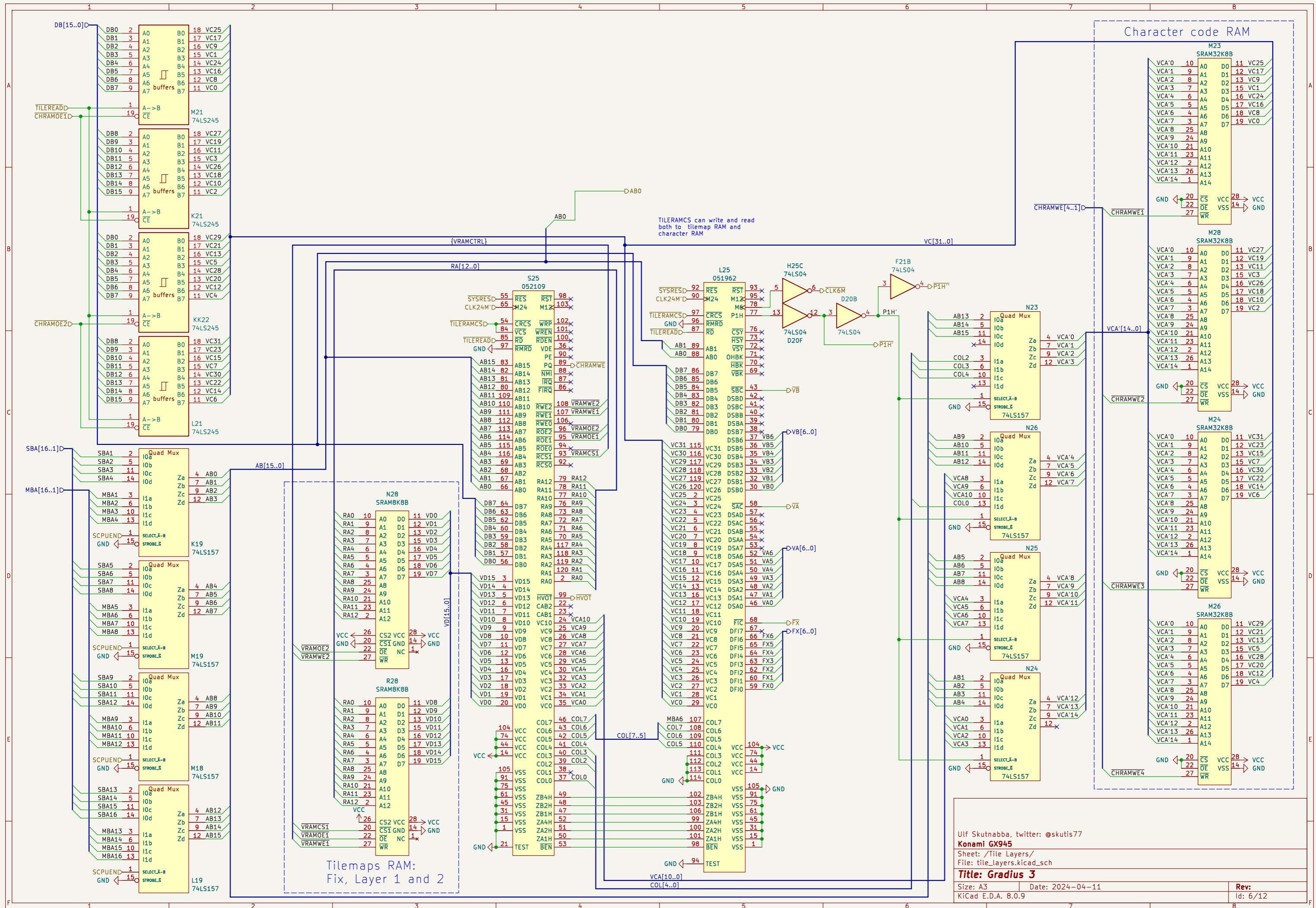
D

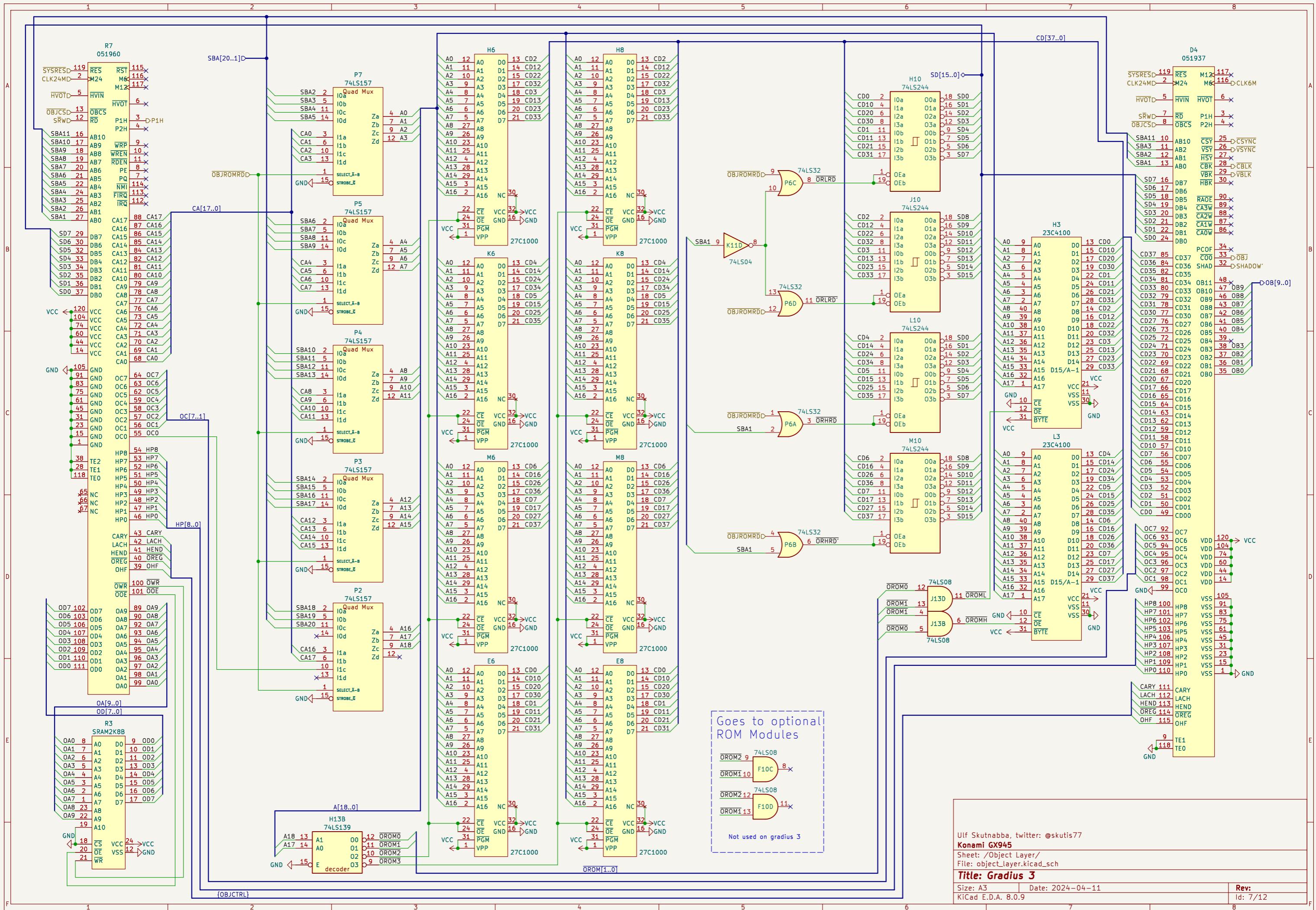


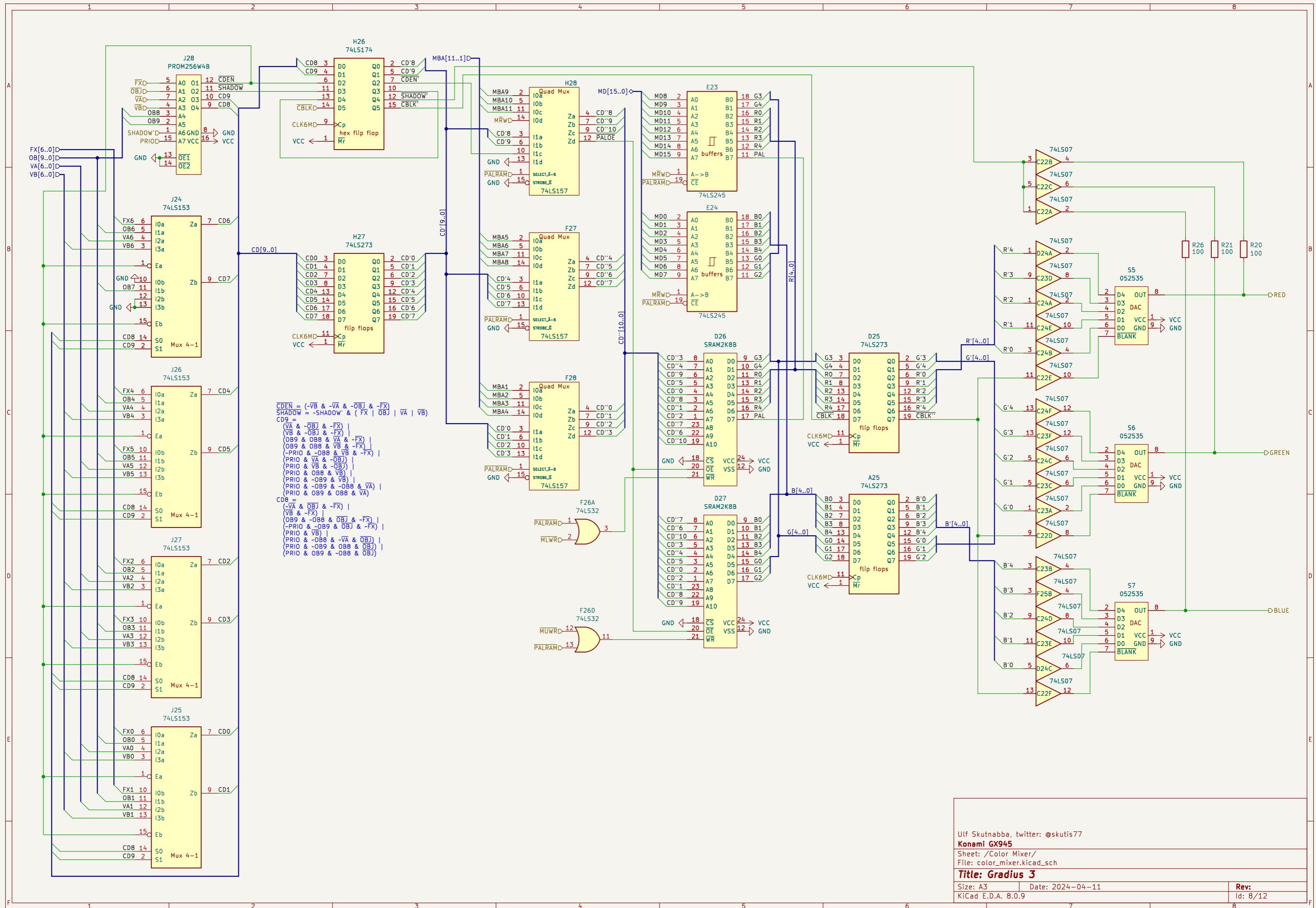
E

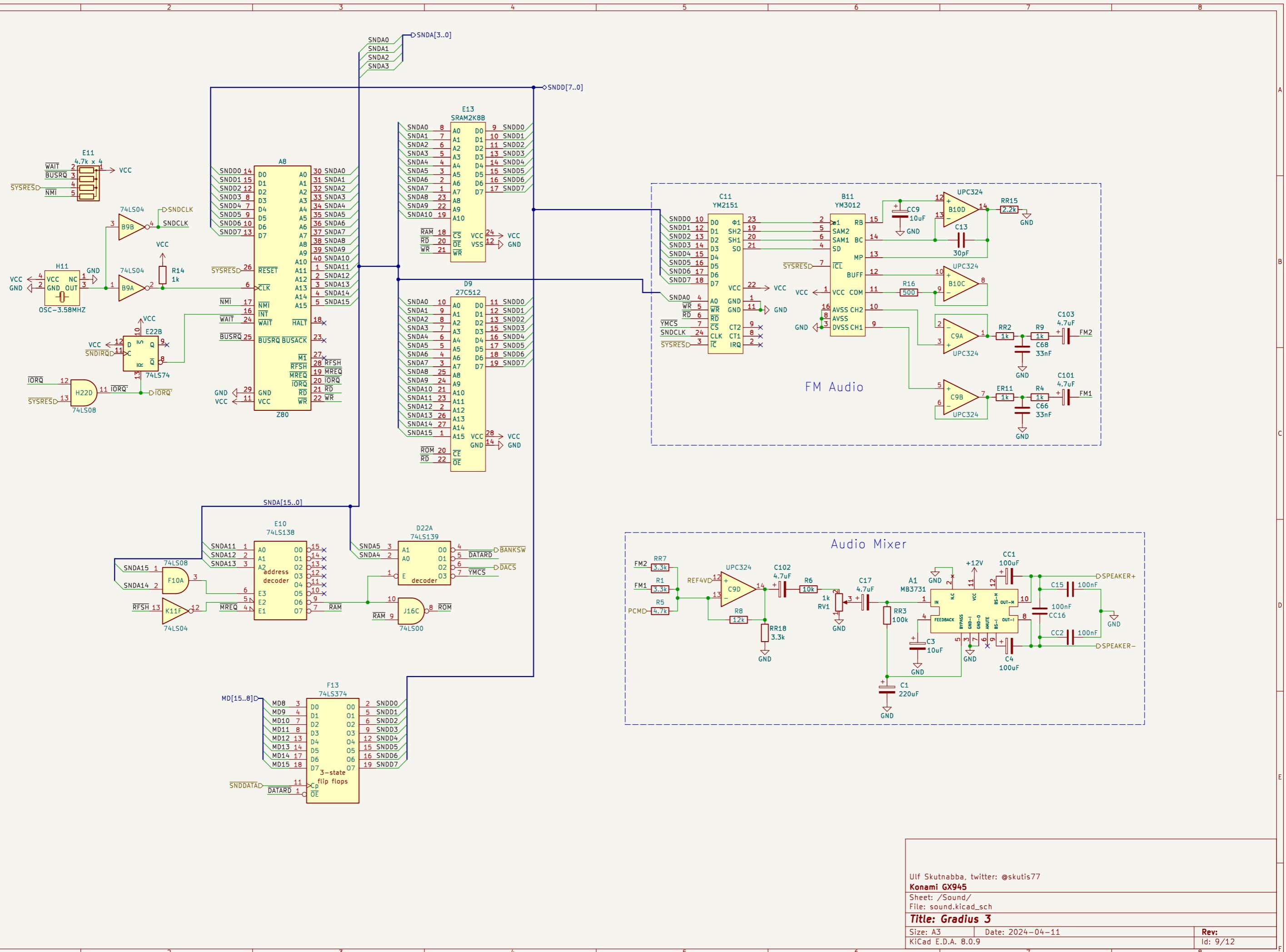
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Sheet: /Tile Logic/
File: tile_logic.kicad_sch
Title: Gradius 3
Size: A3 Date: 2024-04-11
KiCad E.D.A. 8.0.9 Rev:
Id: 5/12

F

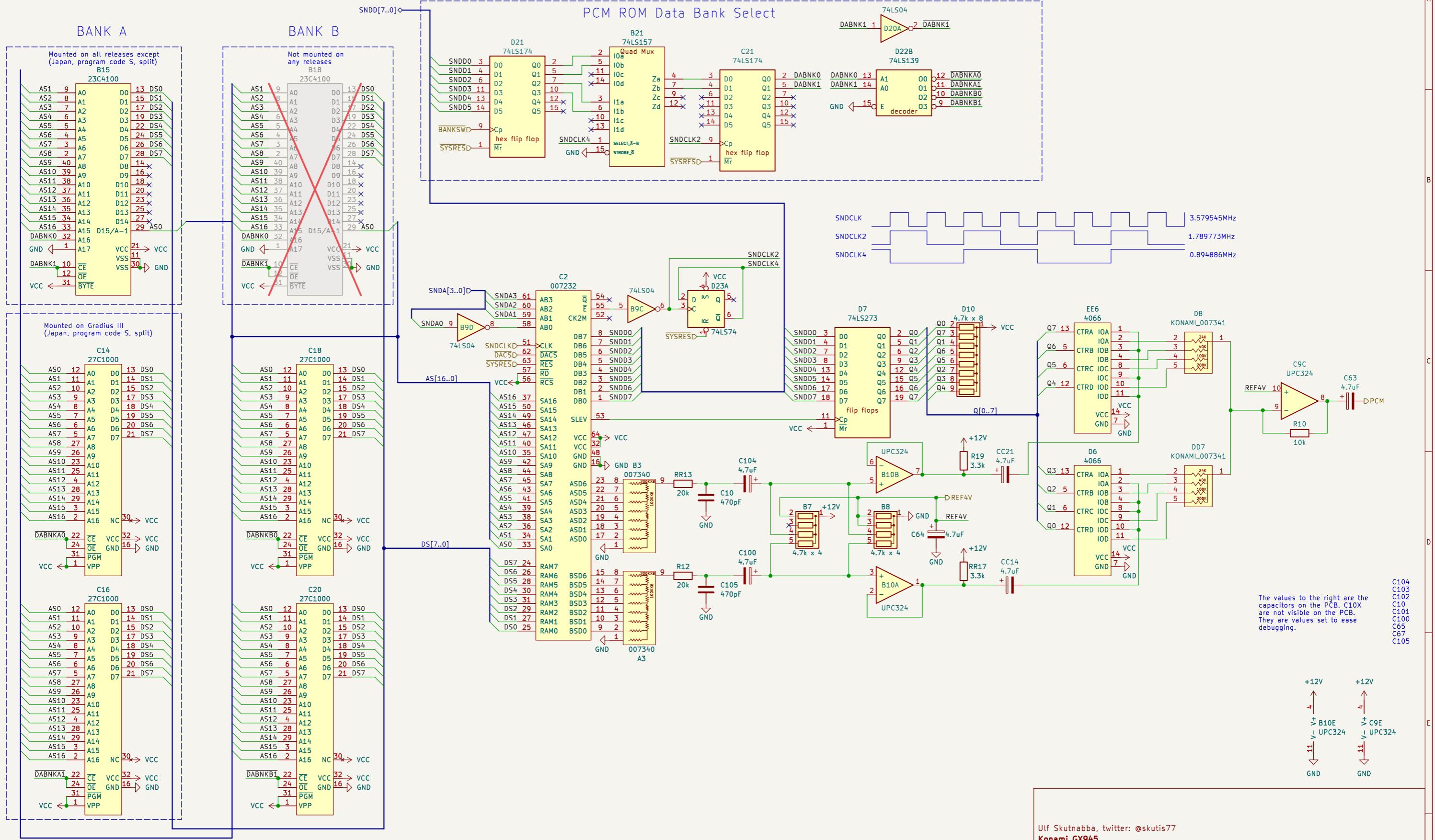








B15 and B18 do not follow the standard Mask ROM behaviour.
The BYTE mode select must be selected from factory and pin 31 is probably not connected.



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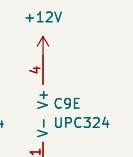
Sheet: /PCM/

File: pcm.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11

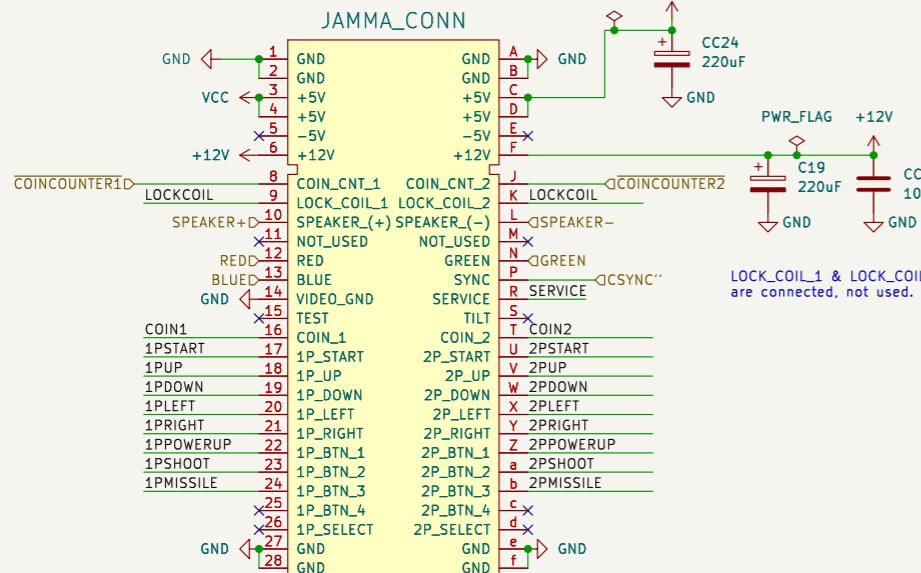
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Id: 10/12

A



PWR_FLAG VCC

PWR_FLAG +12V

LOCK_COIL_1 & LOCK_COIL_2 are connected, not used.

MD[7..0]

INPUT[19..0]

CABINPUTSD

MBA[2..1]D

RN1

RN2

RN3

RN4

RN5

C25

74LS253

SW32

INPUT9

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD1

INPUT10

INPUT11

INPUT12

INPUT13

INPUT14

INPUT15

INPUT16

INPUT17

INPUT18

INPUT19

SW31

INPUT10

I0b

I1b

I2b

I3b

4-to-1 mux

OEb

Zb

MD0

INPUT12

INPUT13

INPUT14

INPUT15

INPUT16

INPUT17

INPUT18

INPUT19

SW34

INPUT12

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD3

INPUT14

INPUT15

INPUT16

INPUT17

INPUT18

INPUT19

SW33

INPUT11

I0b

I1b

I2b

I3b

4-to-1 mux

OEb

Zb

MD2

INPUT16

INPUT17

INPUT18

INPUT19

SW32

INPUT10

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD1

INPUT18

INPUT19

INPUT10

INPUT11

INPUT12

INPUT13

INPUT14

INPUT15

SW34

INPUT11

I0b

I1b

I2b

I3b

4-to-1 mux

OEb

Zb

MD2

INPUT20

INPUT21

INPUT22

INPUT23

INPUT24

INPUT25

INPUT26

INPUT27

SW34

INPUT12

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD3

INPUT22

INPUT23

INPUT26

INPUT27

INPUT28

INPUT29

INPUT30

INPUT31

SW34

INPUT12

I0b

I1b

I2b

I3b

4-to-1 mux

OEb

Zb

MD4

INPUT24

INPUT25

INPUT28

INPUT29

INPUT30

INPUT31

INPUT32

INPUT33

SW34

INPUT12

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD5

INPUT26

INPUT27

INPUT30

INPUT31

INPUT32

INPUT33

INPUT34

INPUT35

SW34

INPUT12

I0b

I1b

I2b

I3b

4-to-1 mux

OEb

Zb

MD6

INPUT28

INPUT29

INPUT32

INPUT33

INPUT34

INPUT35

INPUT36

INPUT37

SW34

INPUT12

I0a

I1a

I2a

I3a

4-to-1 mux

OEa

Za

MD7

In the schematic symbol for LS257 the channels are in wrong order but the connections are correct.

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Sheet: /10/
File: io.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11

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Rev:

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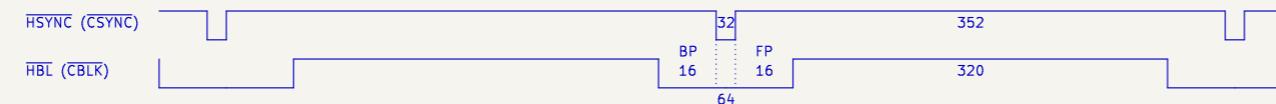
Horizontal and vertical synch timing diagrams

The pixel clock is derived from the 24MHz oscillator.
Pixel clock OVCK: $f = 24\text{MHz} / 4 = 6\text{MHz}$

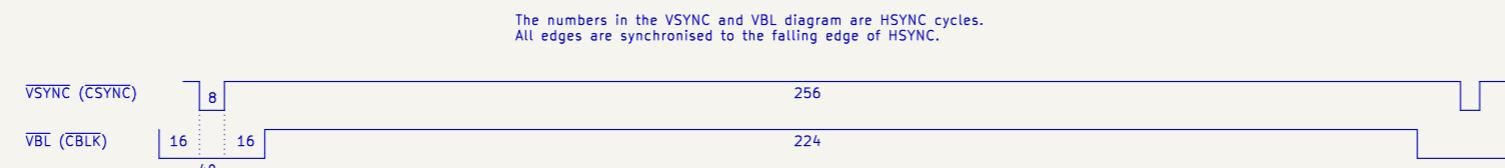
The numbers in the HSYNC and HBL diagram are pixel clock cycles.
All edges are synchronised to the rising edge of the pixel clock.

The signals have been measured at the output of the
graphic chips.

If horizontal blanking is measured at the RGB DACs, the blanking
is delayed 2 pixel clocks relative to composite sync. This
gives BP = 14 and FP = 18.



HSYNC and HBL
Frequency $f = 6\text{MHz} / 384 = 15.625\text{kHz}$.
Period $T = 1/f = 64\text{us}$.



VSYNC and VBL:
Frequency $f = 15.625\text{kHz} / 264 = 59.1856\text{Hz}$
Period $T = 1/f = 1 / 59.1856\text{Hz} = 16.896\text{ms}$

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Sheet: /Misc/

File: misc.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11

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Rev:

Id: 12/12