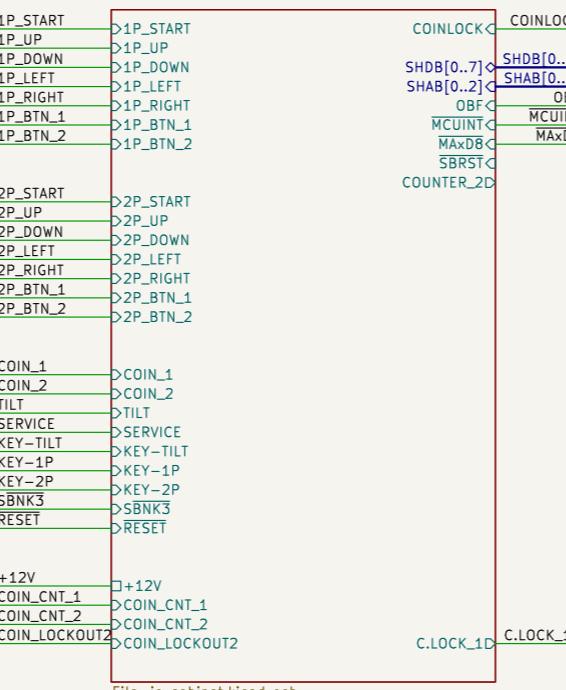
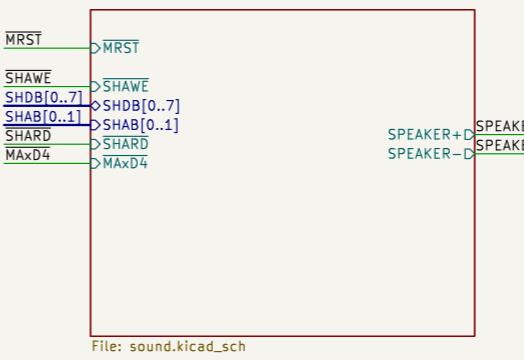


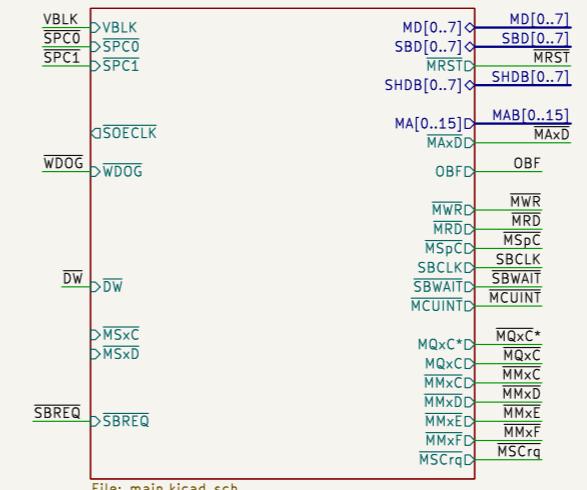
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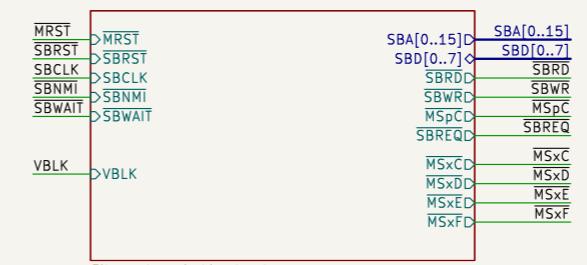
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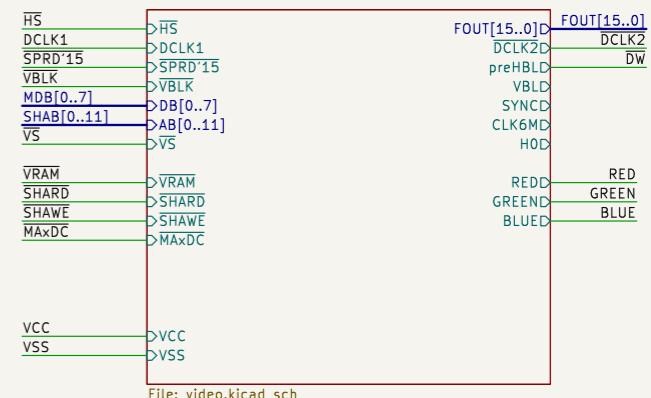
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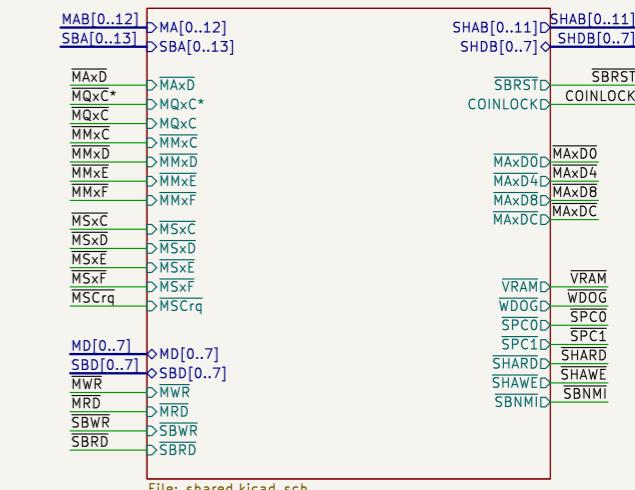
## Sub



## Video



## Shared



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Sheet: /  
File: fairyland.kicad\_sch

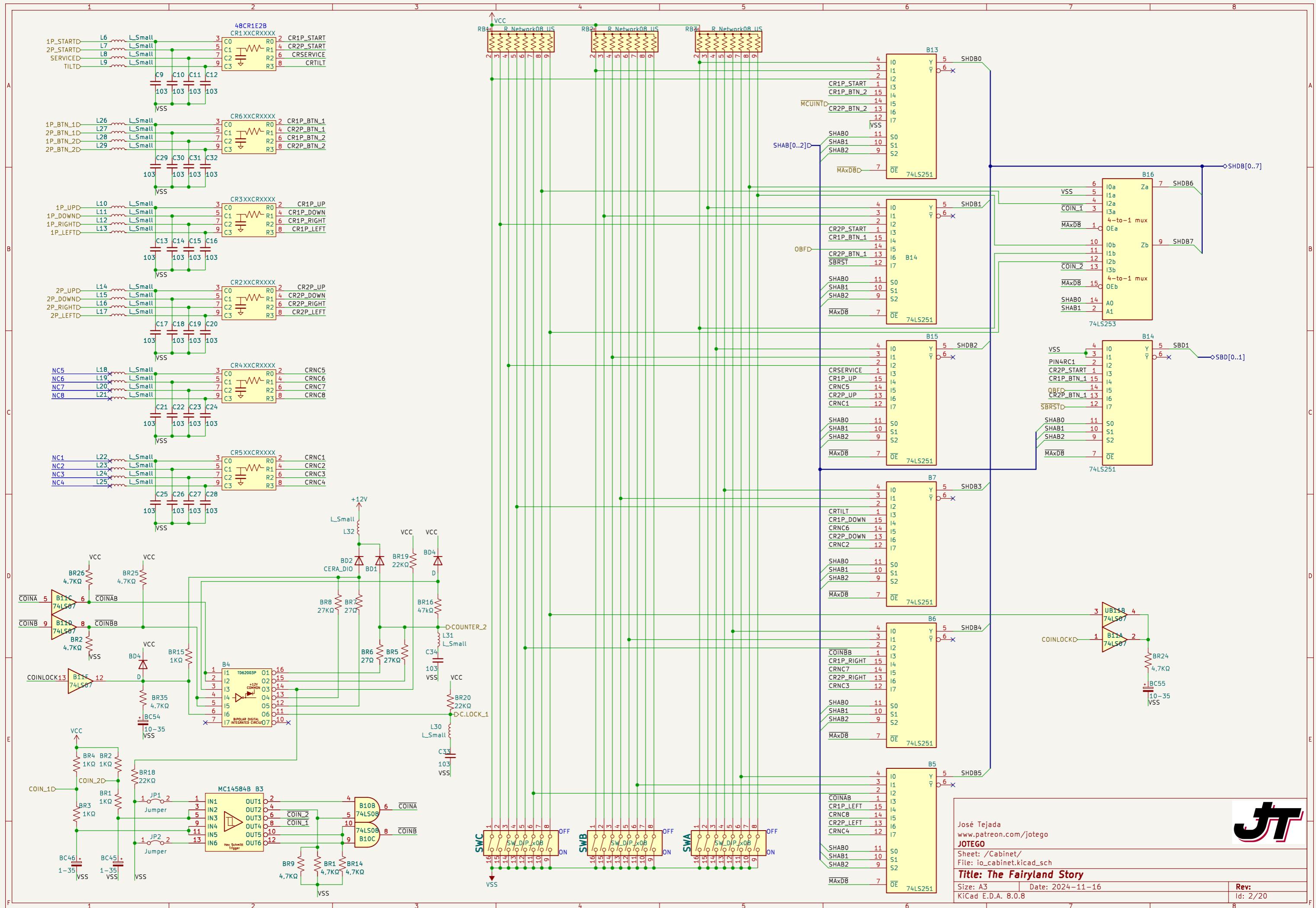
**Title: The Fairyland Story**

Size: A3 Date: 2024-11-16  
KiCad E.D.A. 8.0.8



File: capacitors\_lu.kicad\_sch

Rev: 1/10



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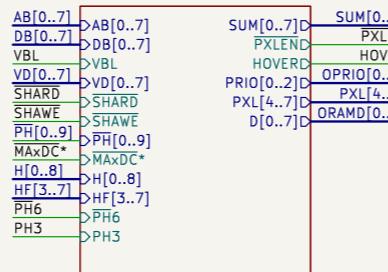
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E

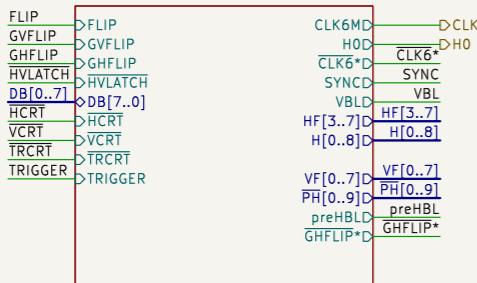
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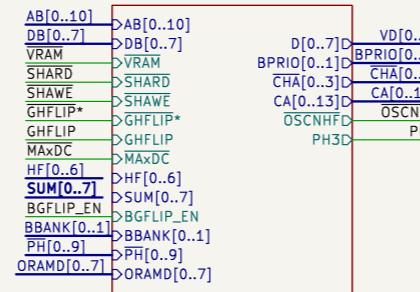
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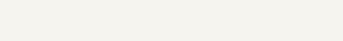
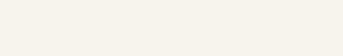
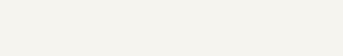
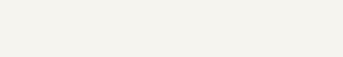
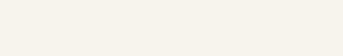
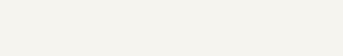
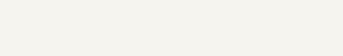
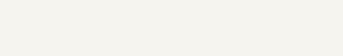
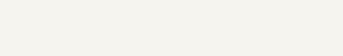
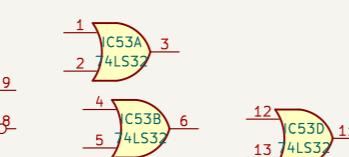
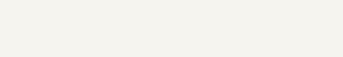
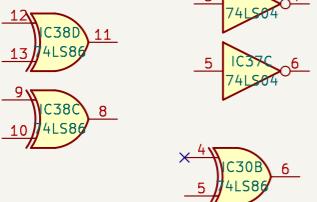
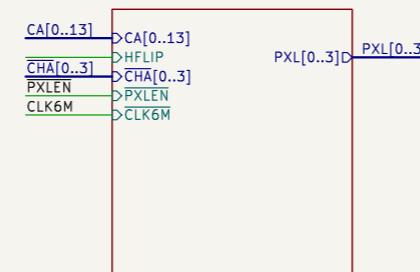
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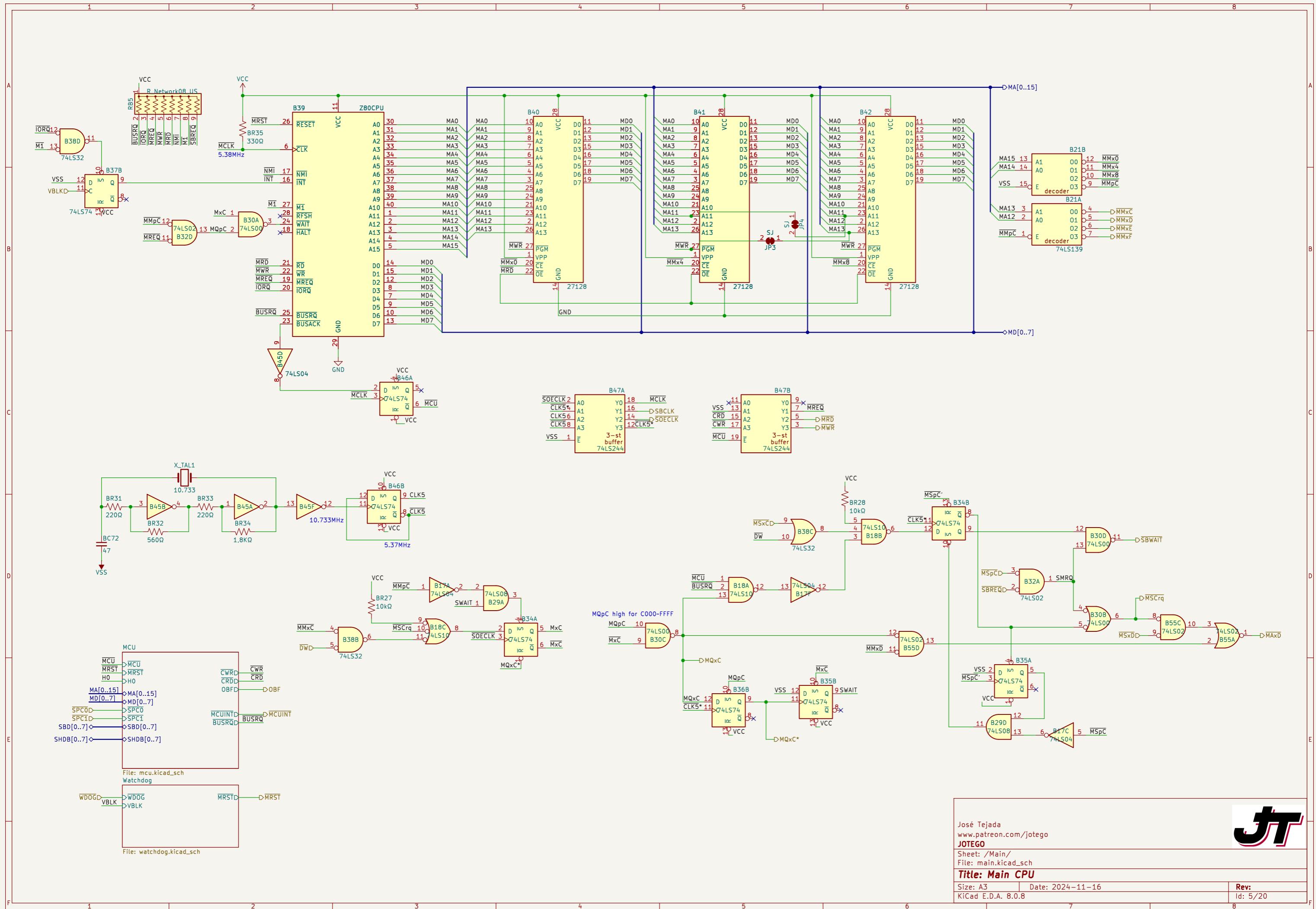


### Video RAM



### Tile ROM





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File: main.kicad\_sch

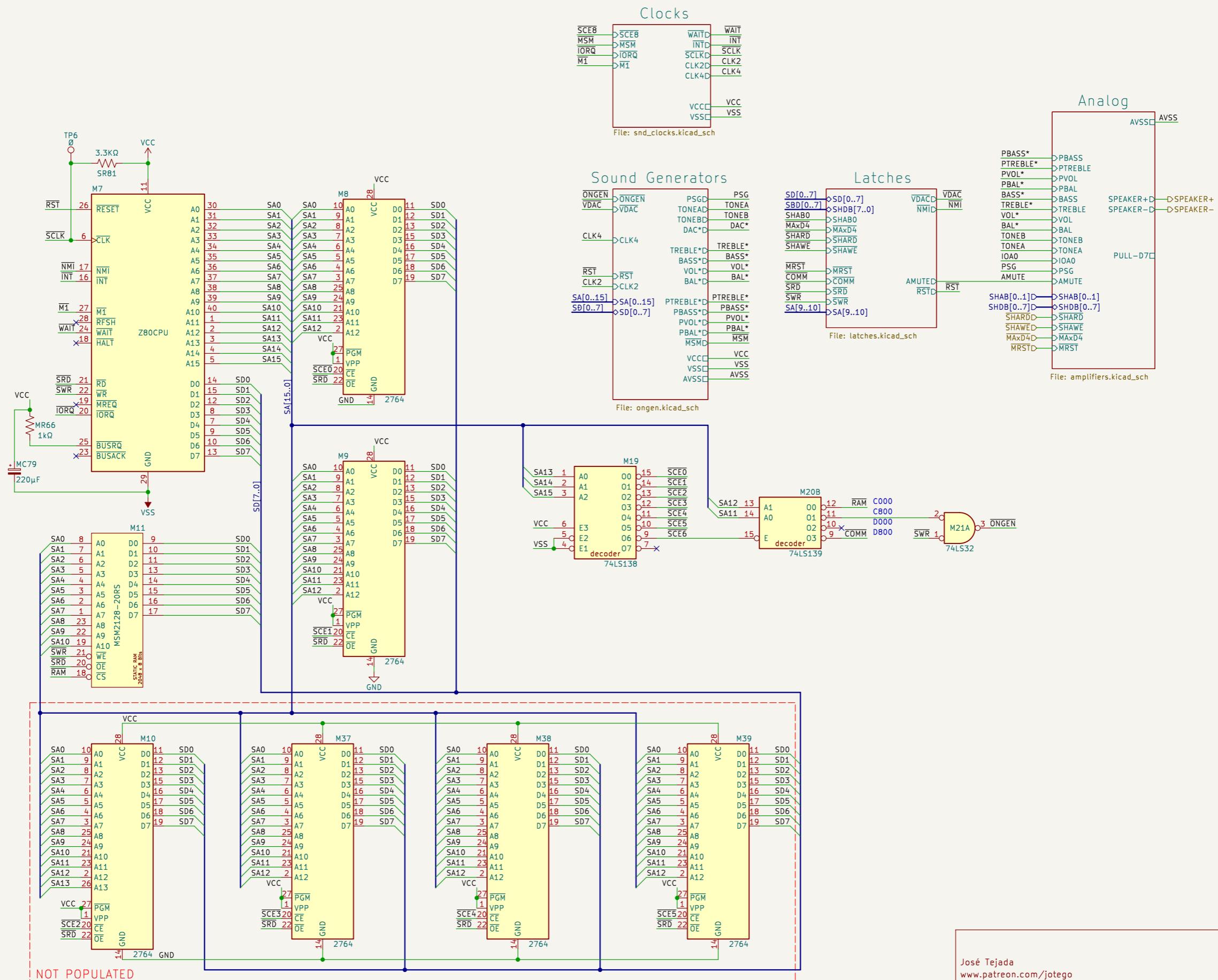
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Size: A3 | Date: 2024-11-16

KiCad E.D.A. 8.0.8



Rev: 5/20

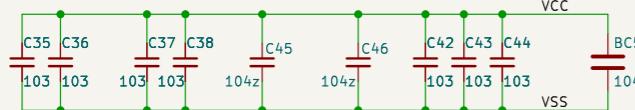
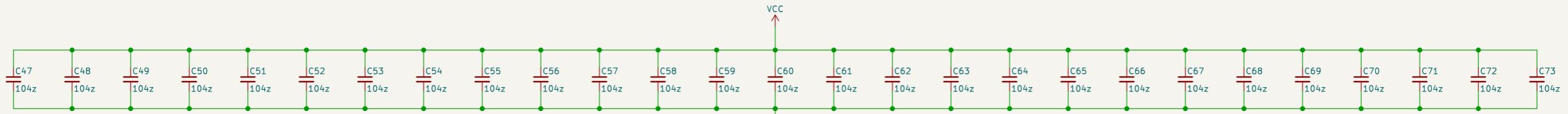


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Sheet: /Sound/  
File: sound.kicad\_sch

## Title: Sound Board

Size: A3 Date: 2024-11-16  
KiCad E.D.A. 8.0.8



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+ M22C 74LS74	+ M23E 74LS08	+ M22C 74LS74	+ M22C 74LS74	+ IC53E 74LS32	+ M20C 74LS139	+ decoder	+ M18C 74LS139	+ decoder	+ IC15E 74LS08	+ decoder	+ IC20C 74LS139	+ decoder	+ IC40C 74LS20	+ IC96E 74LS08	+ IC37G 74LS04	+ IC1G 74LS04	+ IC68E 74LS08	+ IC2C 74LS107	+ IC39E 74LS86	+ IC38E 74LS86	+ IC24C 74LS86	+ IC14C 74LS74	+ IC5C 74LS74	+ IC25D 74LS10	+ IC29G 74LS04	+ IC30E 74LS86	+ IC6E 74LS86	+ IC6E 74LS86	M6E MC3301P
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The circuit diagram illustrates a logic design using the following components:

- IC16E 74LS02**: A dual AND gate (B55B) with inputs 5 and 6, and output 4.
- IC26E 74LS86**: A dual OR gate (B45C) with inputs 5 and 6, and output 6.
- 74LS04**: An inverter (B17B) with input 3 and output 4.
- 74LS139**: A 4-to-16 decoder (A1-A3) with inputs A0, A1, A2, and A3. It has 16 outputs labeled 00 through 15. The output 03 is labeled "decoder".
- M24P**: A 74LS04 inverter chip, which is noted as "NOT POPULATED".

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Sheet: /capacitors\_lu/  
File: capacitors\_lu.kicad\_sch

## Title: The Fairyland Story

Size: A3 Date: 2024-11-16

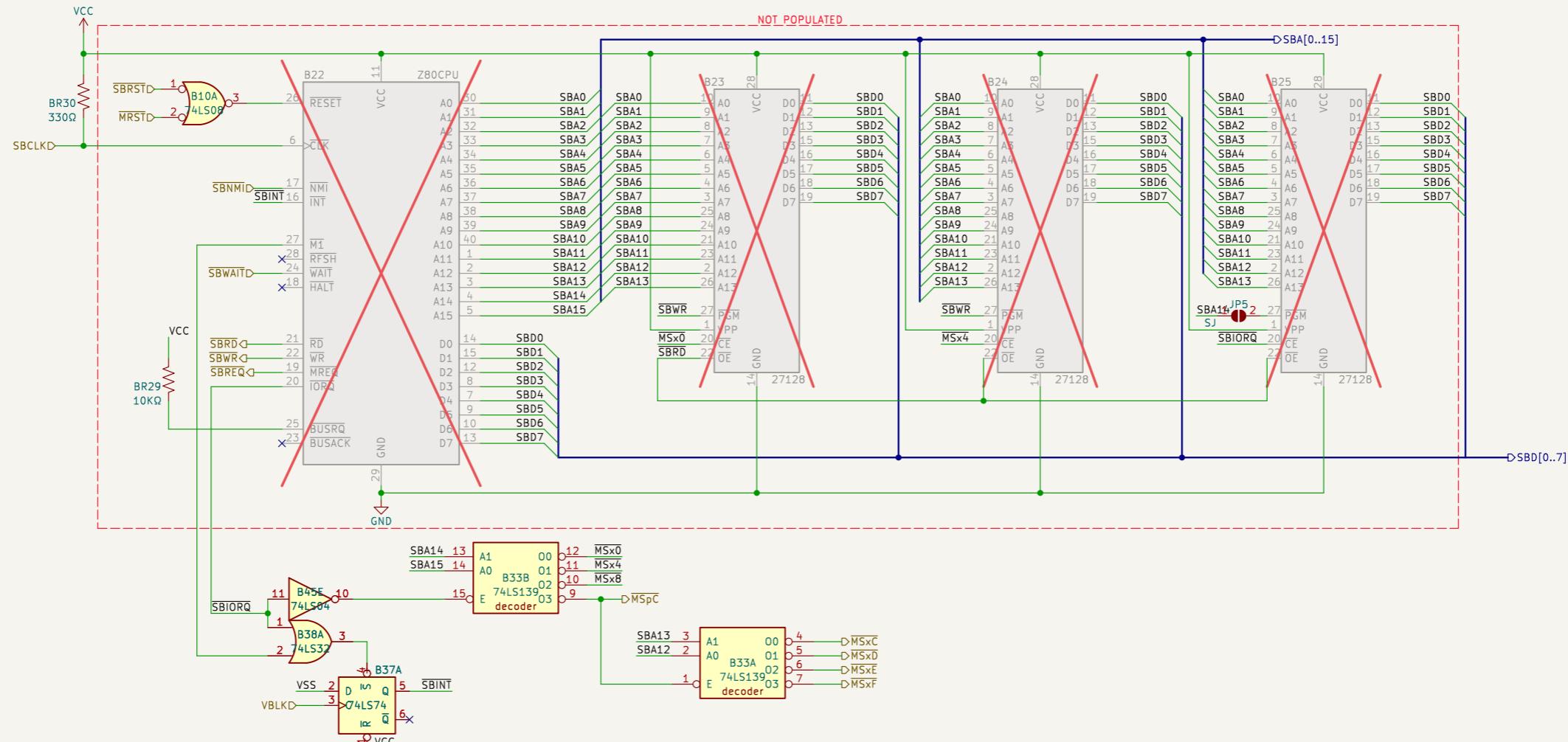
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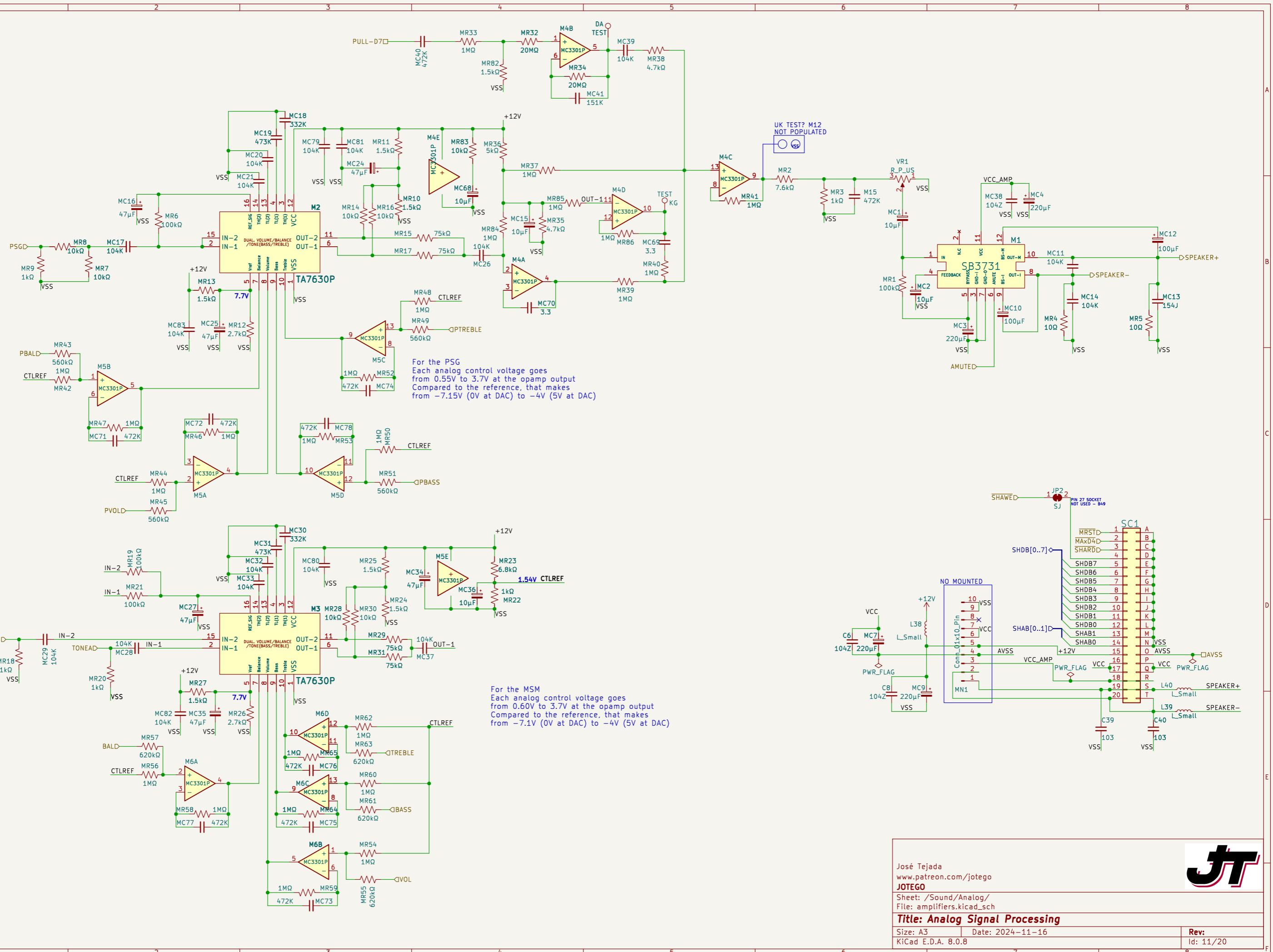


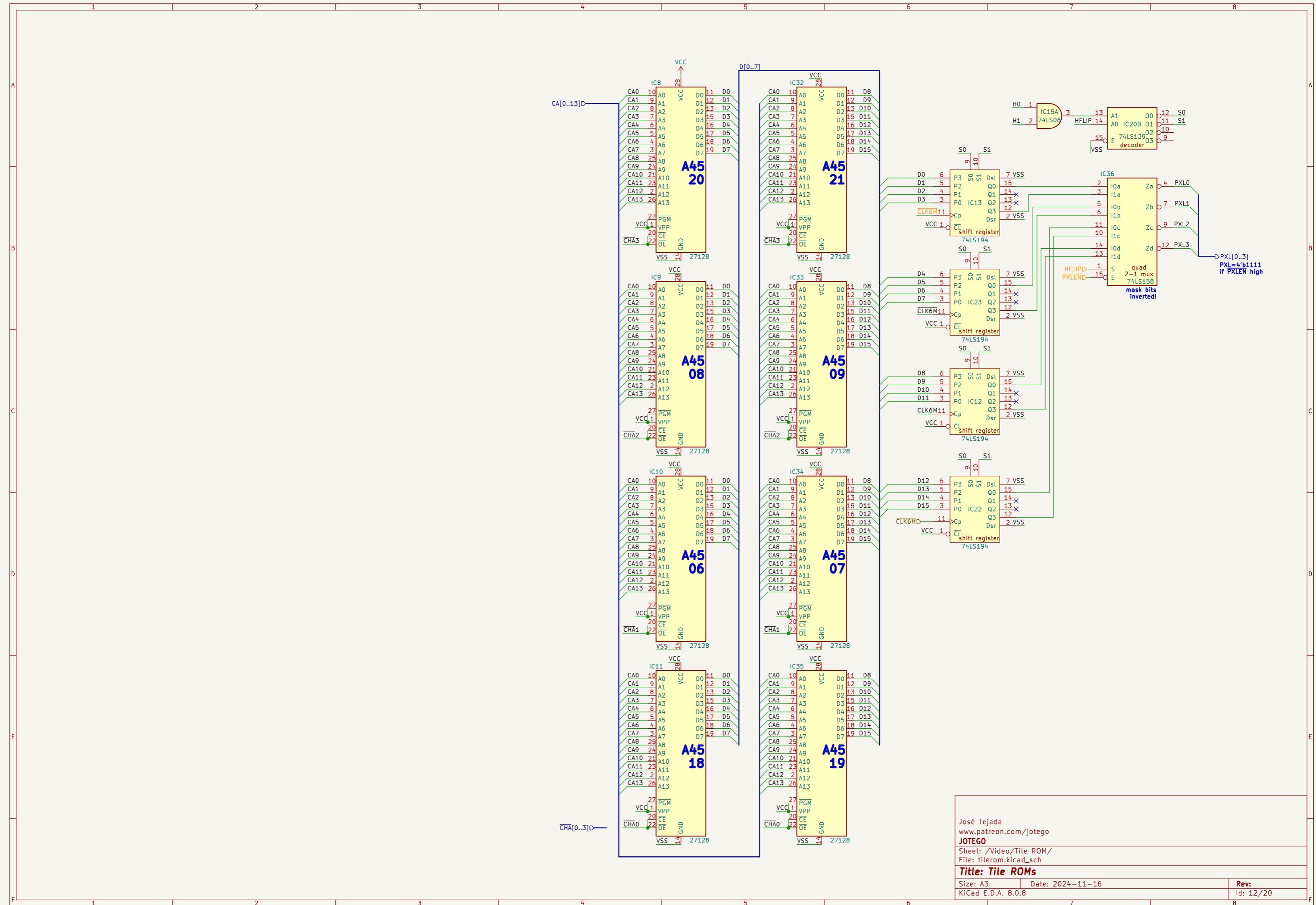
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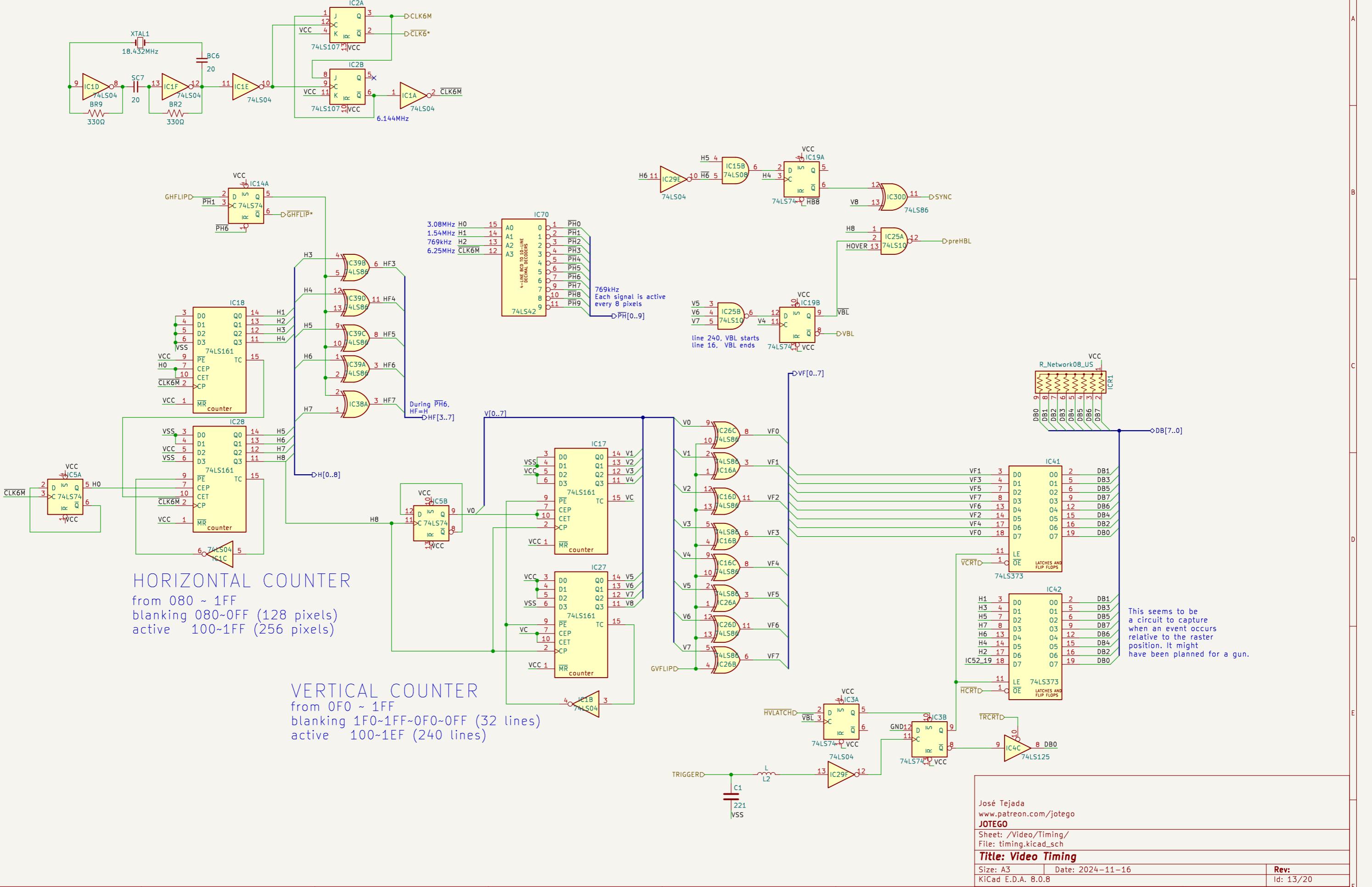
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**Title: Subsidiary CPU**

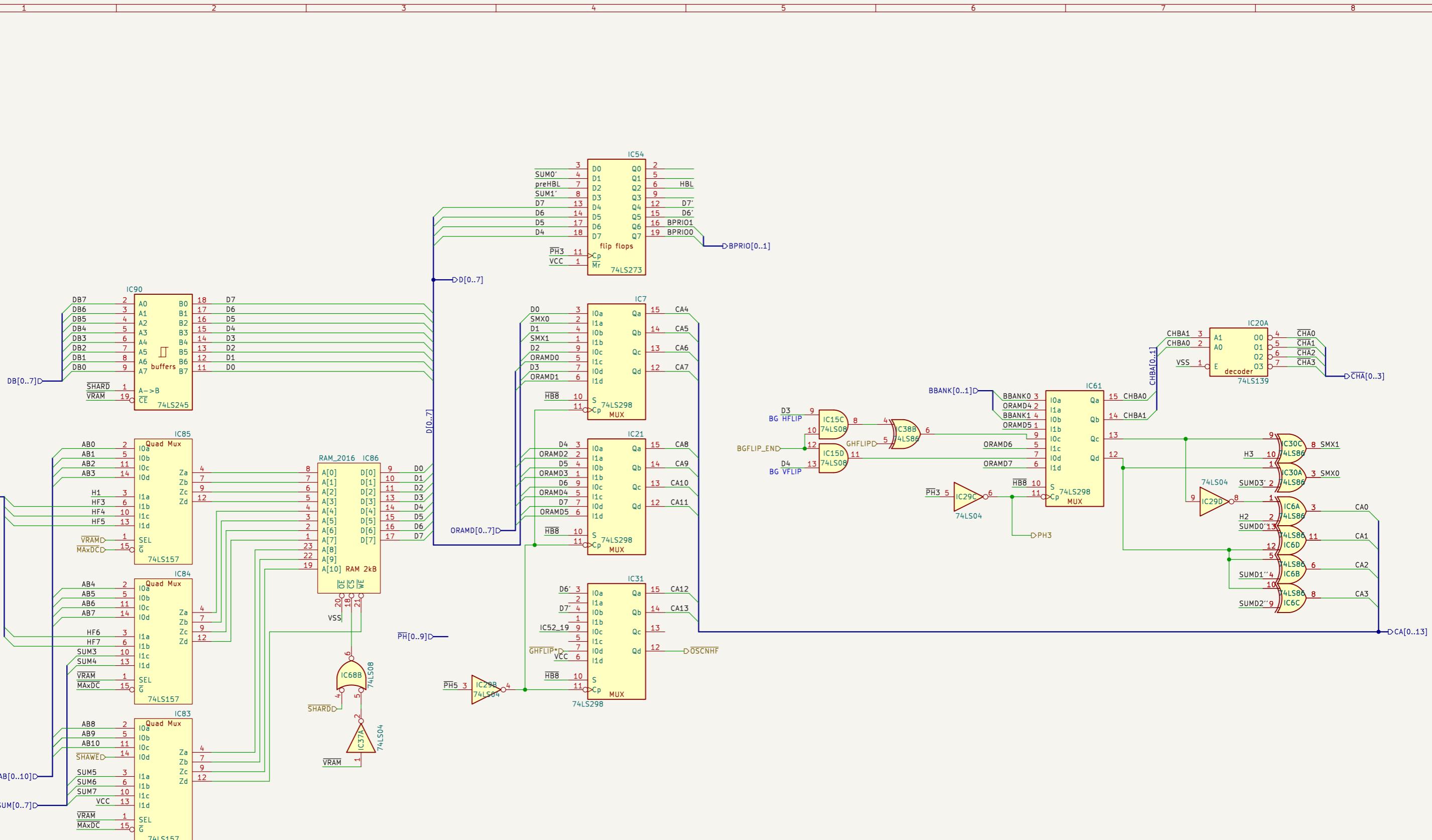
Size: A3 | Date: 2024-11-16  
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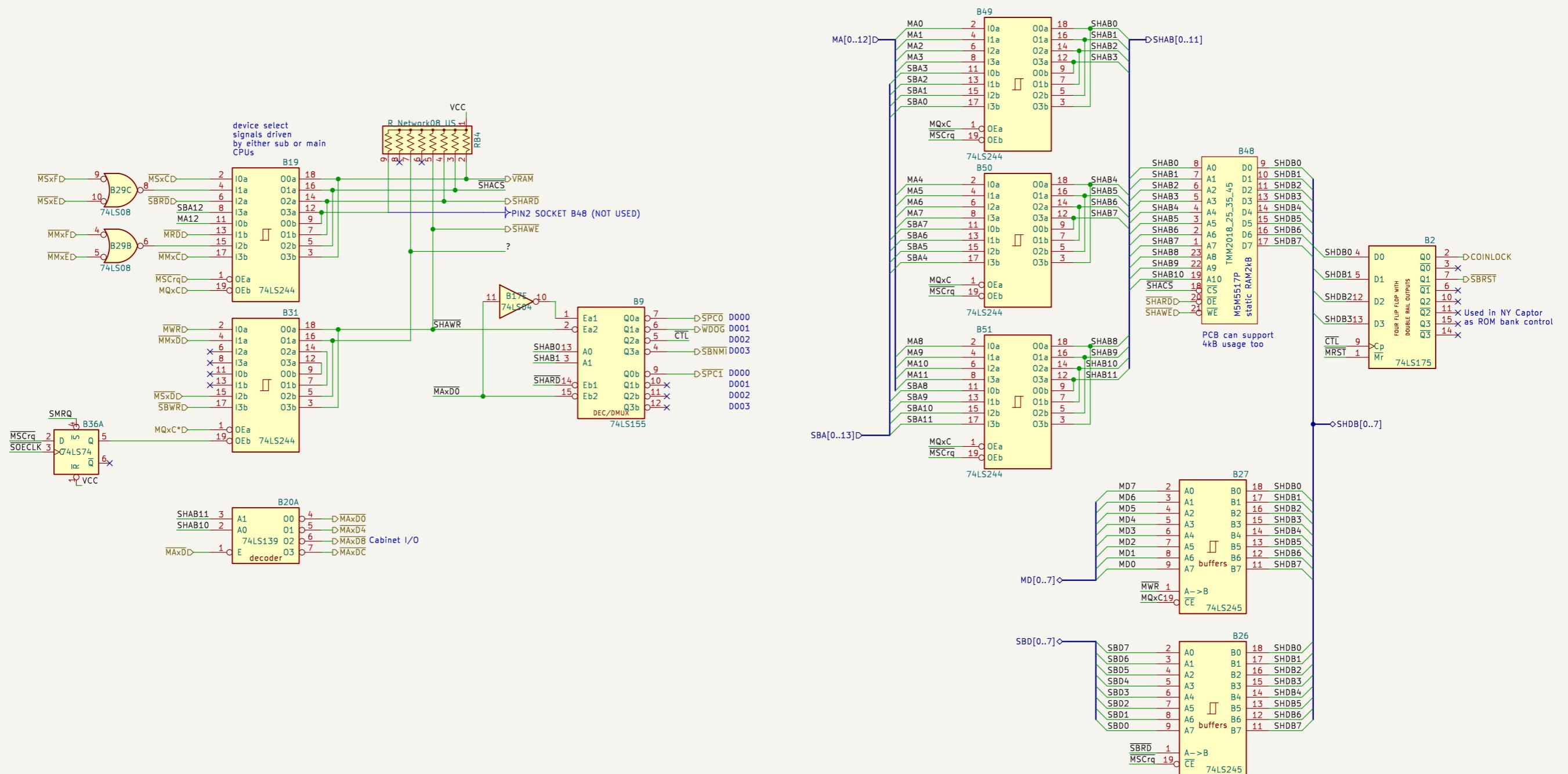
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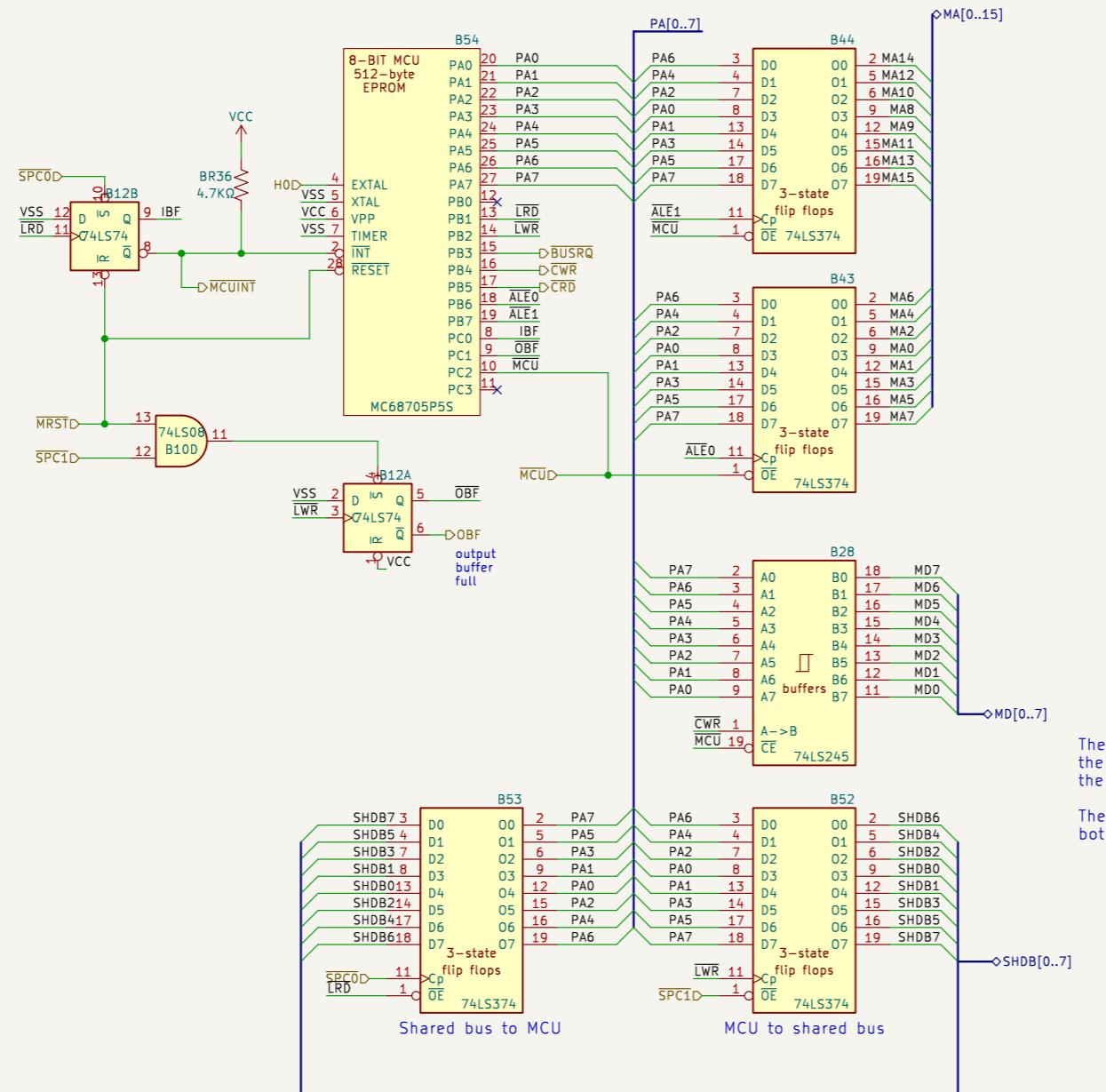
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File: vram.kicad\_sch

**Title: Background Video RAM**

Size: A3 | Date: 2024-11-16  
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Rev: 13/20





The MCU can take control of the share bus by requesting the main CPU bus

The MCU can communicate with both CPUs via latches B52 and B53

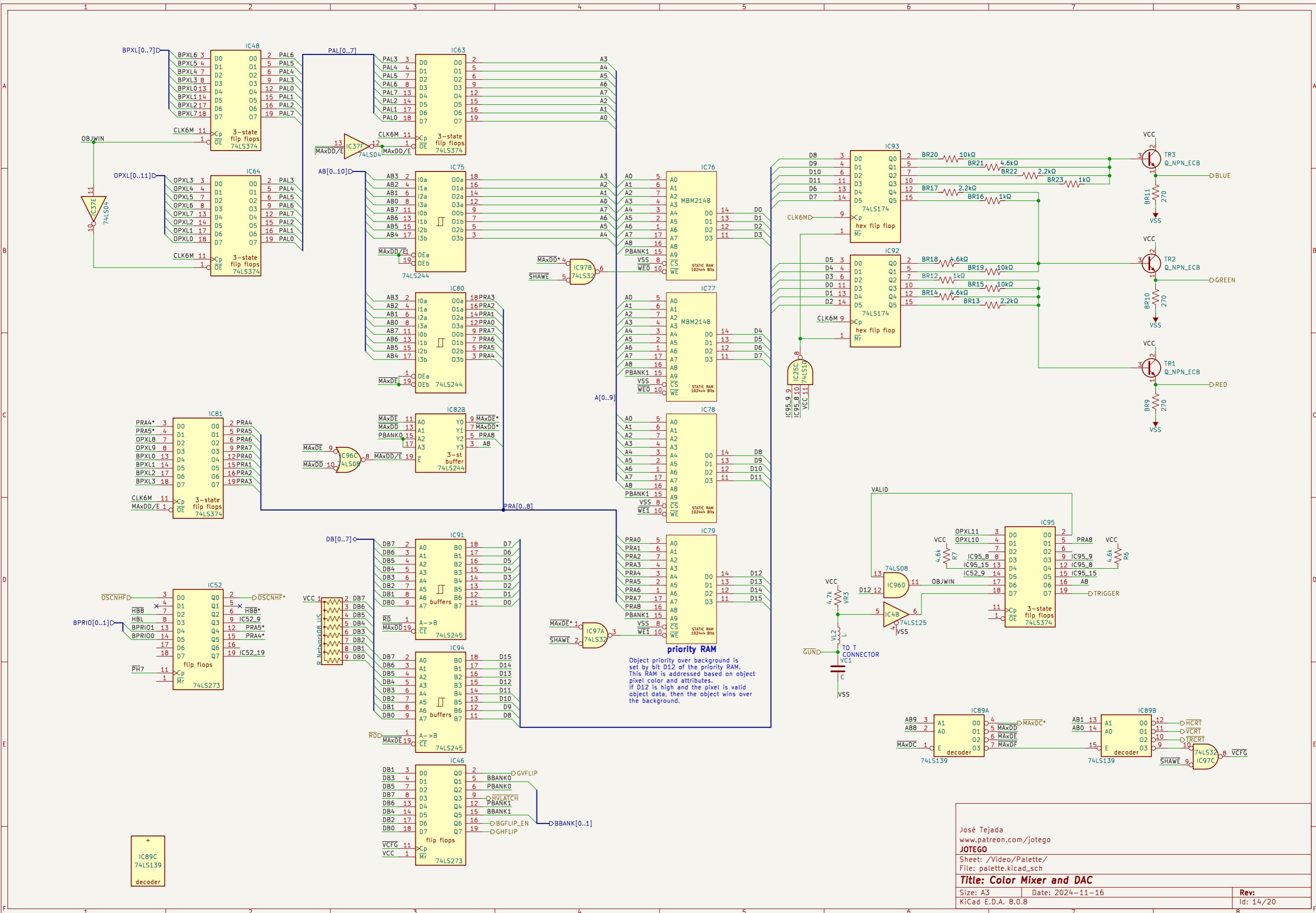
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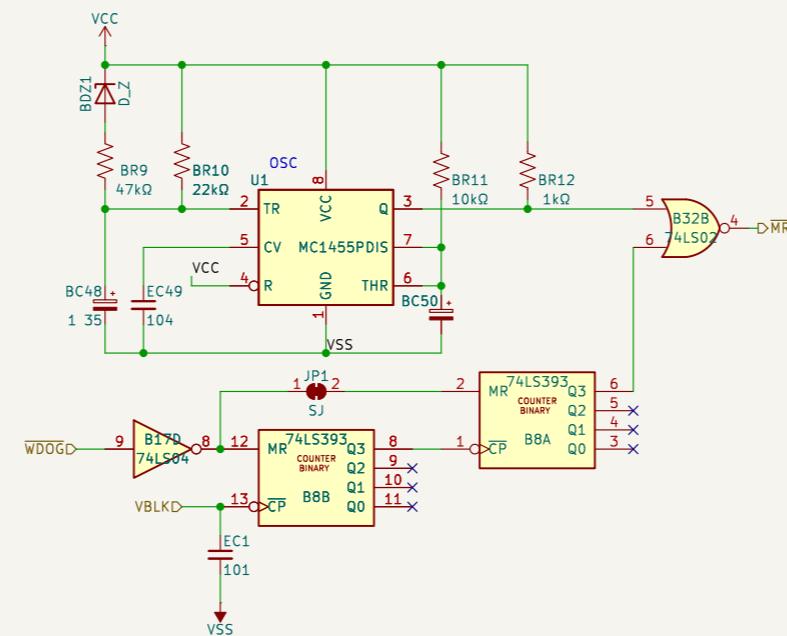
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File: mcu.kicad\_sch

**Title: MCU**

Size: A3 Date: 2024-11-16  
KiCad E.D.A. 8.0.8

Rev: Id: 14/20





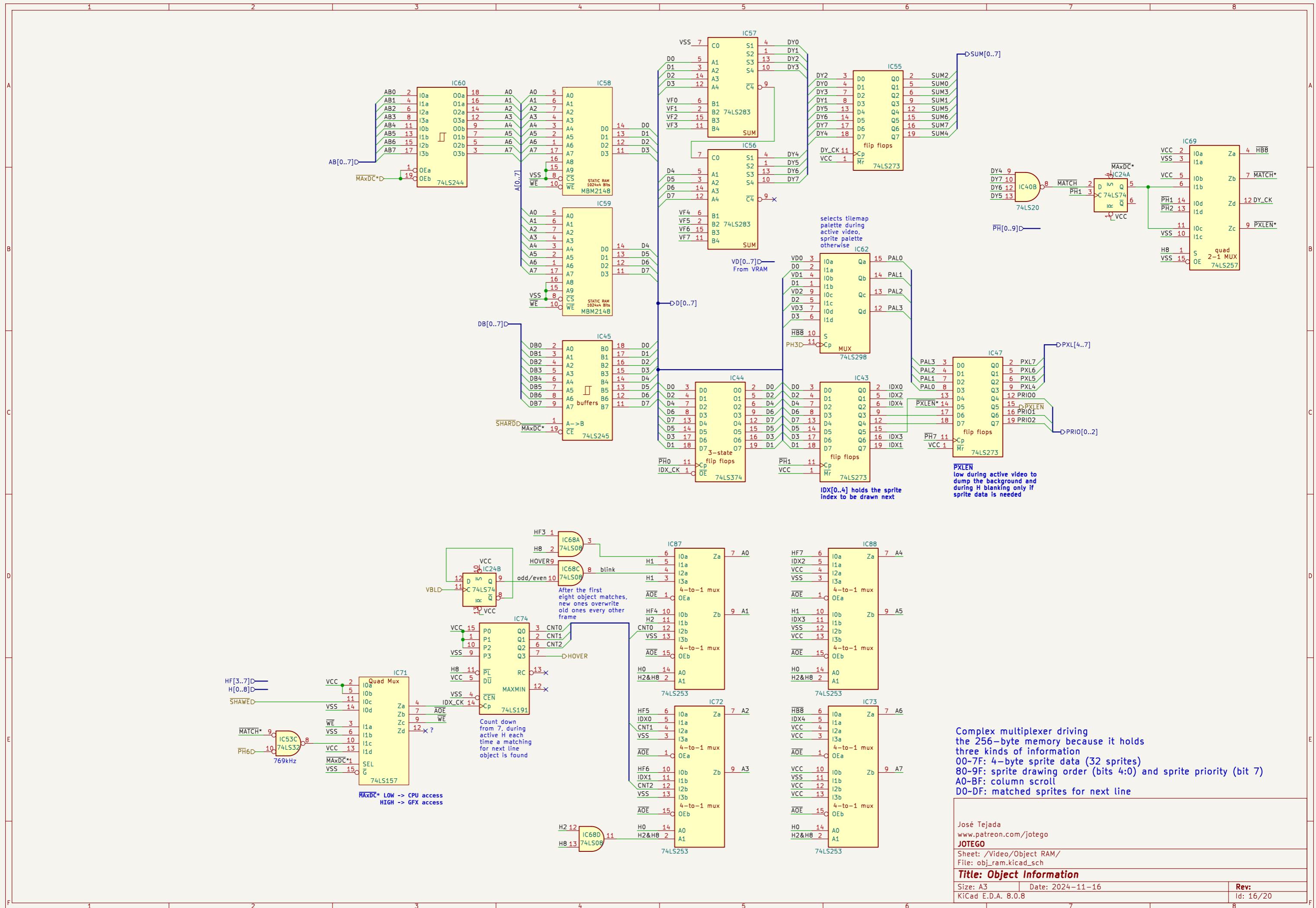
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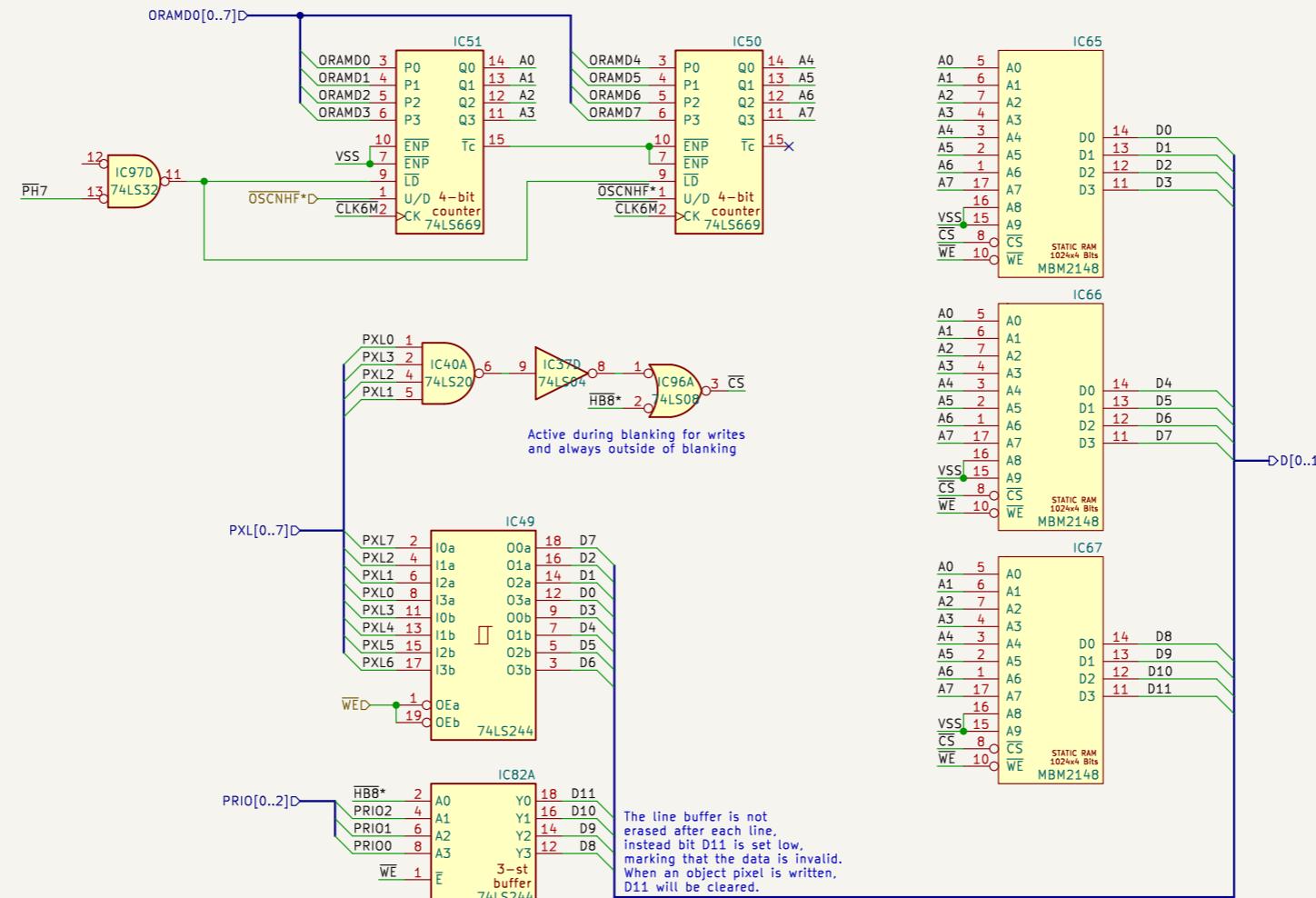
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File: watchdog.kicad\_sch

**Title:**

Size: A3 Date: 2024-11-16  
KiCad E.D.A. 8.0.8

**Rev:**  
Id: 15/20





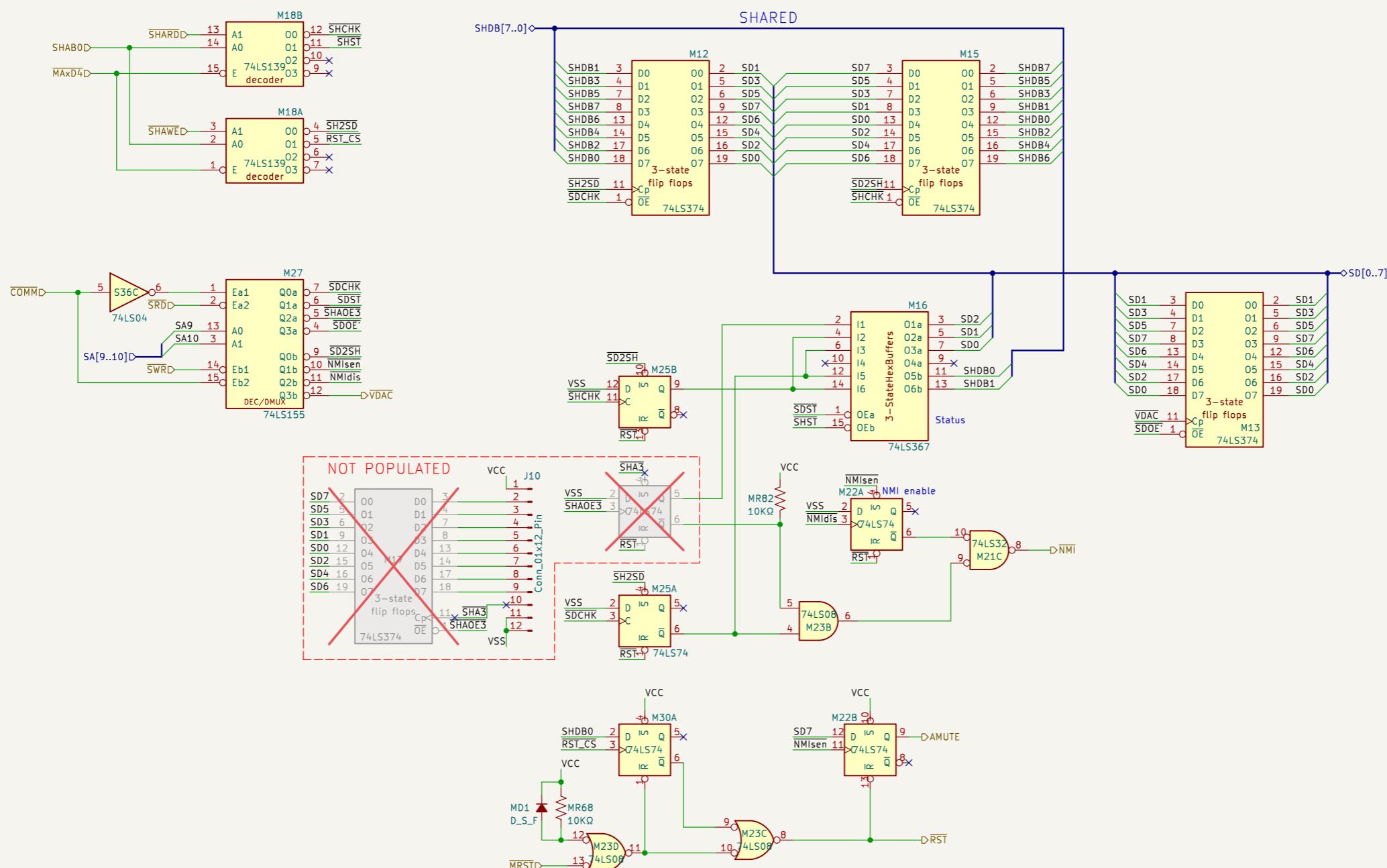
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**JOTEGO**

Sheet: /Video/Line buffer/  
File: linebuf.kicad\_sch

**Title: Single Line Video Buffer**

Size: A3	Date: 2024-11-16
KiCad E.D.A. 8.0.8	Rev:

Id: 17/20	F
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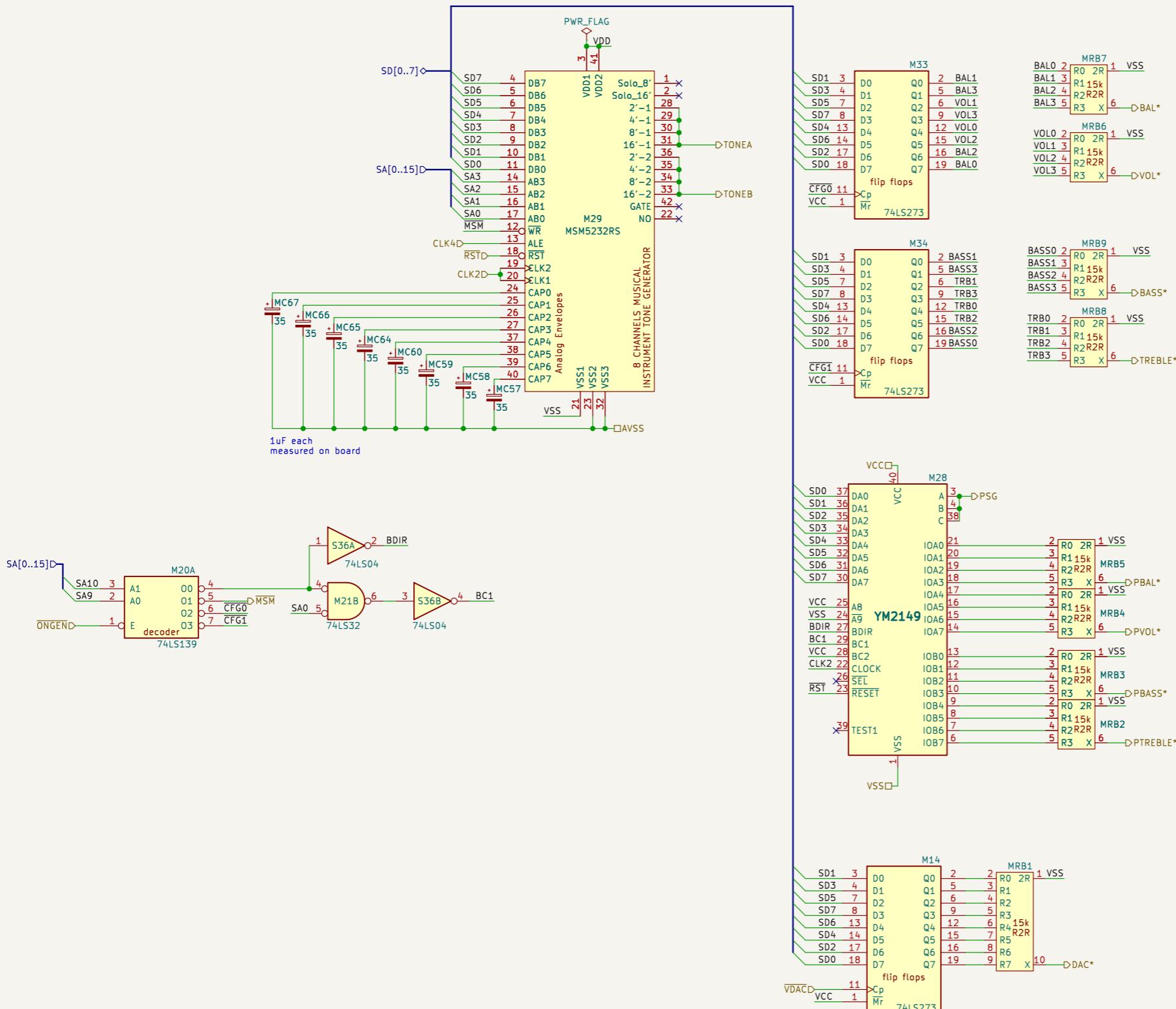
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Sheet: /Sound/Latches/  
File: latches.kicad\_sch

## Title: Communication Latches

Size: A3 Date: 2024-11-16  
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## JOTEGO

## Title: Sound Generators

Size: A3 Date: 2024

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KIUG E.D.W. 0.0.0

For more information about the study, please contact Dr. John Smith at (555) 123-4567 or via email at [john.smith@researchinstitute.org](mailto:john.smith@researchinstitute.org).

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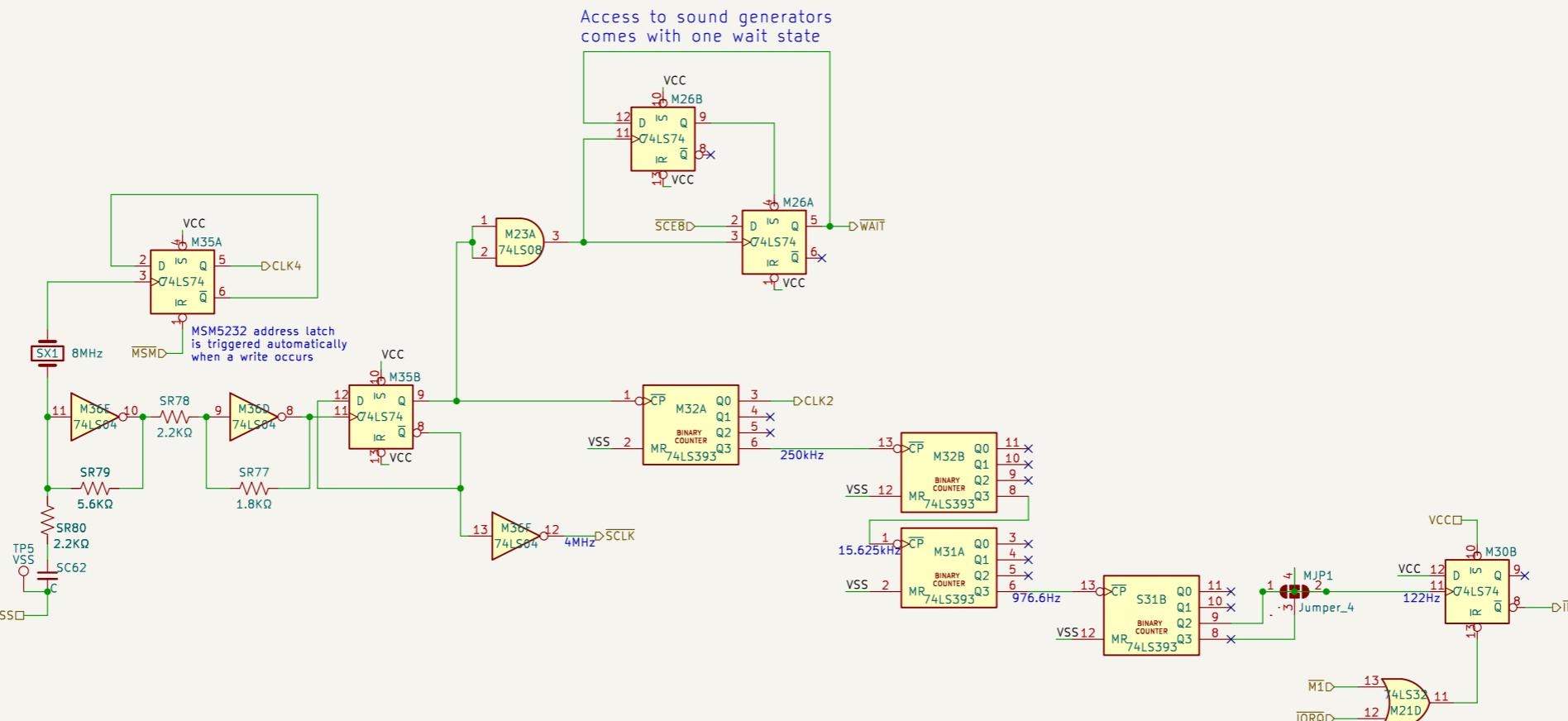
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Sheet: /Sound/Clocks/  
File: snd\_clocks.kicad\_sch

**Title: Sound Clock Generation**

Size: A3 Date: 2024-11-16  
KiCad E.D.A. 8.0.8

Rev:  
Id: 20/20