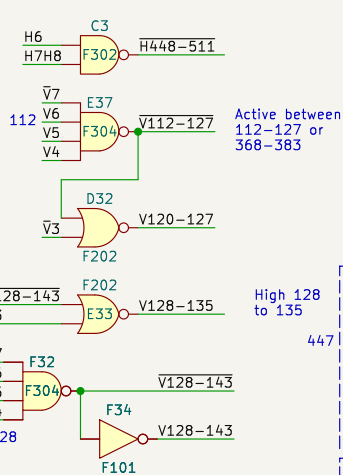
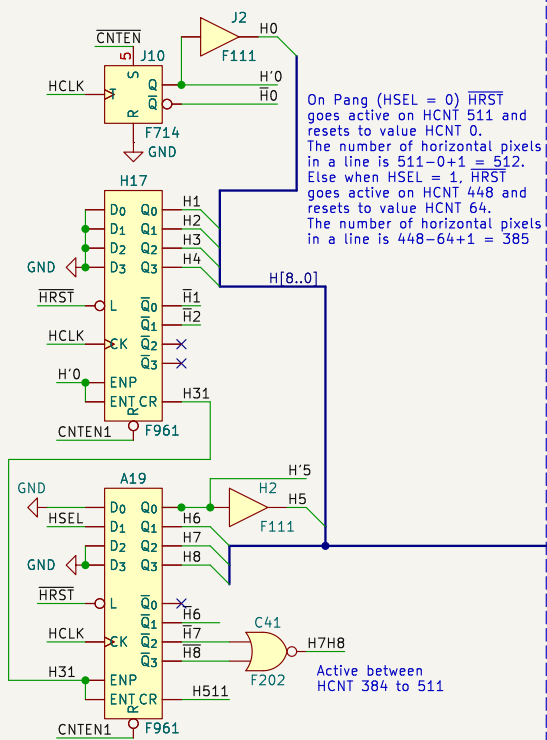
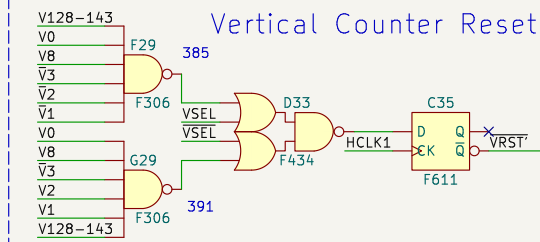


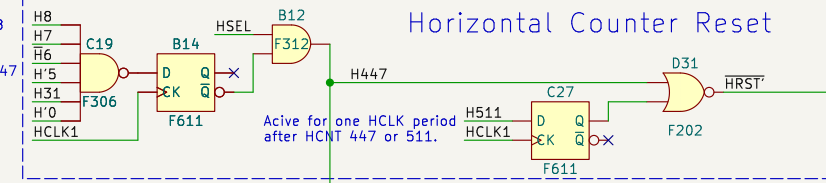
## Horizontal Counter



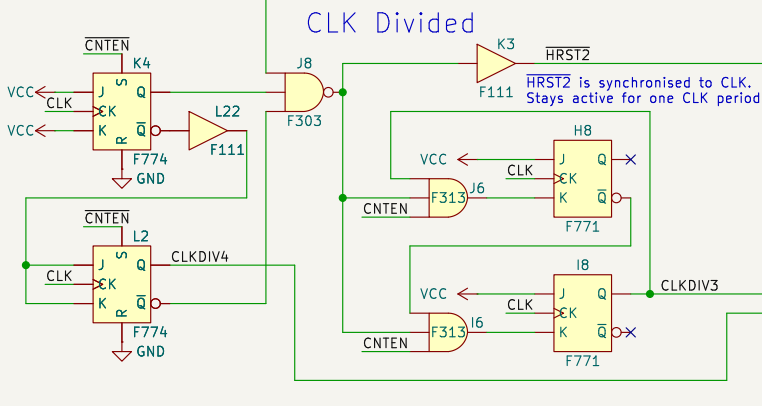
## Vertical Counter Reset



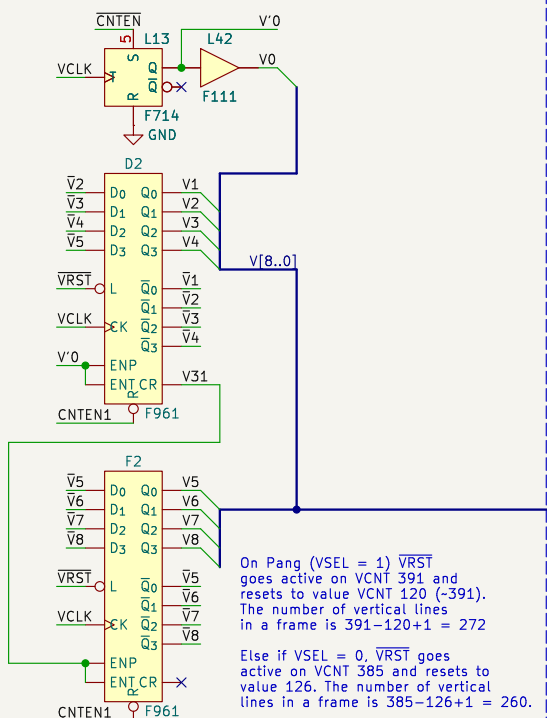
## Horizontal Counter Reset



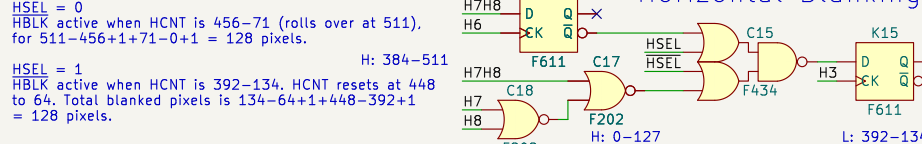
## CLK Divided



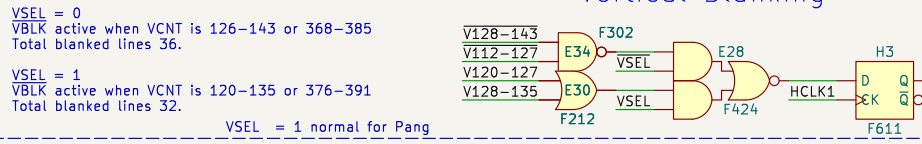
## Vertical Counter



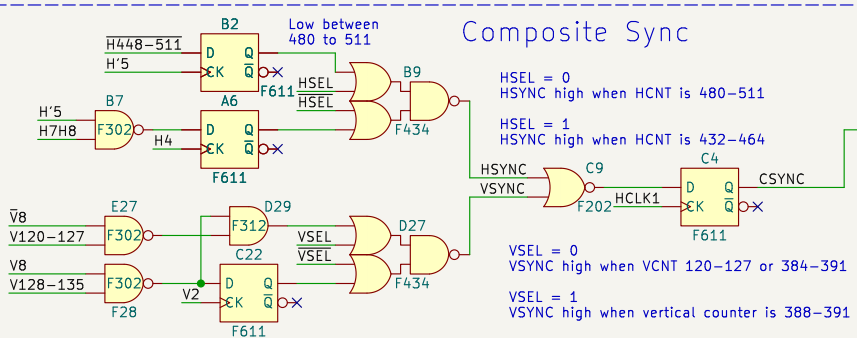
## Horizontal Blanking



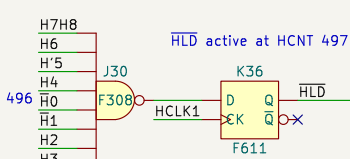
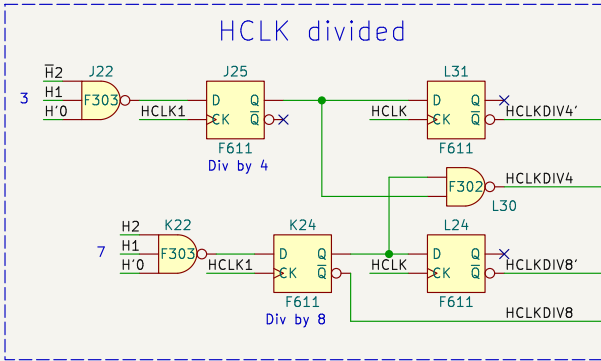
## Vertical Blanking



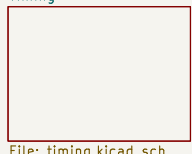
## Composite Sync



## HCLK divided



## Timing

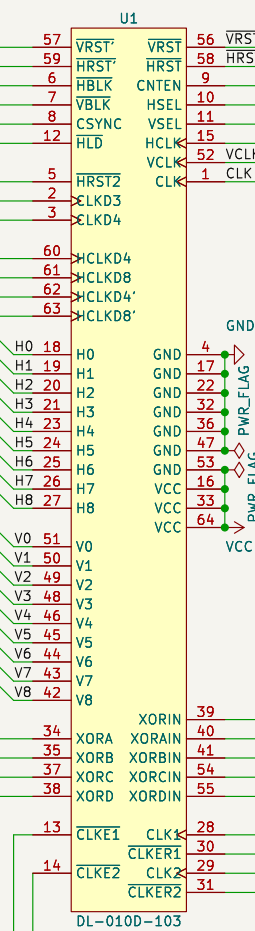


The Schematics have been analyzed from a die picture by InfoSecDJ. The chip is identified as:

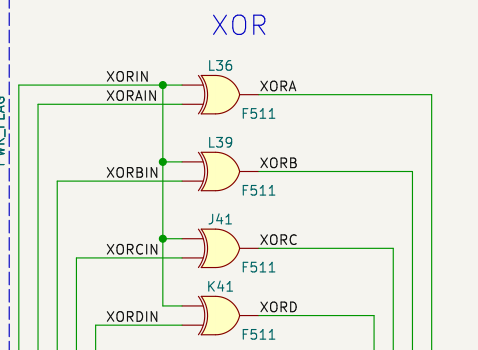
NEC 65006-103

It is a uPD65000 (CMOS-2) series, 3-micron gate array.  
- 528 Basic Cells  
- 12 Columns, 44 Rows

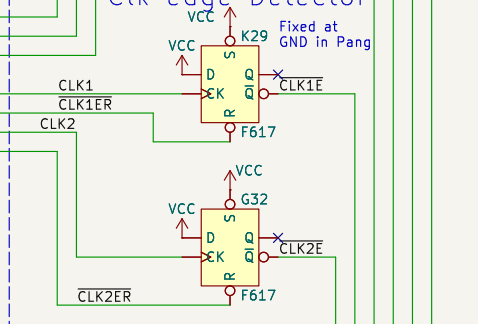
CNTEN Connected to VCC on pang



## XOR



## Clk edge Detector



Ulf Skutnabba, twitter: @skutis77

Sheet: /

File: dl-010d-103.kicad\_sch

Title: **Capcom DL-010D-103**

Size: A3

Date: 2025-09-18

Rev:

KiCad E.D.A. 8.0.9

Id: 1/2



HSEL = 0, VSEL = 1 is used on all games on the Capcom/Mitchell platform.

Total pixels: 512

Active pixels: 384

Blanked pixels: 128

Pixel clock: 8Mhz

Hsync frequency: 15.625kHz

Vertical lines: 272

Blanked lines: 32

Vsync frequency: 57.44485Hz

Sheet: /Timing/  
File: timing.kicad\_sch

Title:

Size: A3

Date: 2025-09-18

Rev:

KiCad E.D.A. 8.0.9

Id: 2/2