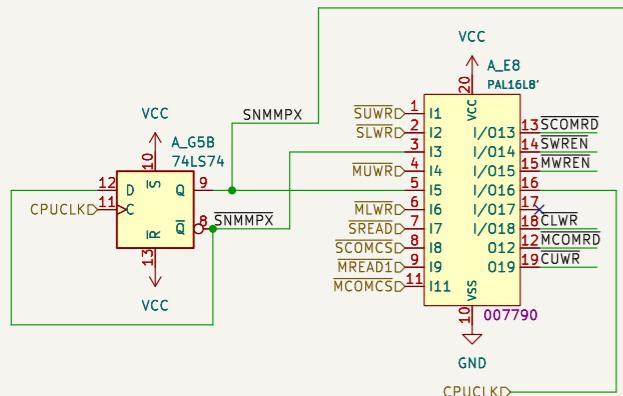


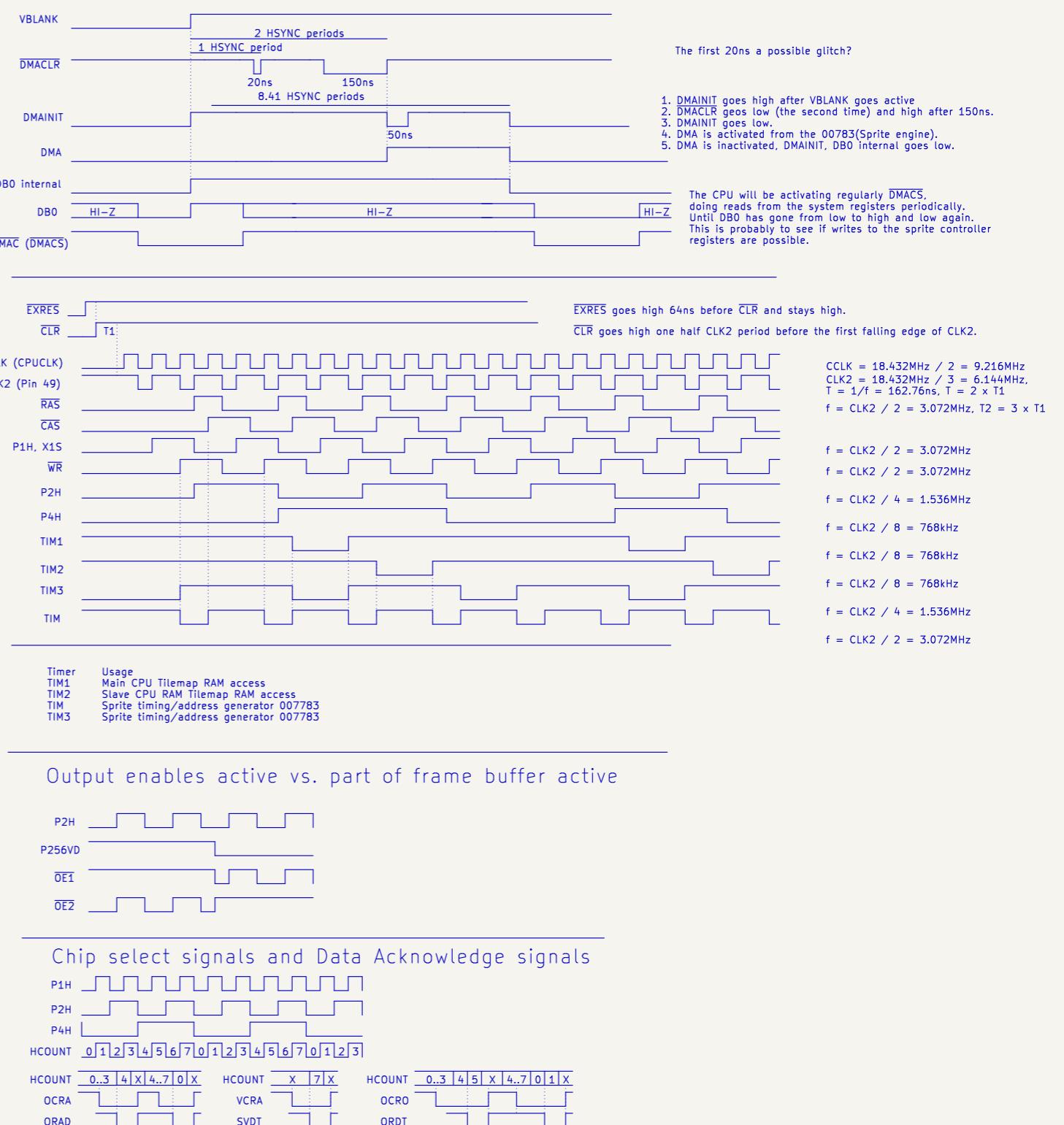
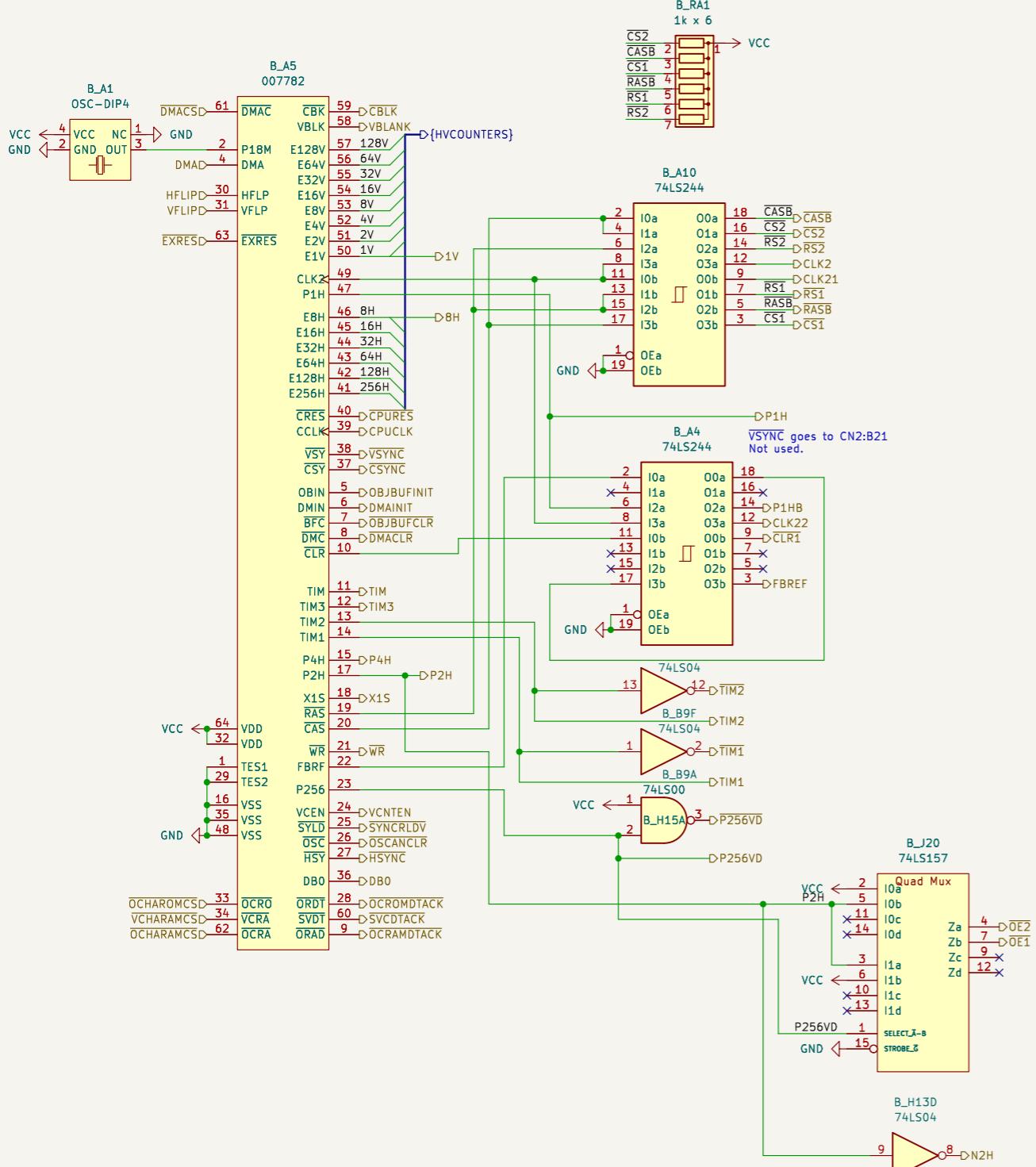
Konami 007790

$MCOMRD = \neg(MREAD1 \& \neg MCOMCS) = MREAD1 \mid MCOMCS$   
 $SCOMRD = \neg(SREAD \& \neg SCOMCS)$   
 $SWREN = \neg(SNMMPPX \& SREAD \& \neg SCOMCS)$   
 $MWREN = \neg(SNMMPPX \& MREAD1 \& \neg MCOMCS)$   
 $CLWR = \neg(CLWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$   
 $CUWR = \neg(CUWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg MUWR \& \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$

A All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16LB device it is kept in that form. The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



## DMA Synchronization



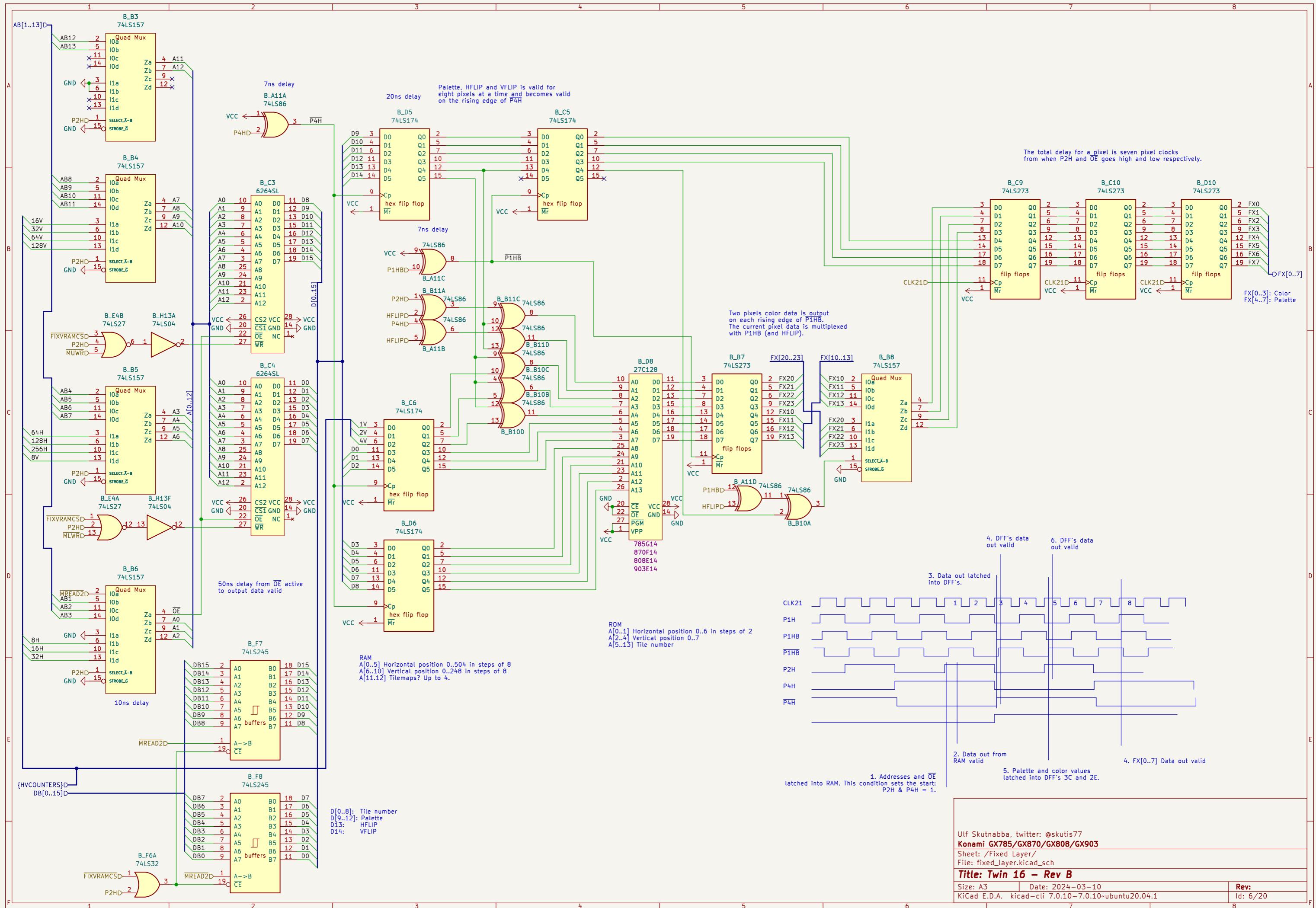
Ulf Skutnabba, twitter: @skutis77  
**Konami GX785/GX870/GX808/GX903**

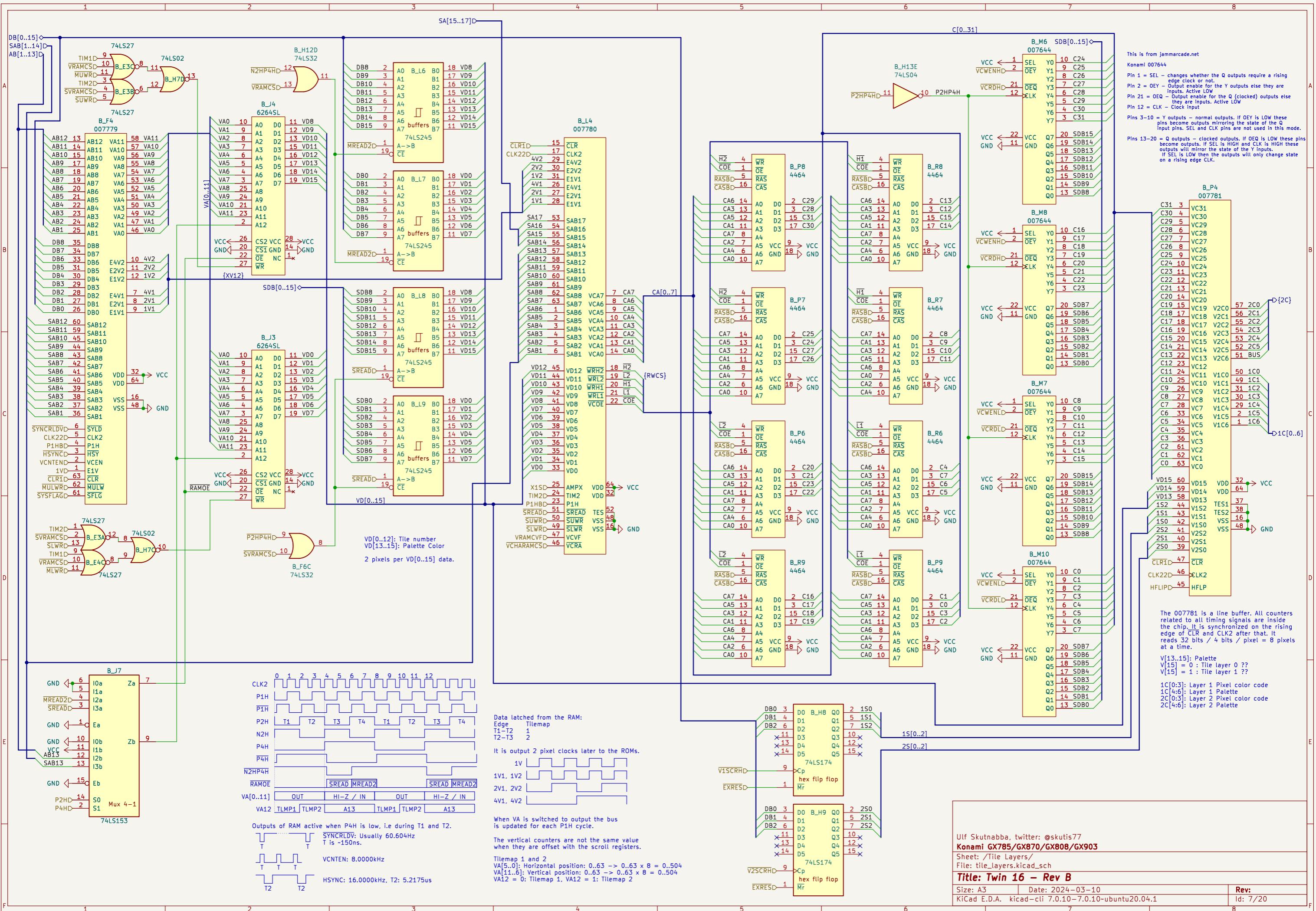
Sheet: /Timing/  
File: timing.kicad\_sch

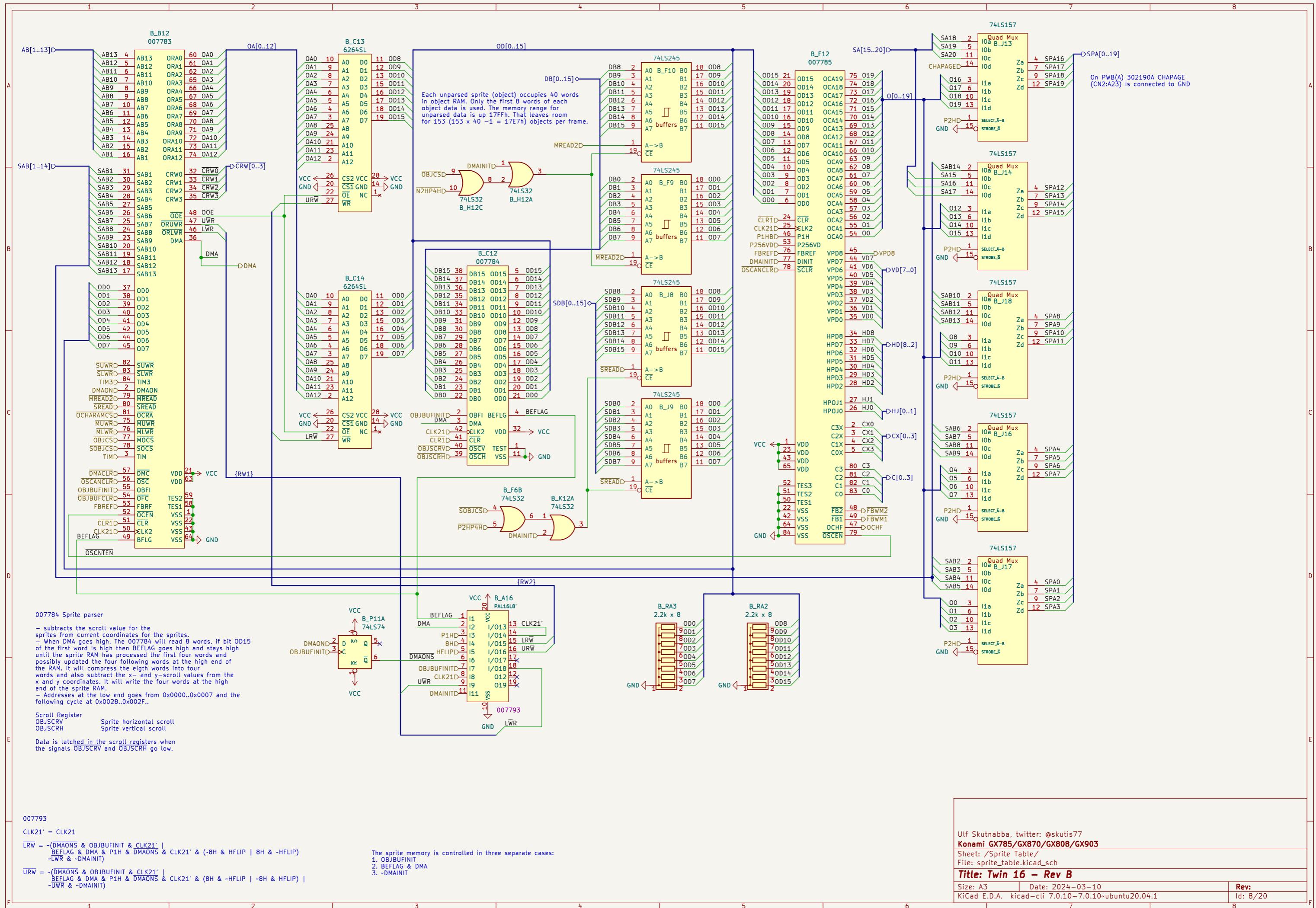
**Title: Twin 16 – Rev B**

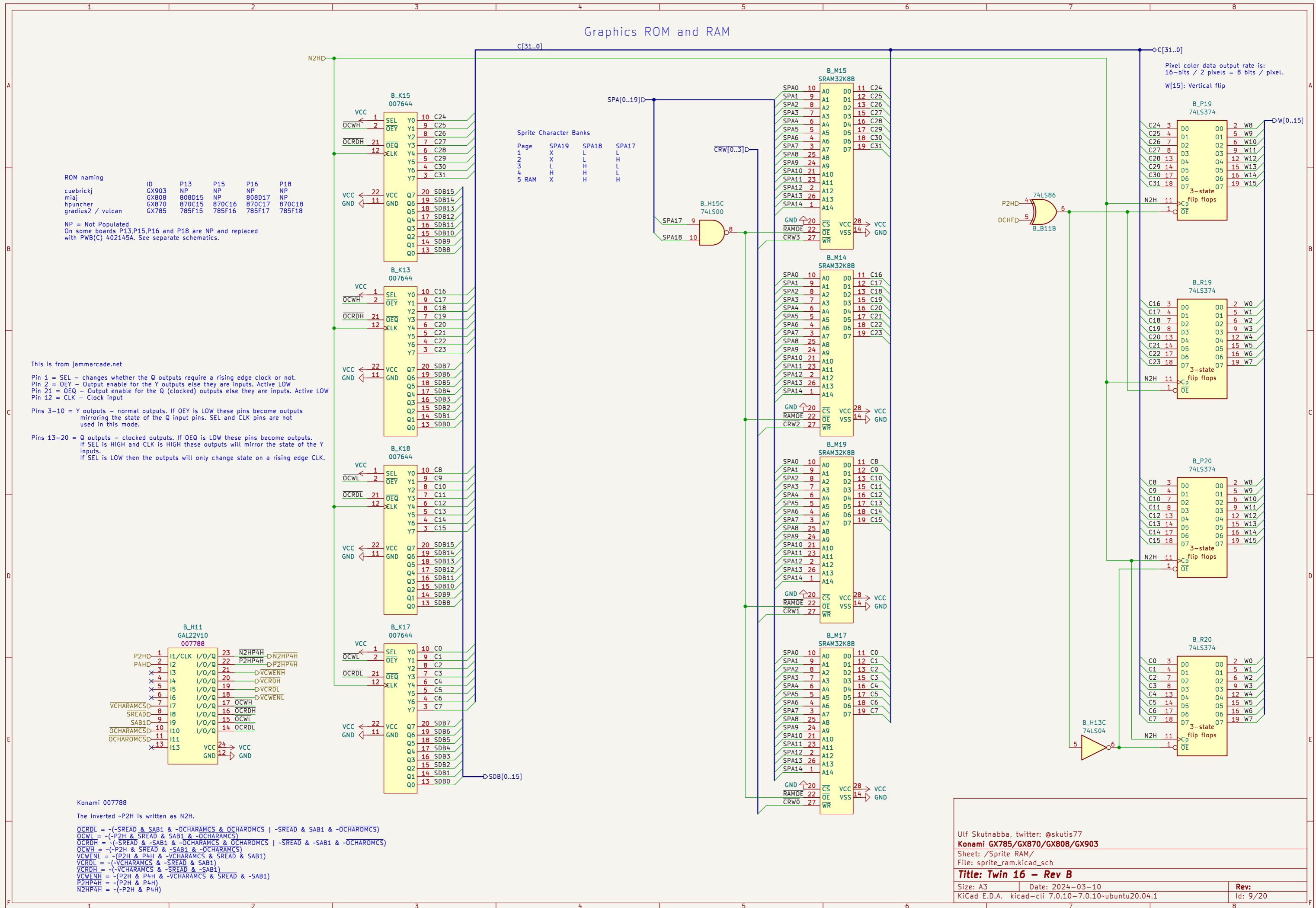
Size: A3 | Date: 2024-03-10  
KiCad E.D.A. kicad-cl 7.0.10-7.0.10-ubuntu20.04.1

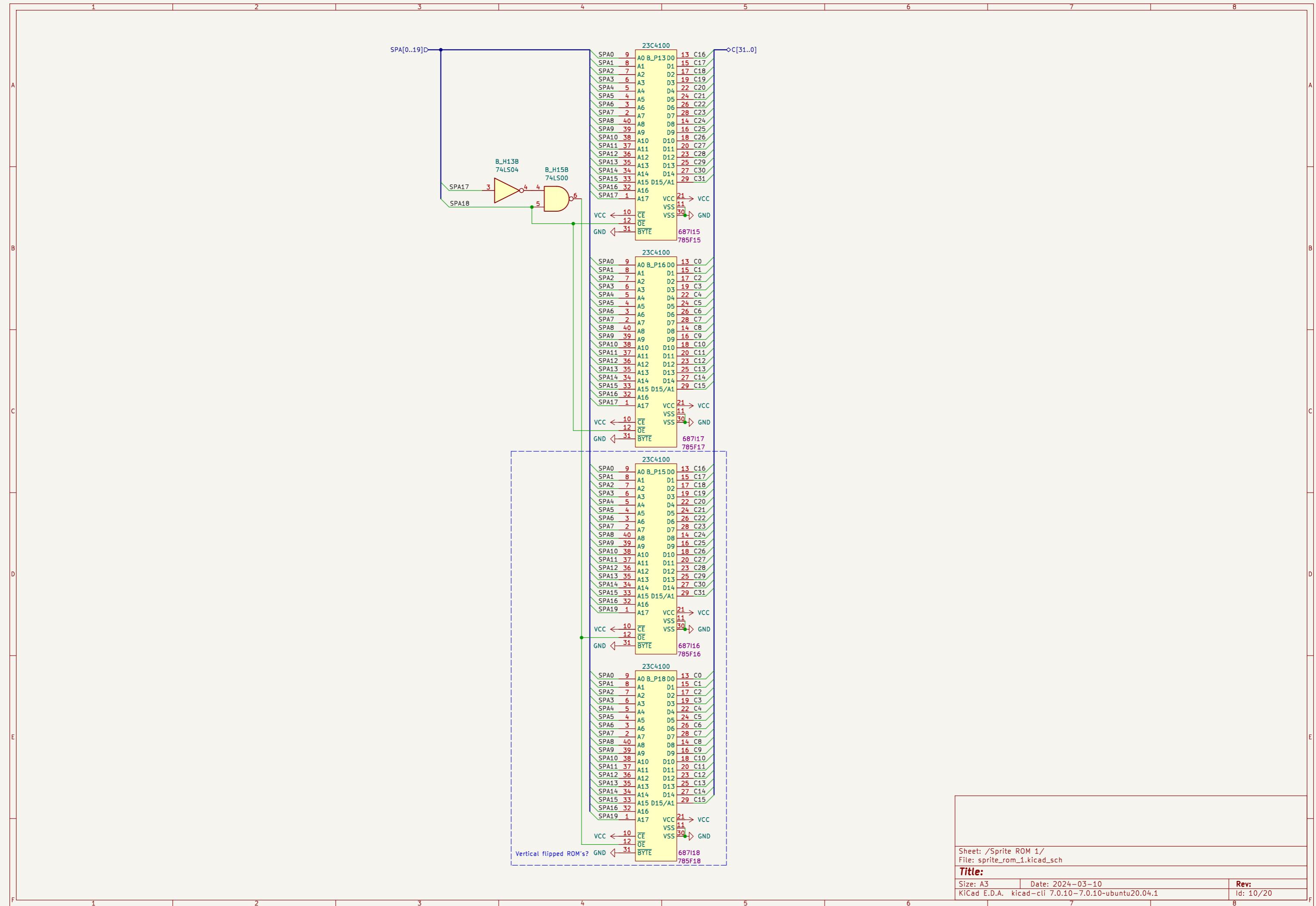
Rev:  
Id: 5/20

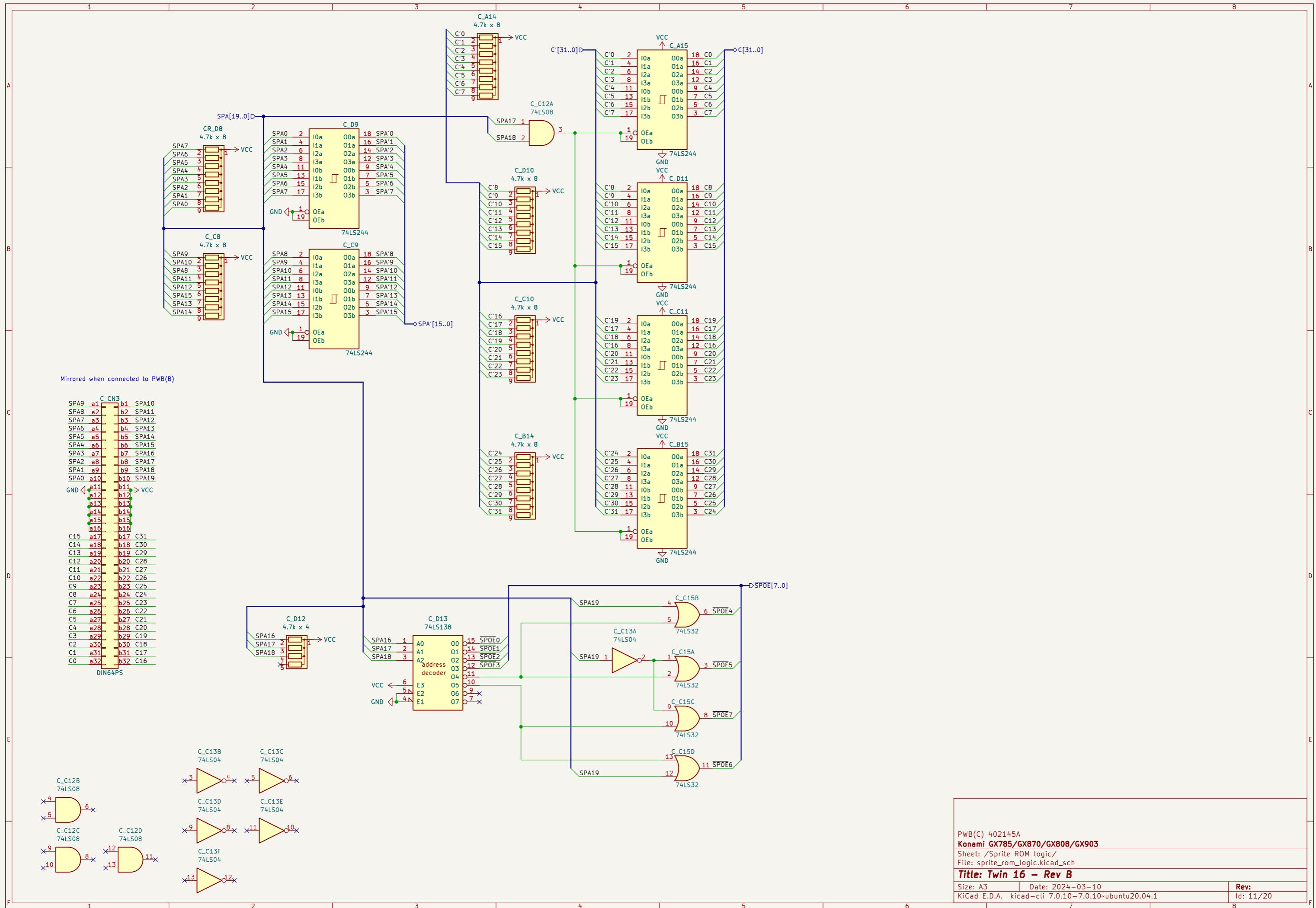


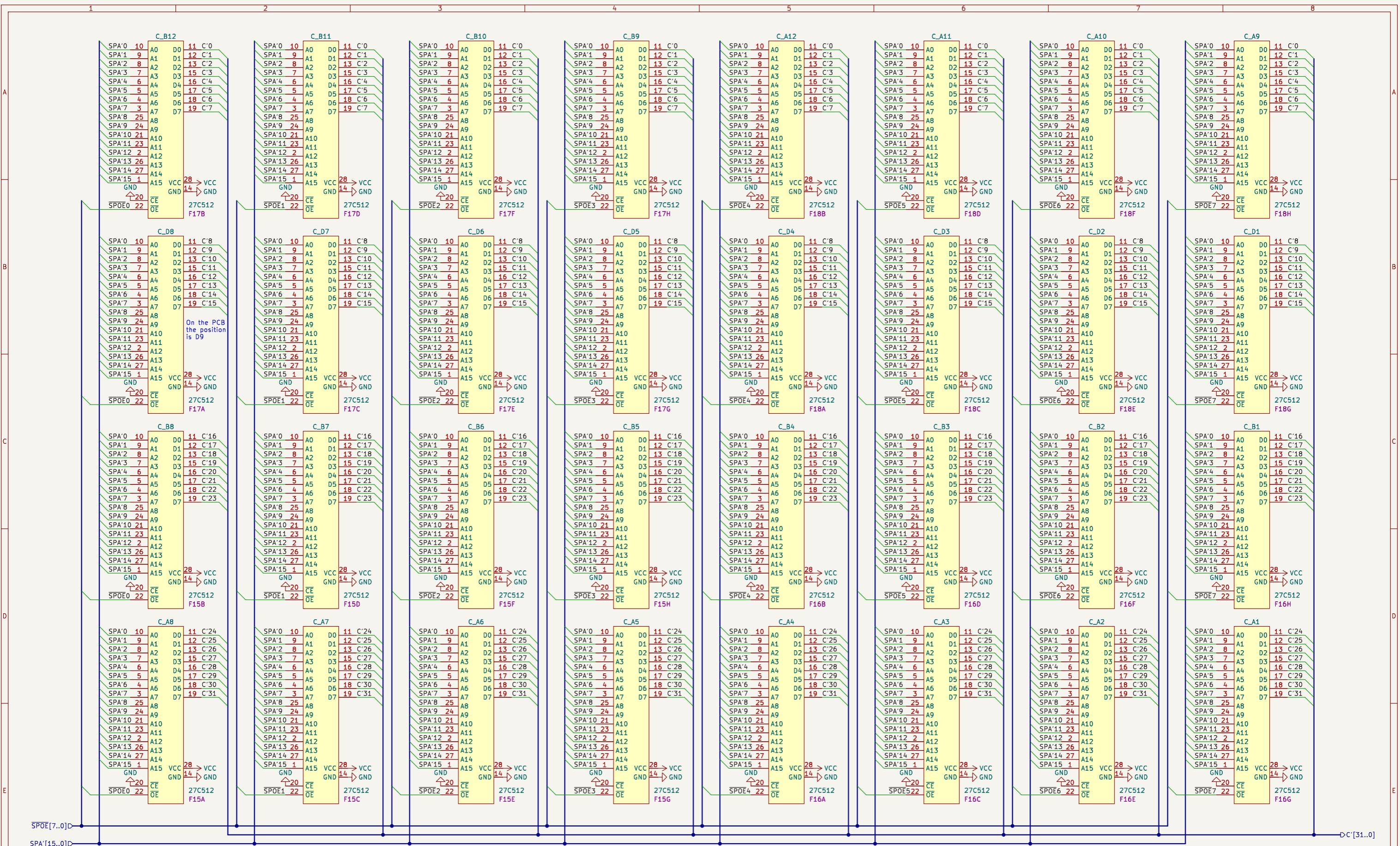












Konami GX785/GX870/GX808/GX903

Sheet: /Sprite ROM 2/  
File: sprite\_rom\_2.kicad\_sch

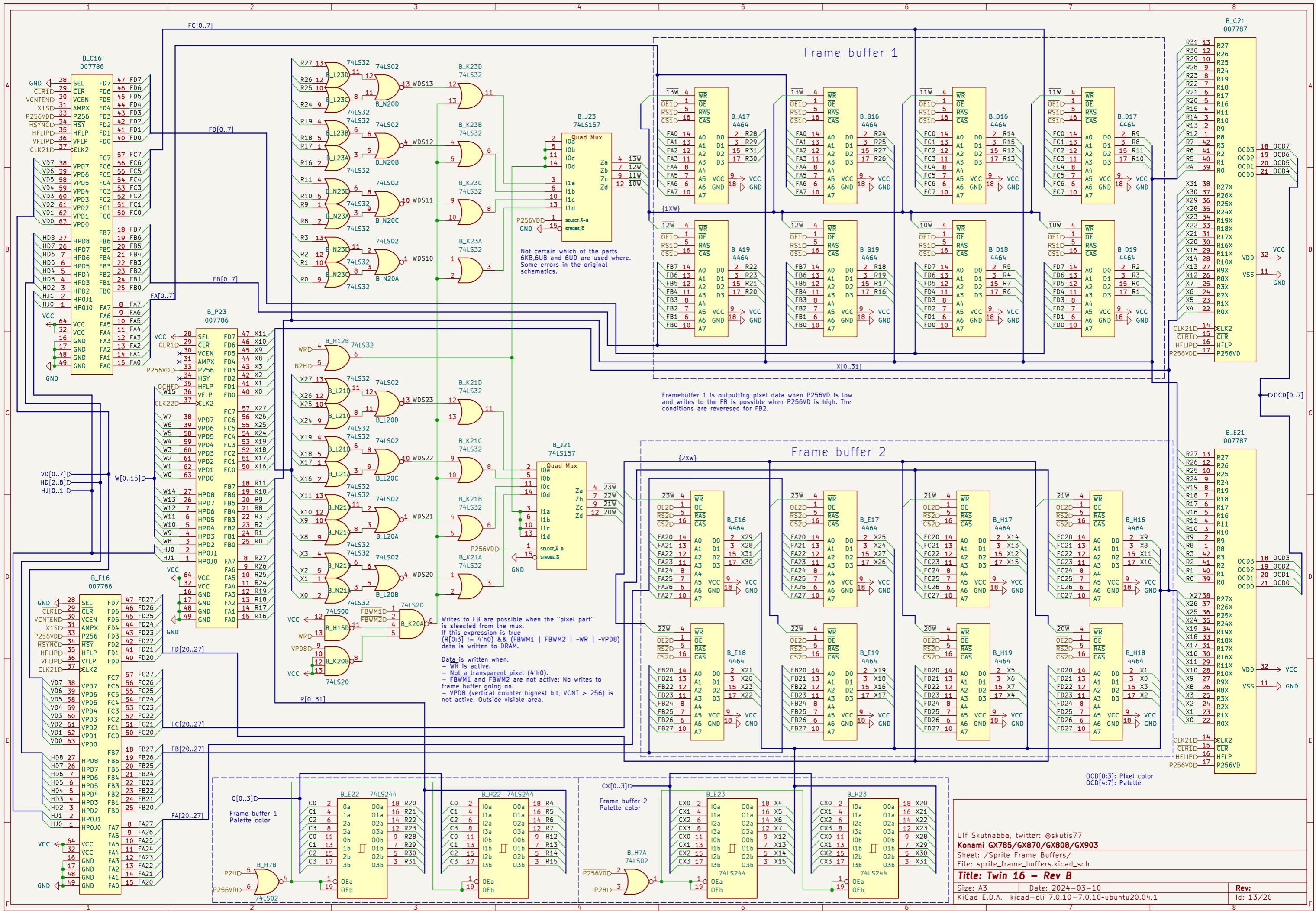
## Title: Twin 16 – Rev B

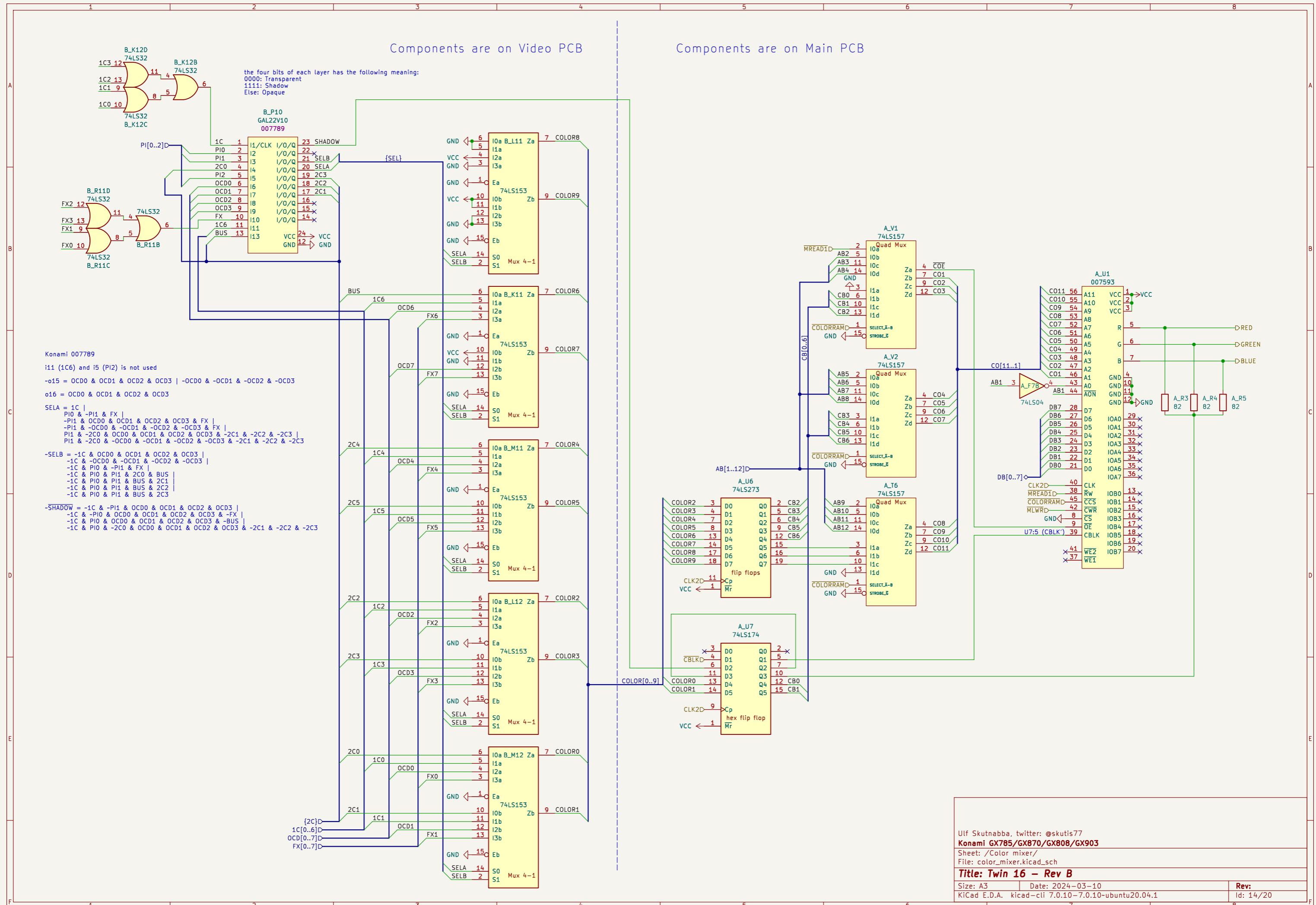
Size: A3 Date: 2024-03  
KiCad EDA kicad-cli 7.0.10-7

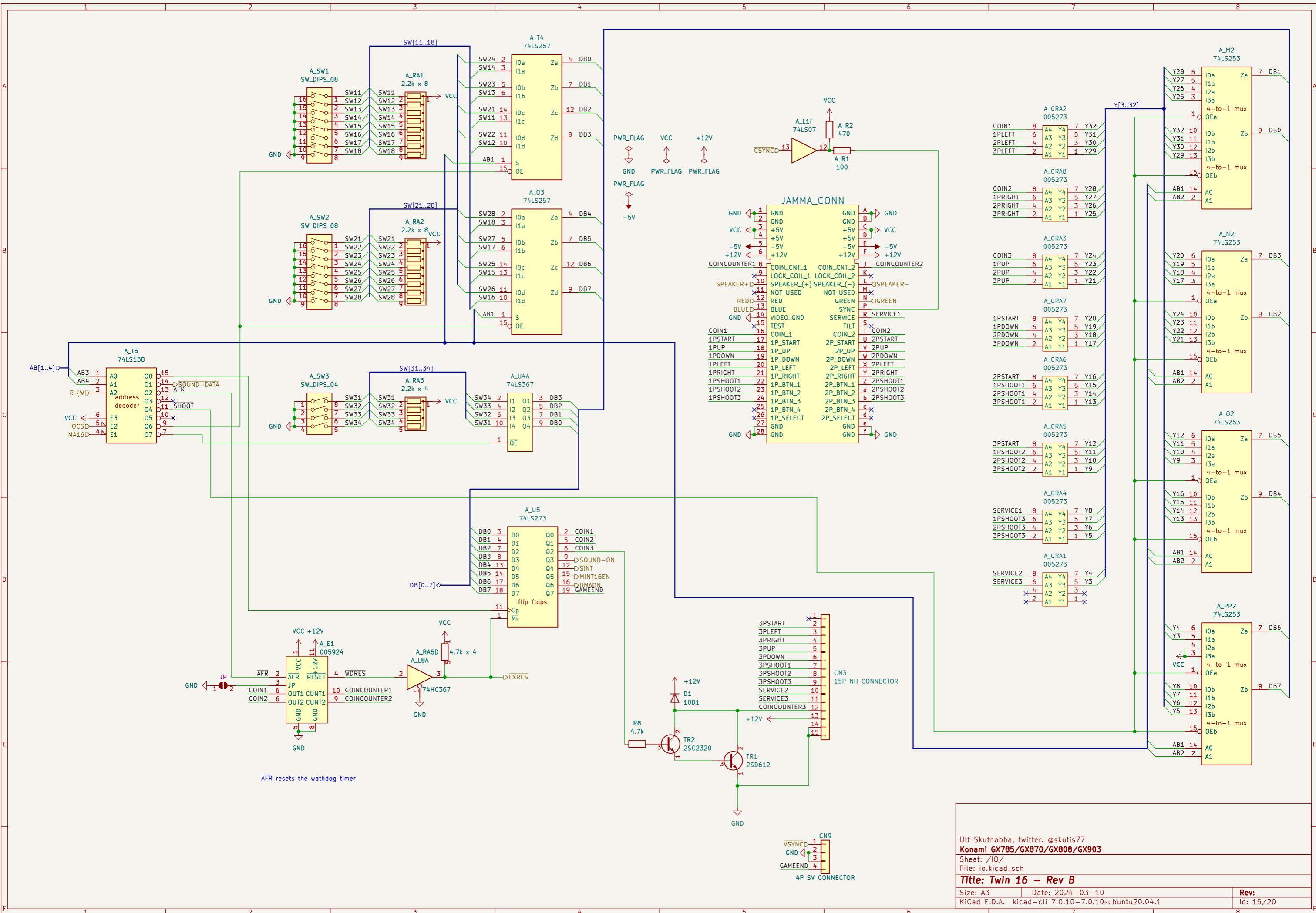
Kicad E.D.A. kicad-cli 7.0.10-7.0.10~ubuntu20.04.1

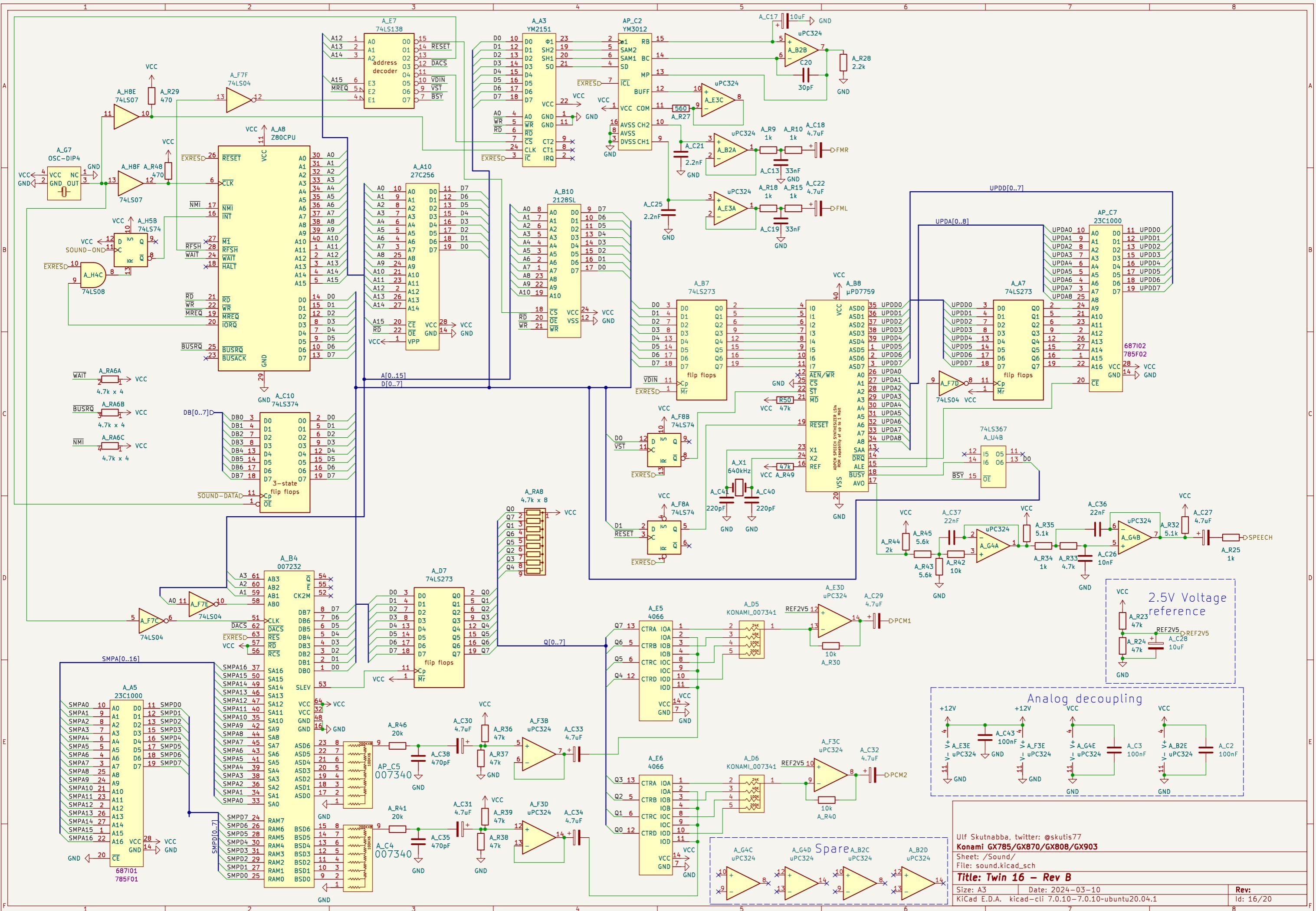
Digitized by srujanika@gmail.com

3

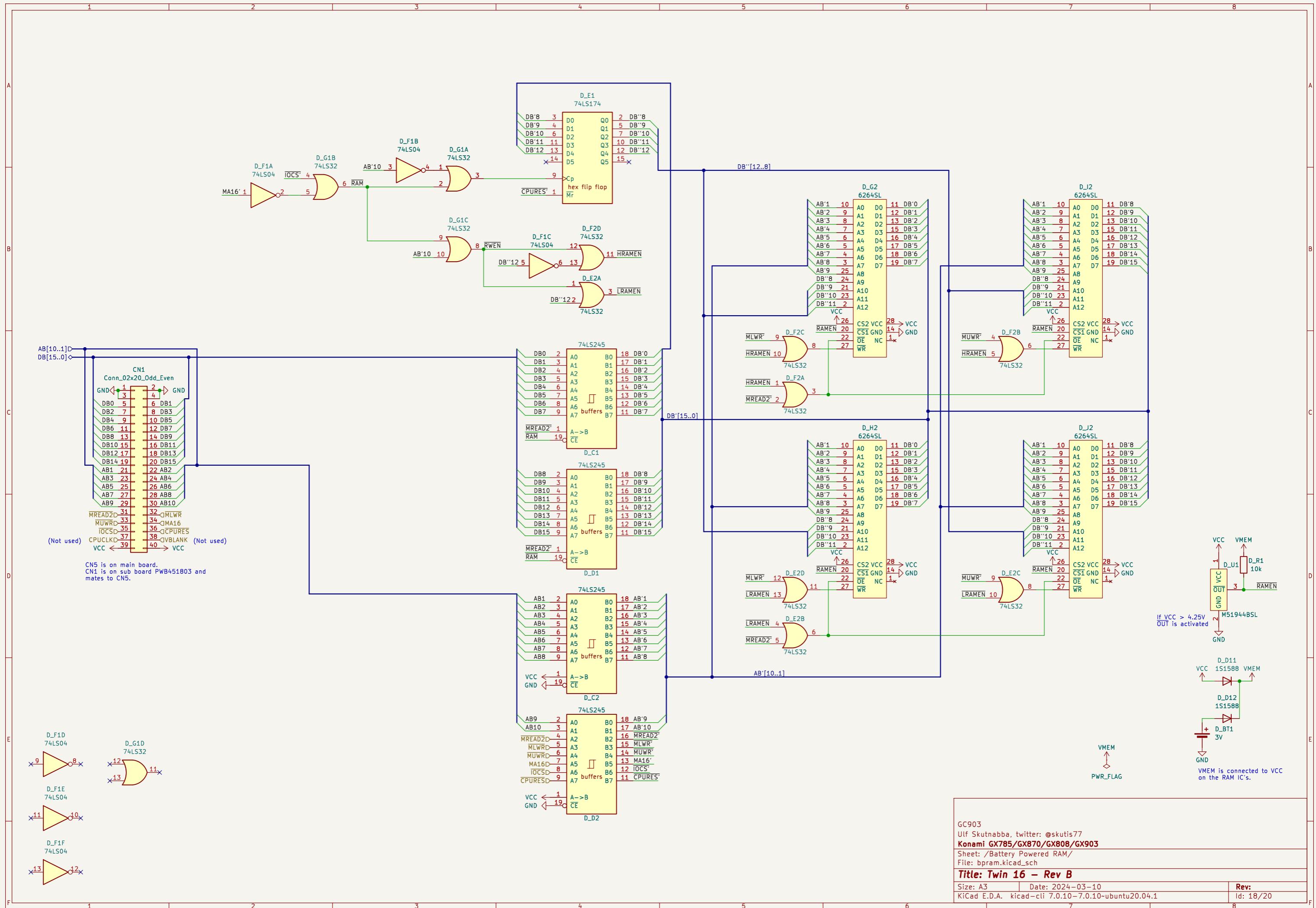




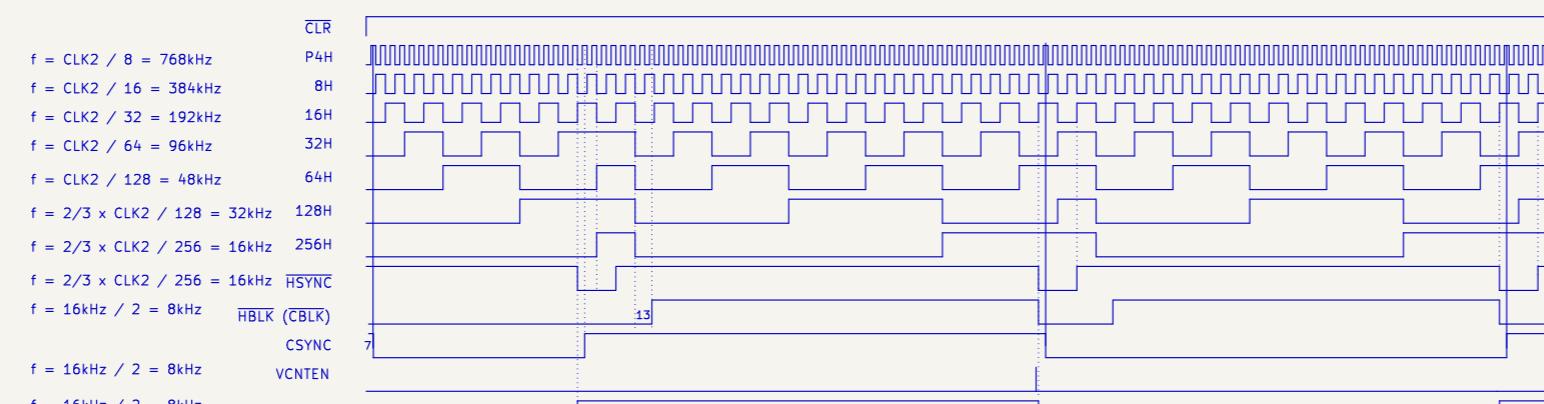








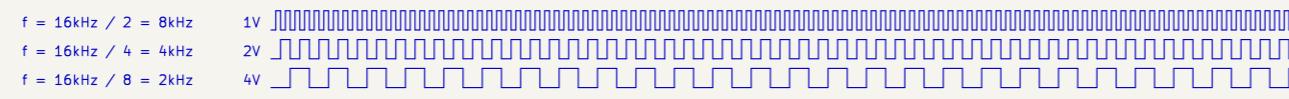
## Horizontal signals



– The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals



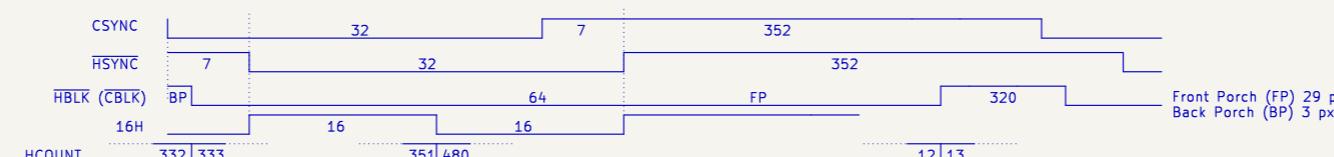
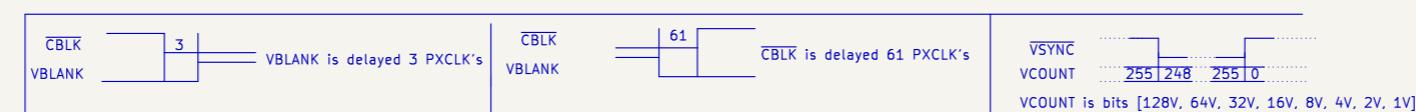
Every 16th pulse is long.  
Every 8th pulse is long.  
Every 4th pulse is long.  
Every 2nd pulse is long.  
High period is longer

VBLANK High:  $7 \times 16 \times 2 = 224$ , Low:  $5 \times 4 \times 2 = 40$   
SYNCRLDV goes low 140ns before FBREF goes low.  
SYNCRLDV goes high again when FBREF goes low.

OBJBUFCLR goes low one pixel clock before the rising edge  
of VBLANK and high again when VBLANK goes high.

60.606Hz, OSCANCLR goes low for 140ns ~ One pixel clock cycle.  
P256VD goes high/low one  
P4H cycle (8 pixels) after VSYNC goes high.

FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.



The horizontal blanking part is shown of the composite blanking signals.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]

HSYNC =  $6.144\text{MHz} / 384 = 16\text{kHz}$

Ulf Skutnabba, twitter: @skutis77

Konami GX785/GX870/GX808/GX903

Sheet: /Timing diagrams/

File: timing\_diagrams.kicad\_sch

Title: Twin 16 – Rev B

Size: A3 Date: 2024-03-10  
KiCad E.D.A. kicad-cliv 7.0.10-7.0.10-ubuntu20.04.1

Rev: Id: 19/20

