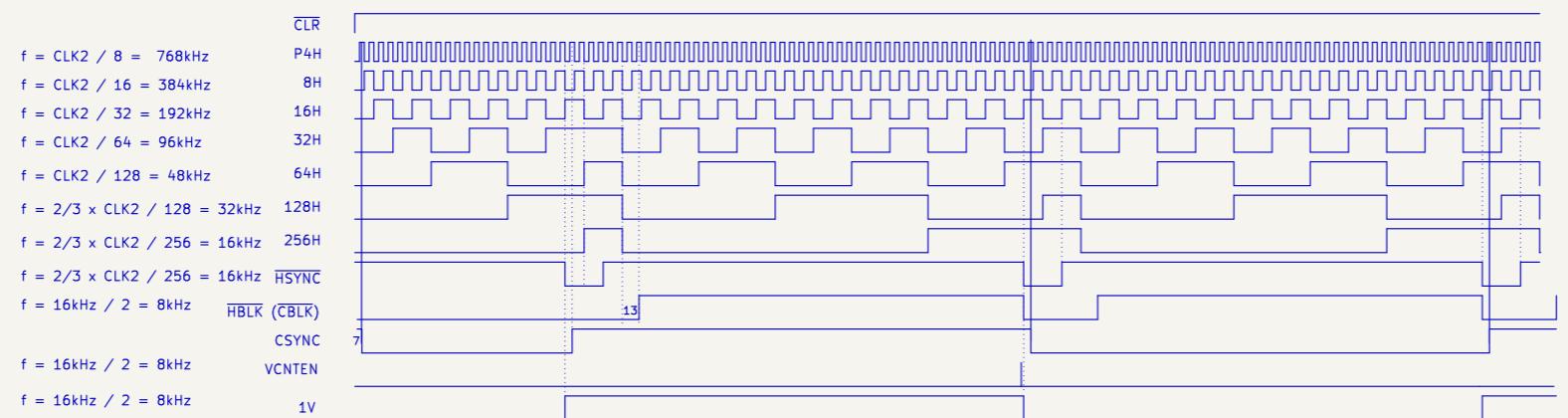


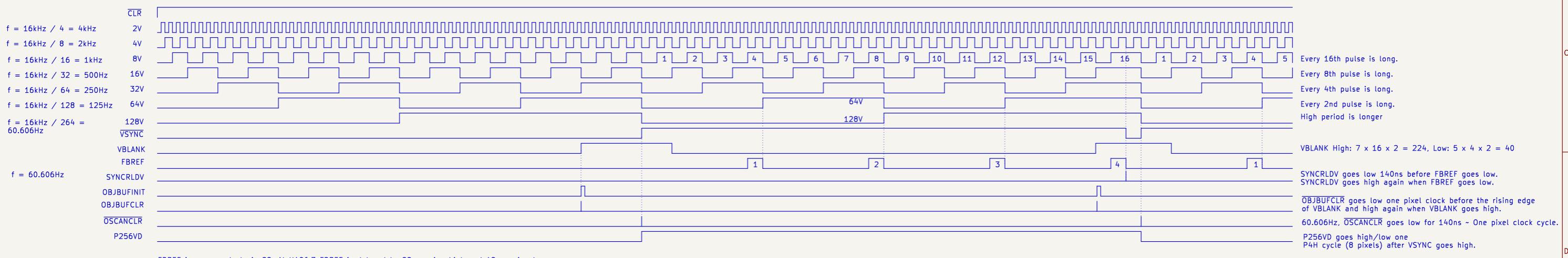
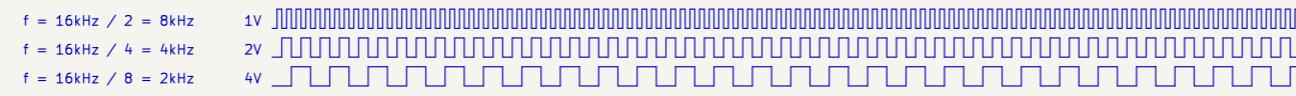
## Horizontal signals



- The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

- CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

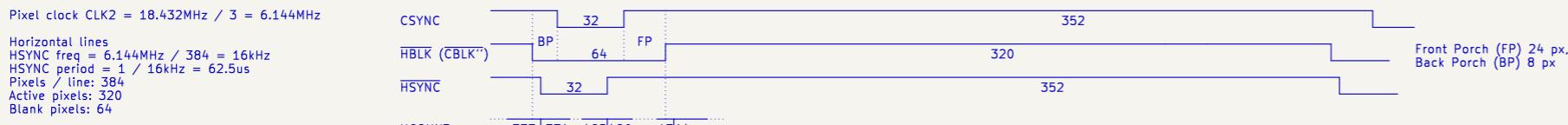
## Vertical signals



FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

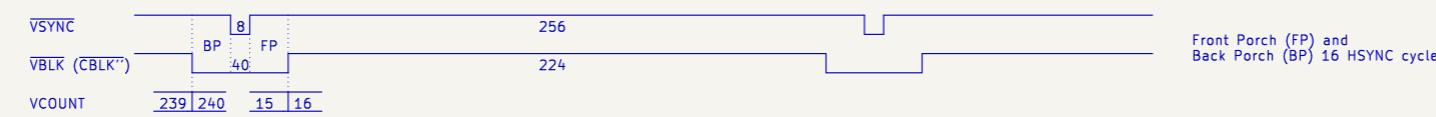
## Horizontal and vertical synch timing diagrams

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.  
All edges are synchronised to the rising edge of CLK2.



Front Porch (FP) 24 px,  
Back Porch (BP) 8 px

The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.  
All edges are synchronised to the falling edge of HSYNC.



Front Porch (FP) and  
Back Porch (BP) 16 HSYNC cycles.

### Konami GX870

Sheet: /Timing diagrams/  
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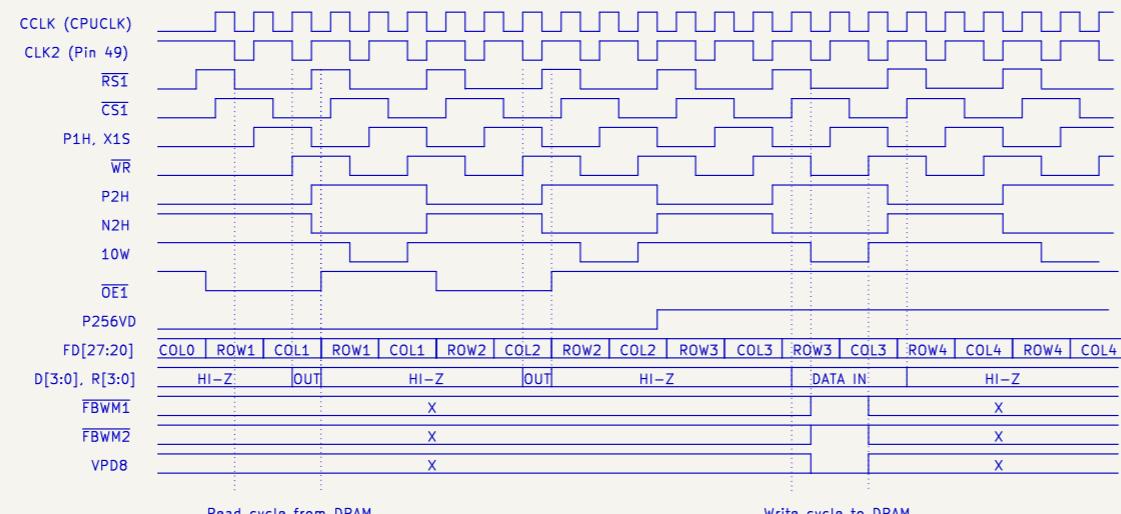
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**Konami GX870**

Sheet: /Sprite timing diagrams/  
 File: sprite\_timing\_diagrams.kicad\_sch

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