

Ulf Skutnabba, twitter: @skutis77

Taito K1100319A

Sheet: /

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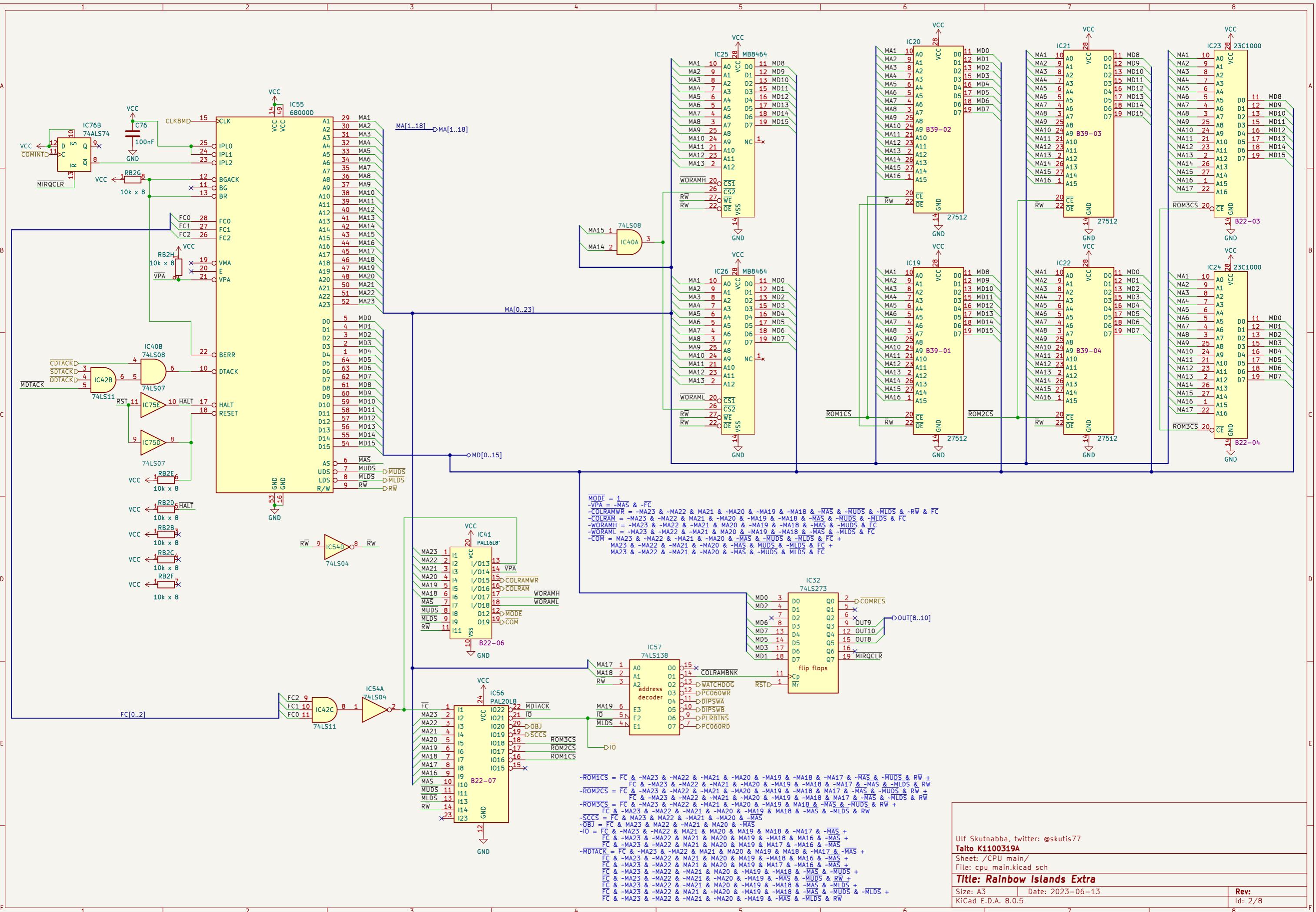
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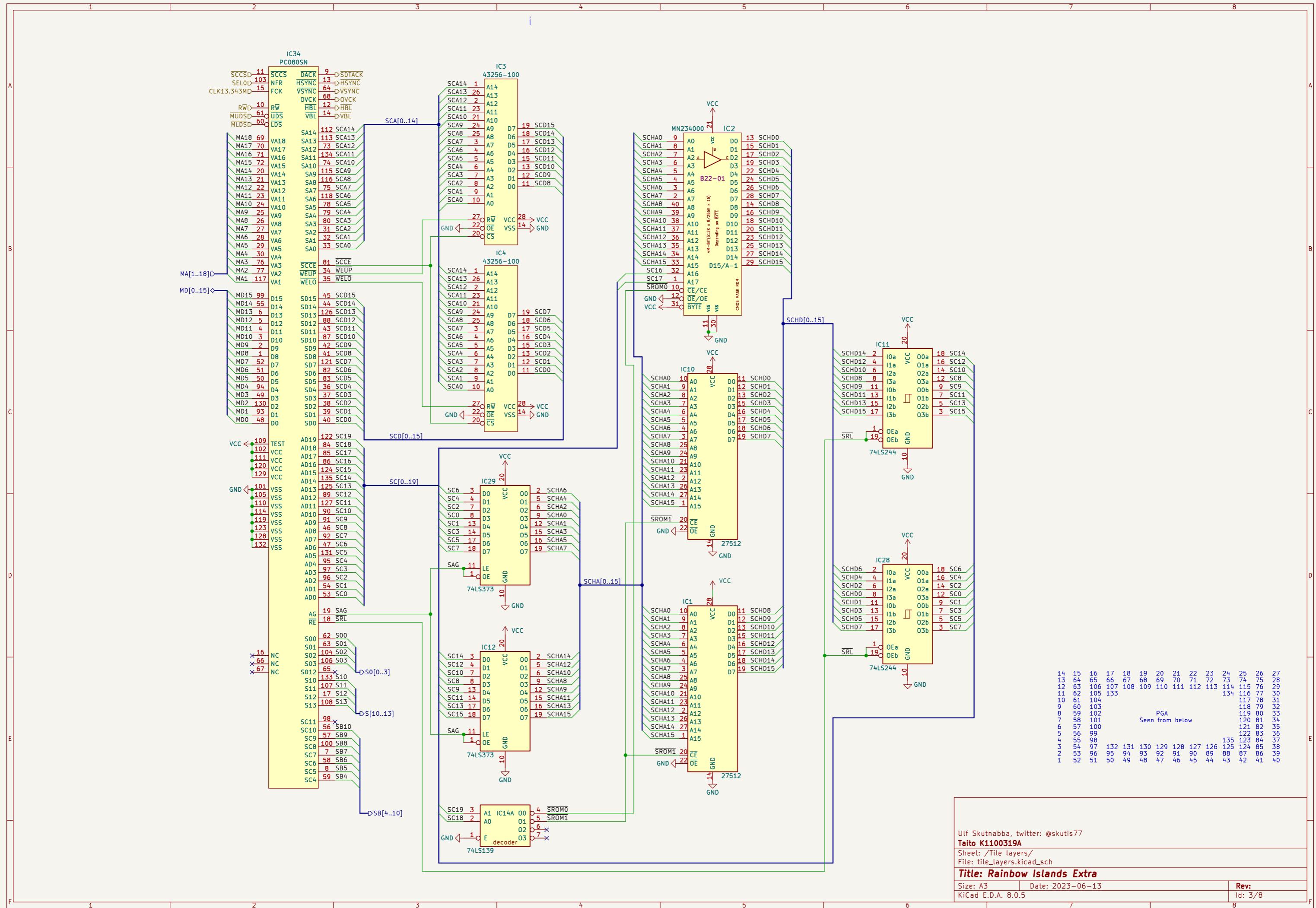
Size: A3 | Date: 2023-06-13

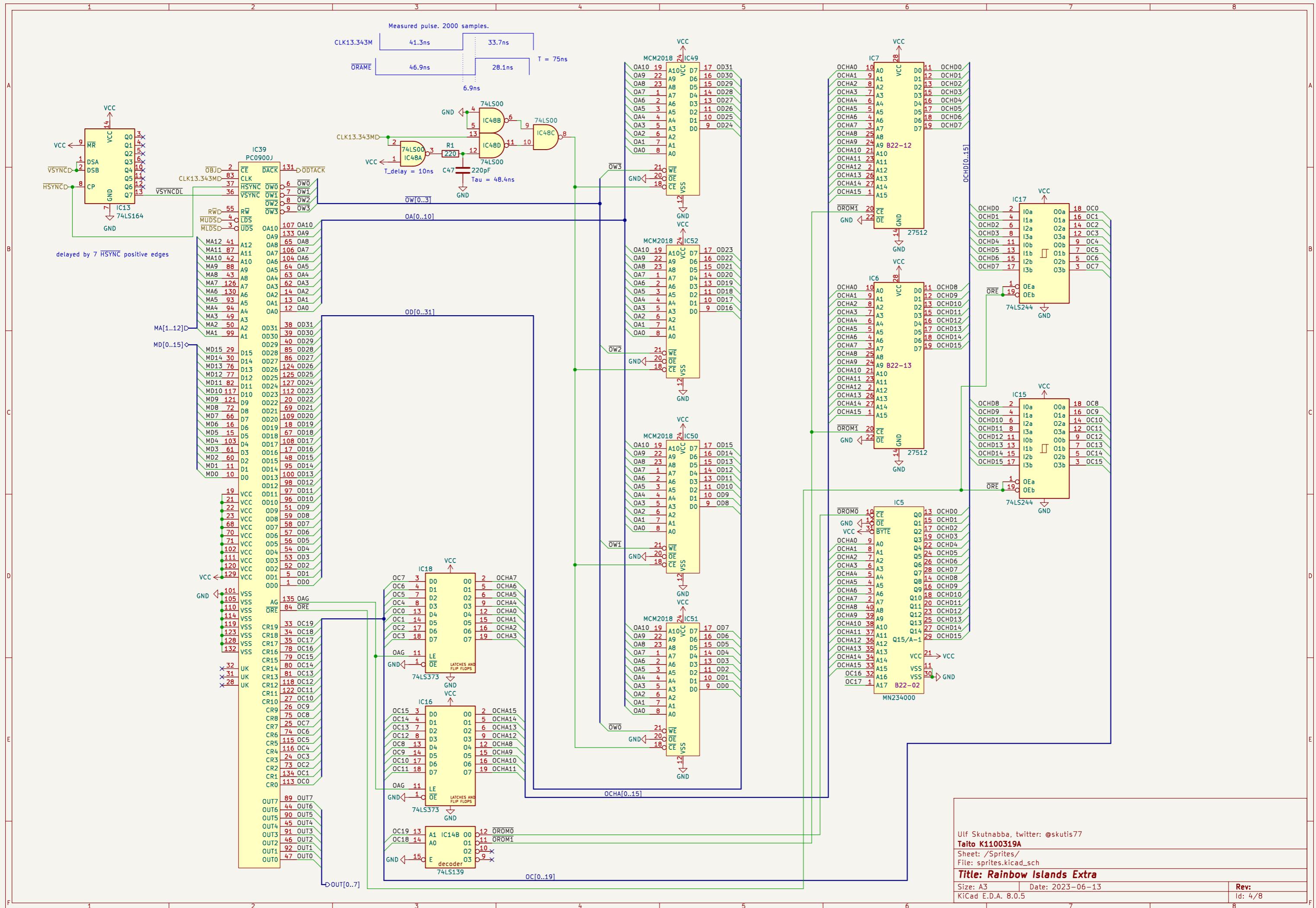
KiCad E.D.A. 8.0.5

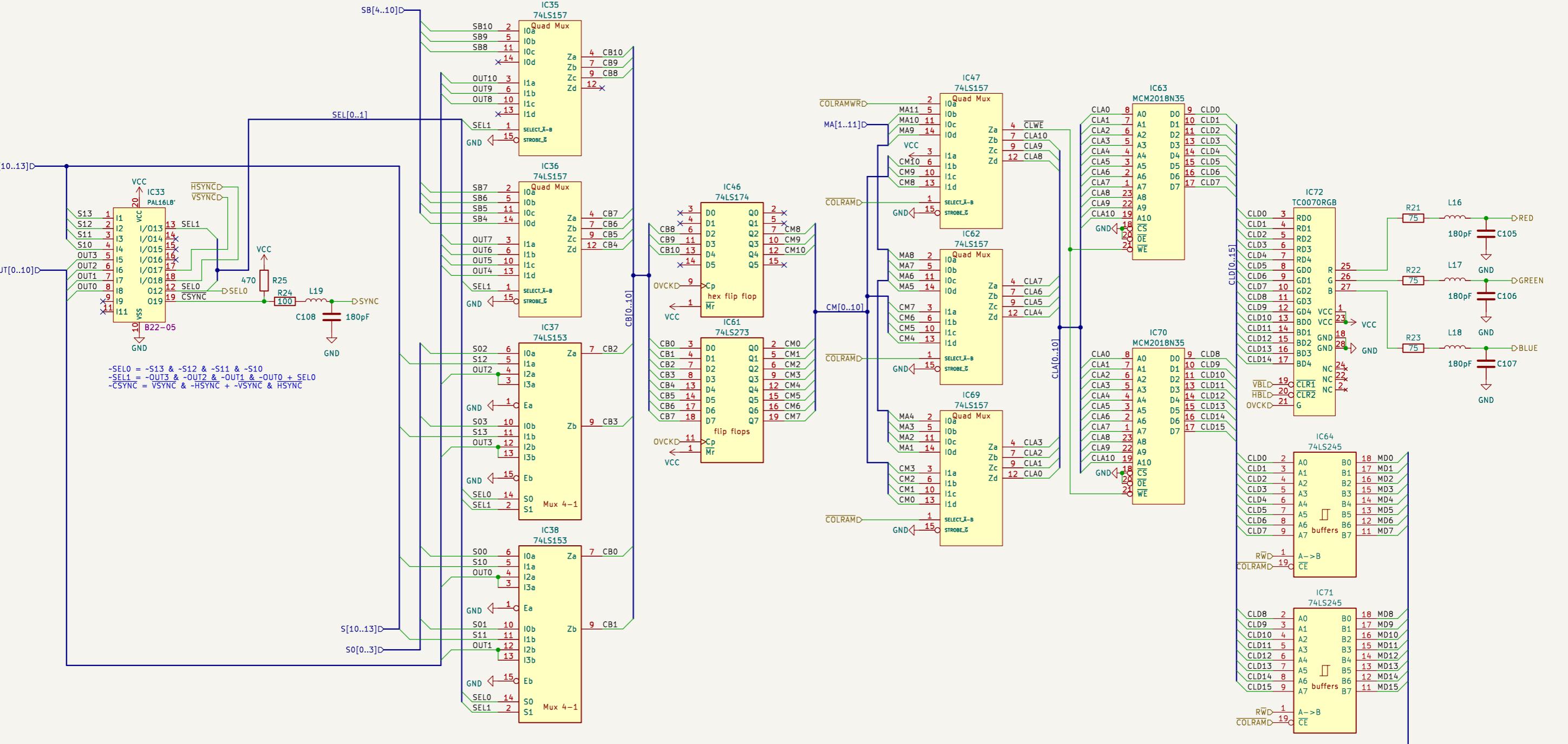
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Sheet: /Color mixer/

File: color_mixer.kicad_sch

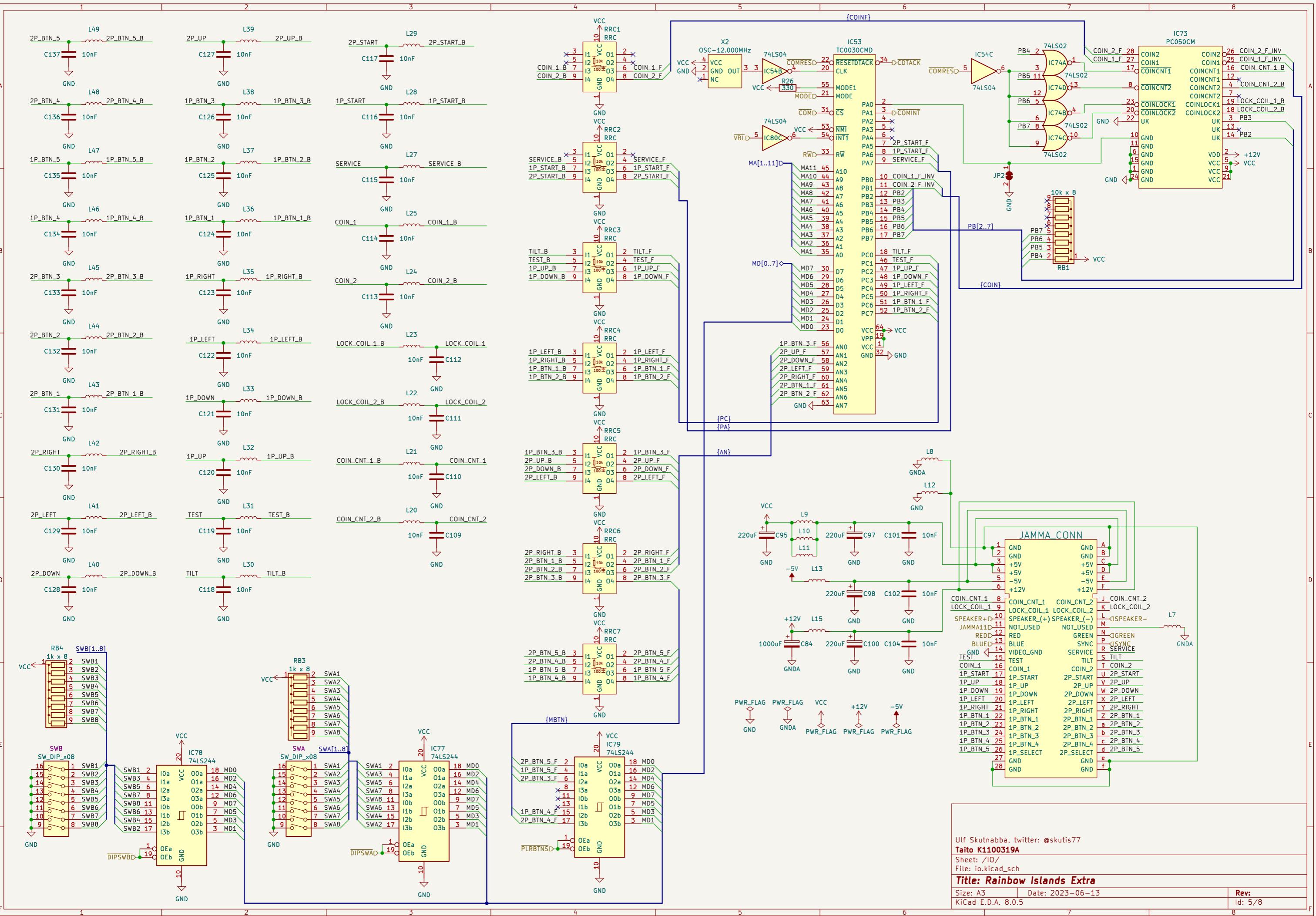
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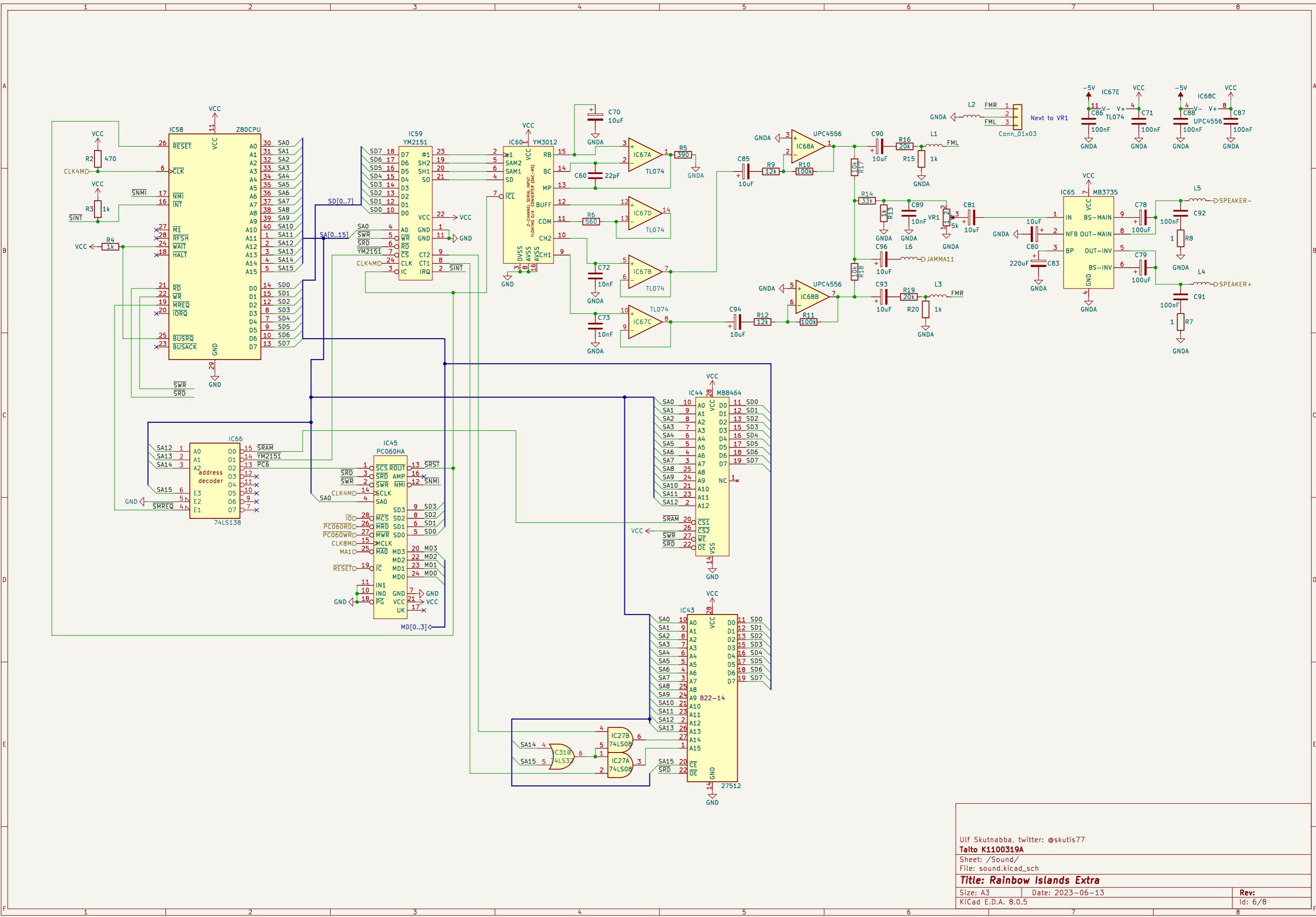
Size: A3 Date: 2023-06-13

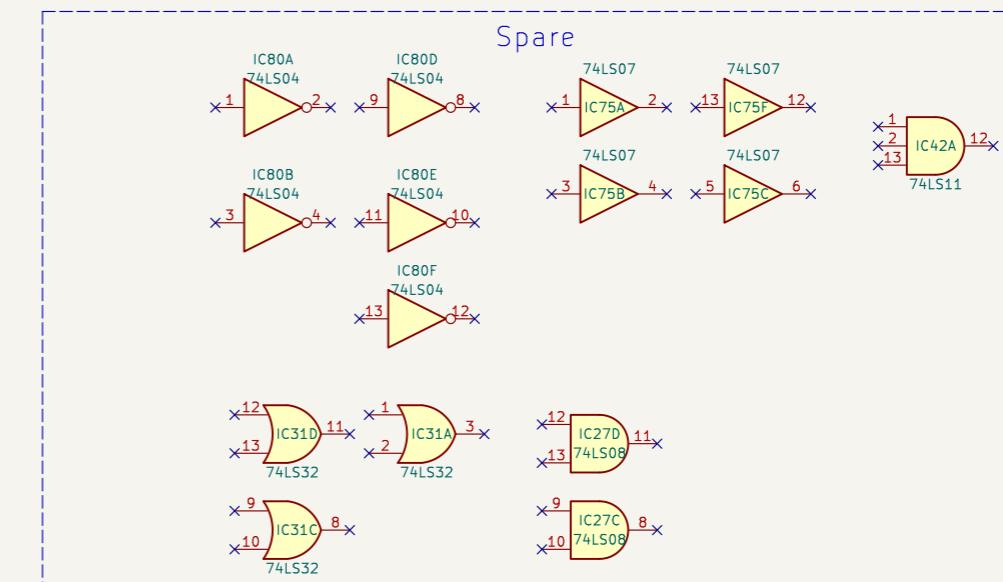
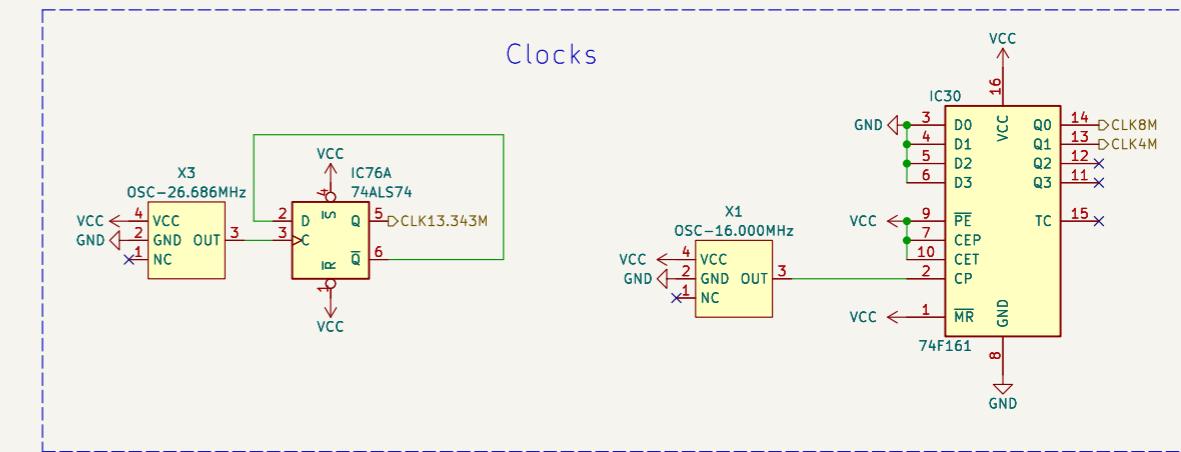
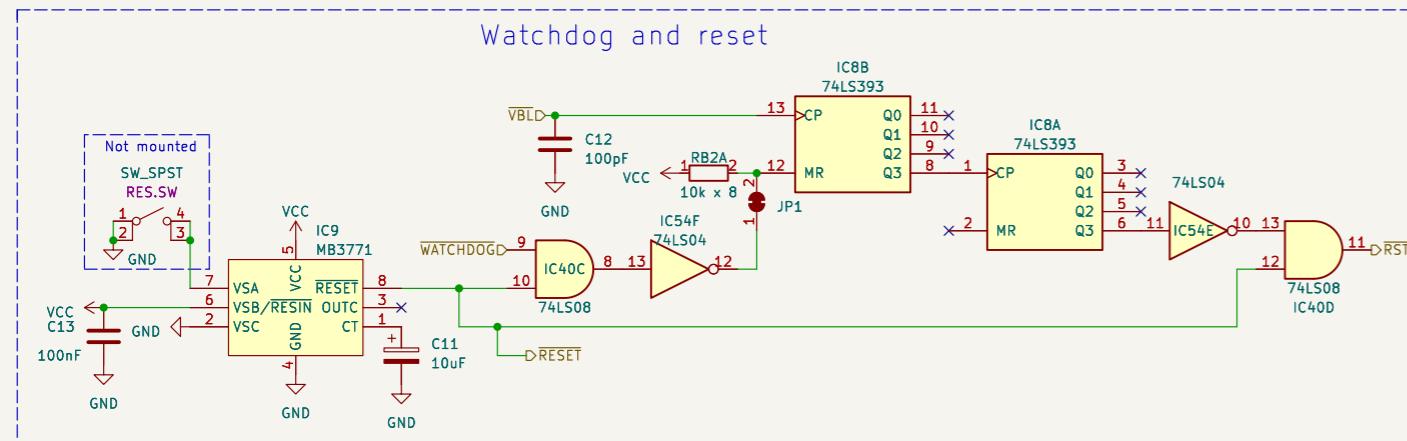
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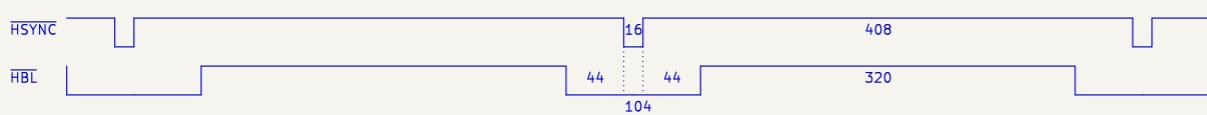




Horizontal and vertical synch timing diagrams

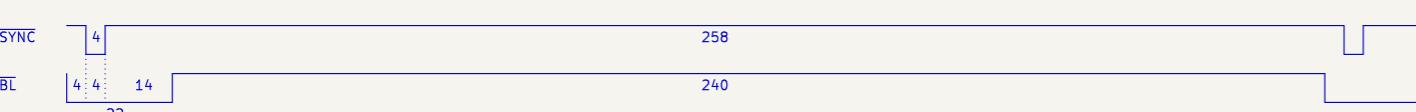
The pixel clock is derived from the 26.686MHz oscillator.
Pixel clock OVCK: $f = 26.686\text{MHz} / 4 = 6.6715\text{MHz}$

The numbers in the HSYNC and HBL diagram are pixel clock cycles.
All edges are synchronised to the rising edge of OVCK.



HSYNC and HBL
Frequency $f = 6.6715\text{MHz} / 424 = 15.734670\text{kHz}$.
Period $T = 1/f = 63.5539\mu\text{s}$.

The numbers in the VSYNC and VBL diagram are HSYNC cycles.
All edges are synchronised to the falling edge of HSYNC.



VSYNC and VBL:
Frequency $f = 15.734670\text{kHz} / 262 = 60.05599\text{Hz}$
Period $T = 1/f = 1 / 15.734670\text{kHz} = 16.6511\text{ms}$

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Sheet: /Misc/

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