

1 2 3 4 5 6 7 8

A

B

C

D

E

F



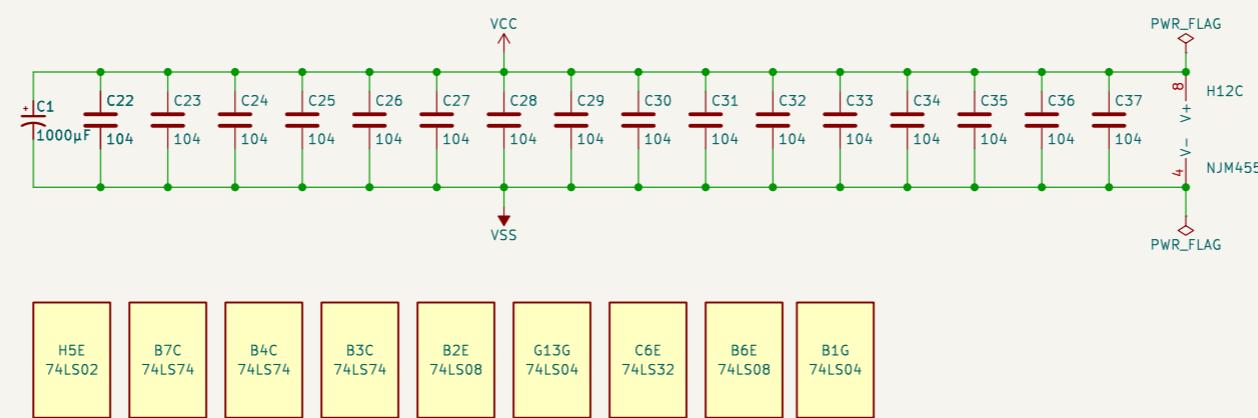
E.Triana
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Sheet: /capacitors/
File: capacitors.kicad_sch

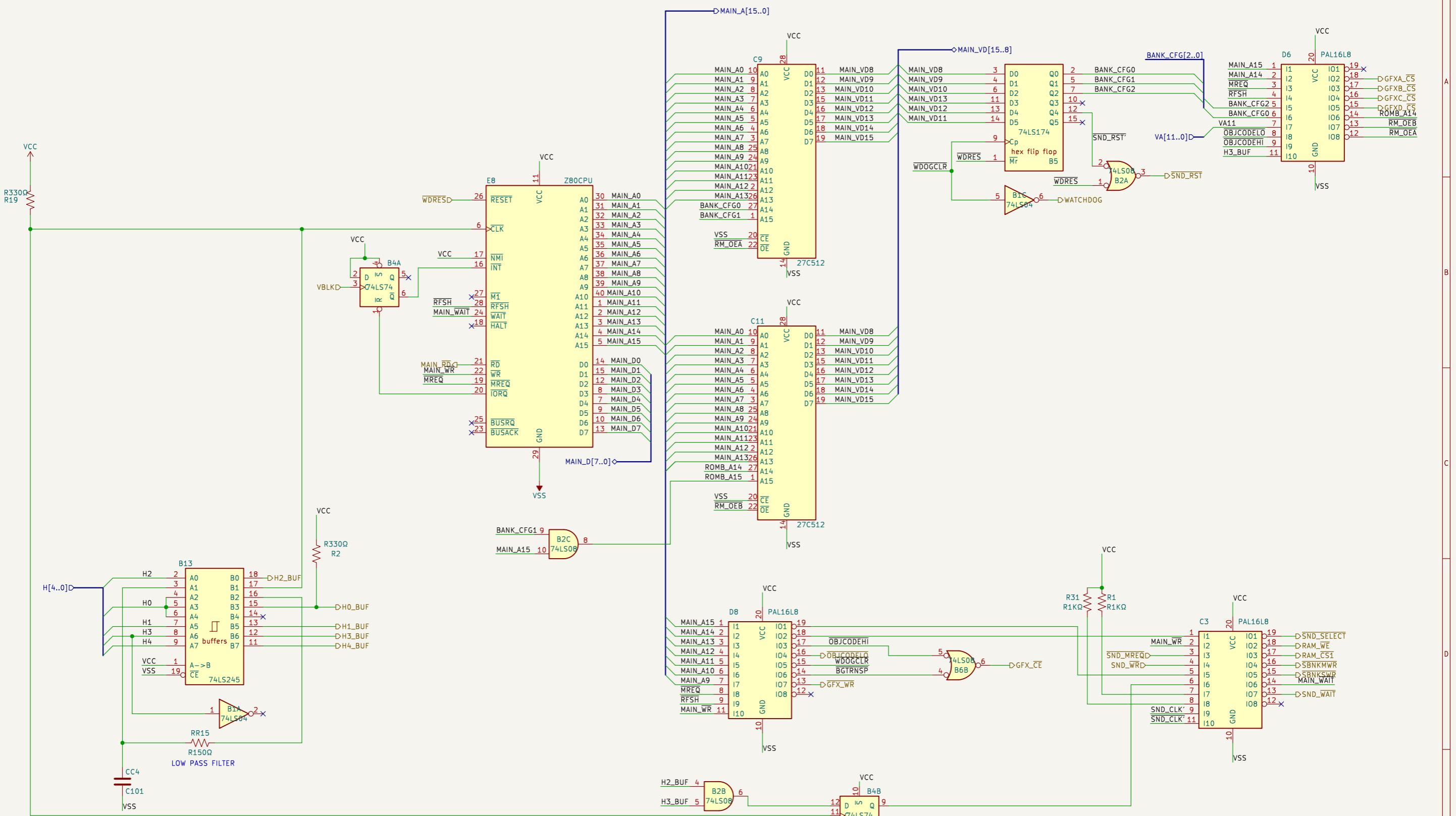
Title: EXTERMINATION

Size: A3 Date: 29/08/2022
KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1

Rev: José Tejada G. Id: 2/10



1 2 3 4 5 6 7 8



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Sheet: /main/
File: main.kicad_sch

Title: EXTERMINATION

Size: A3	Date: 29/08/2022	Rev: José Tejada G.
KiCad E.D.A. kicad-cliv 7.0.10-7.0.10-ubuntu20.04.1		Id: 3/10



A

A

B

B

C

C

D

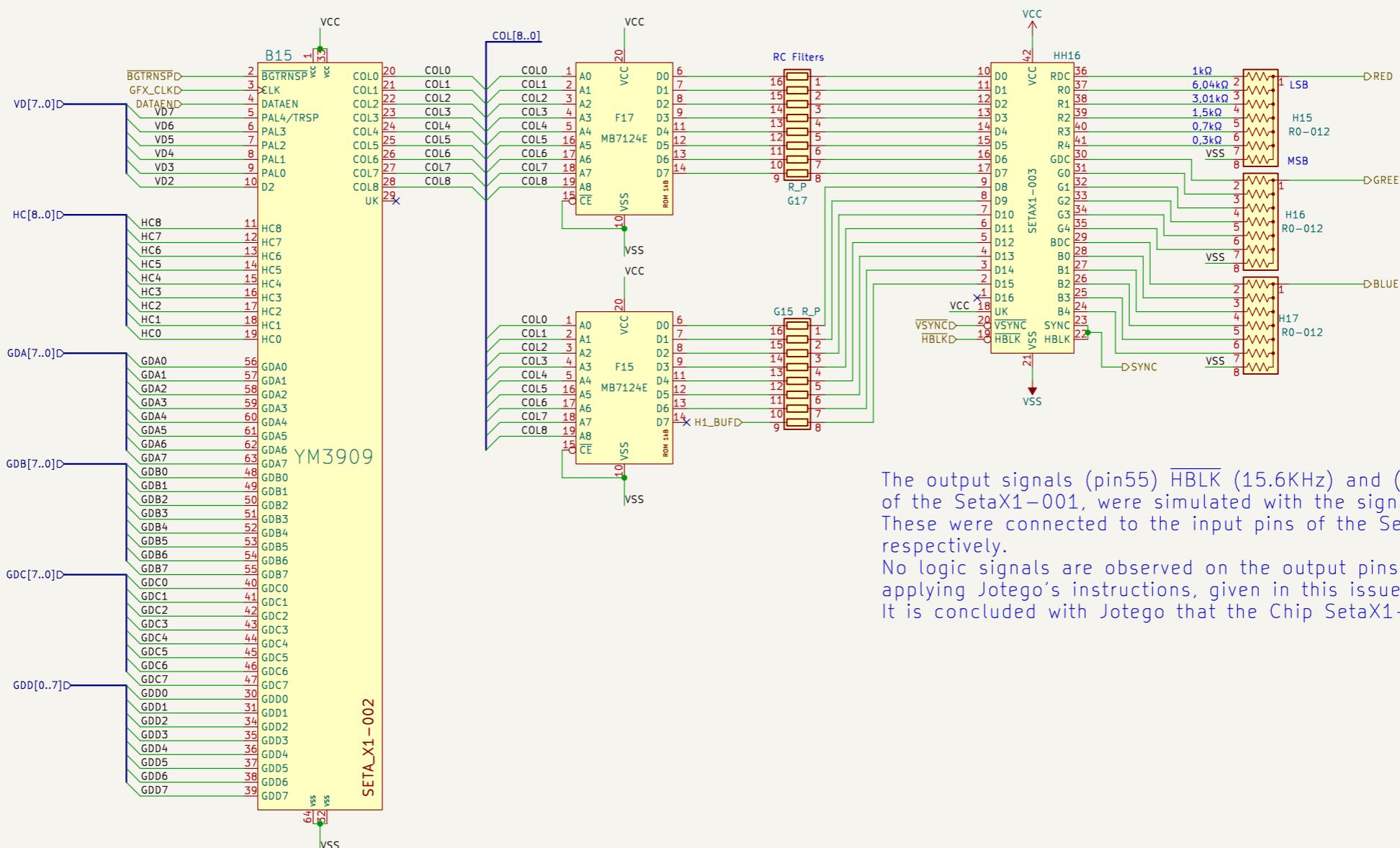
D

E

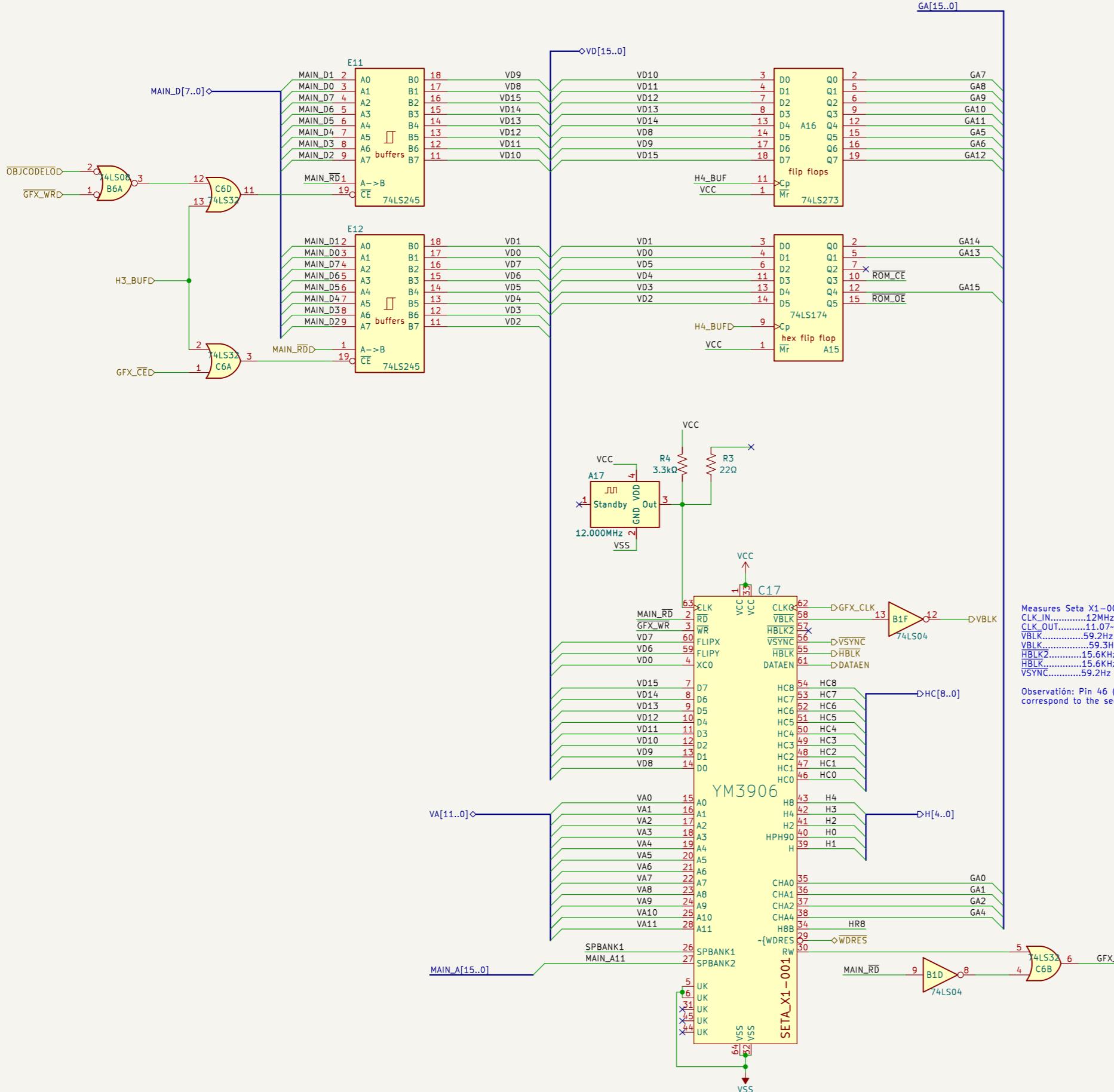
E

F

F

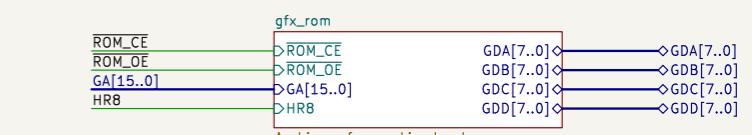


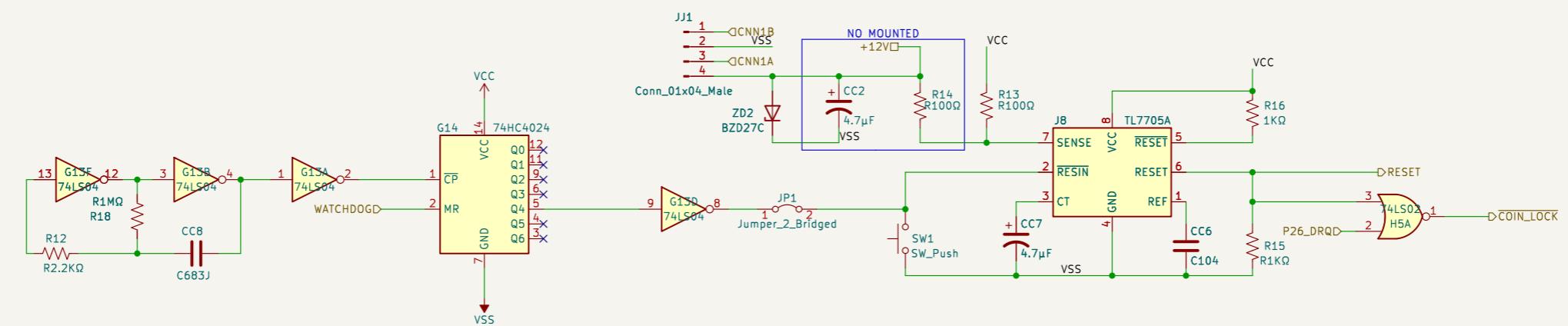
The output signals (pin 55) HBLK (15.6KHz) and (pin 56) VSYNC (59.2 Hz) of the SetaX1-001, were simulated with the signal generator and an inverter. These were connected to the input pins of the Setax01-003 (pin 19 – 20), respectively.
 No logic signals are observed on the output pins (22–23) HBLK – SYNC, applying Jotego's instructions, given in this issue.
 It is concluded with Jotego that the Chip SetaX1-001 is broken.



Measures Seta X1-001:
 CLK_IN.....12MHz
 CLK_OUT.....11.07-12.01MHz
 VBLK.....59.2Hz
 VBLK.....59.3Hz
 HBLK2.....15.6kHz
 HBLK.....15.6kHz
 HBLK.....15.6kHz
 VSYNC.....59.2Hz

Observación: Pin 46 (HCO) does not correspond to the sequence of the HC[8..0] counter.





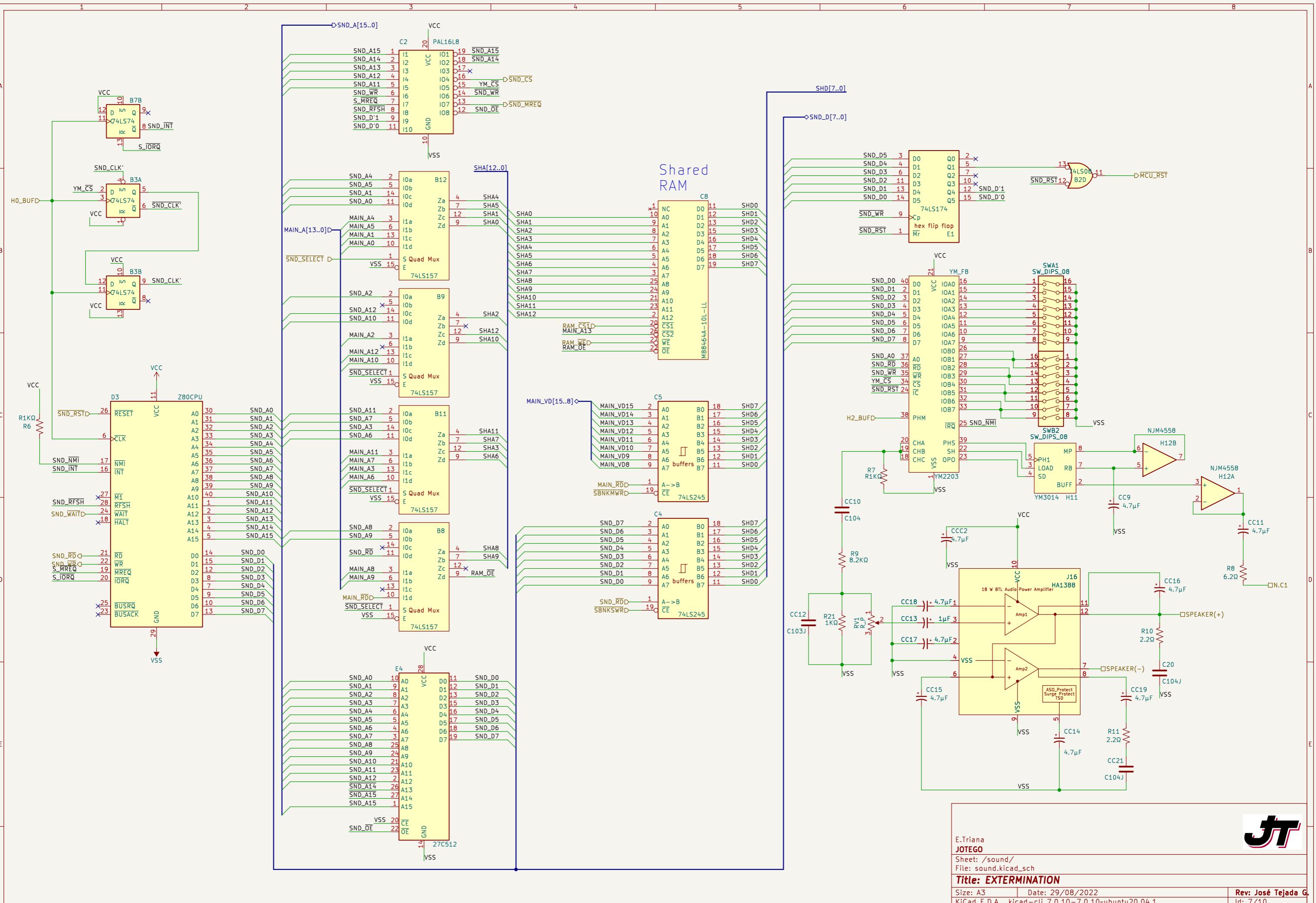
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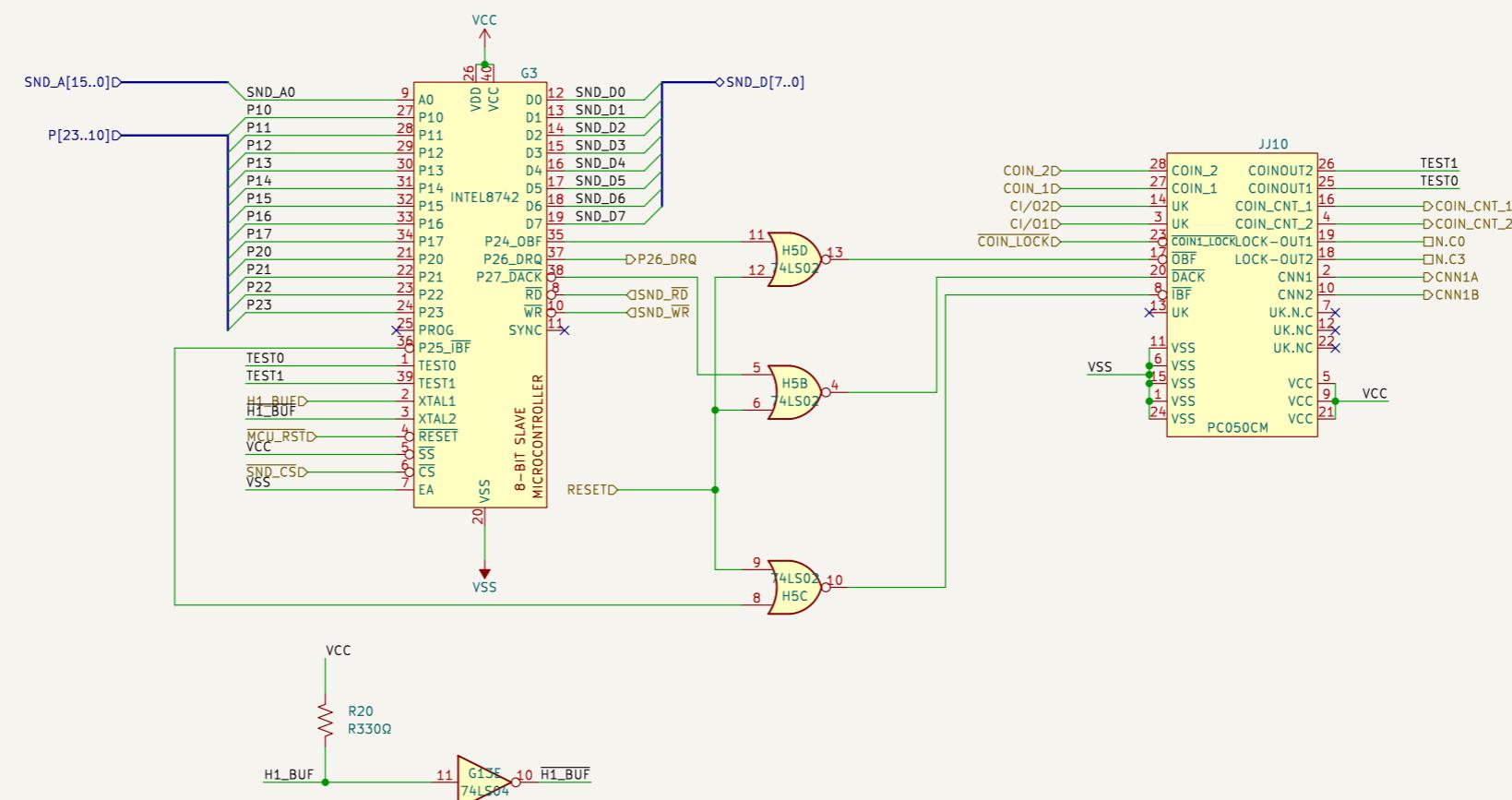
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File: watchdog.kicad_sch

Title: EXTERMINATION

Size: A3 Date: 29/08/2022
KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1







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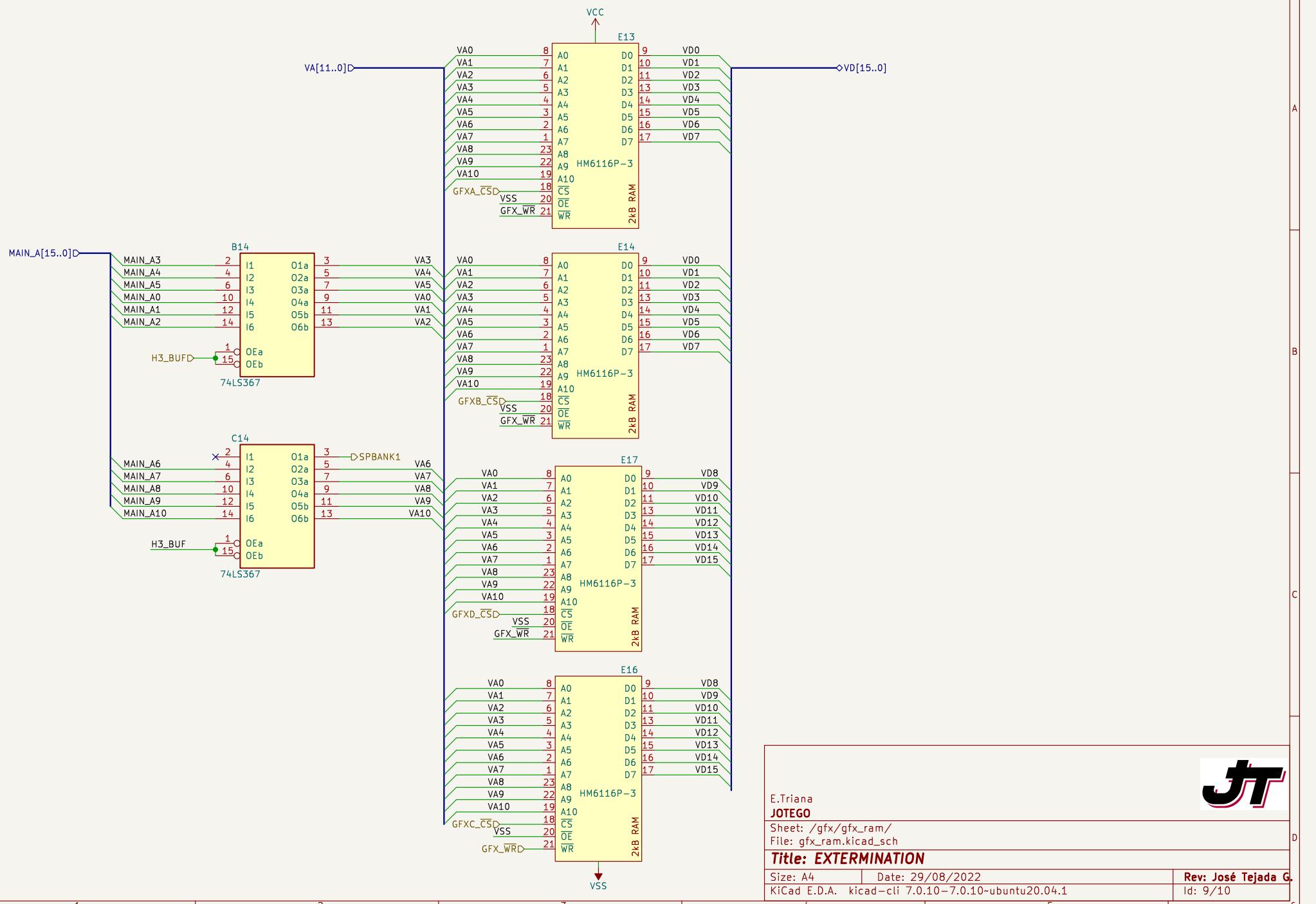


Sheet: /mcu/
File: mcu.kicad_sch

Title: EXTERMINATION

Size: A3 | Date: 29/08/2022
KiCad E.D.A. kicad-cll 7.0.10-7.0.10-ubuntu20.04.1

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Sheet: /gfx/gfx_ram/
File: gfx_ram.kicad_sch

Title: EXTERMINATION

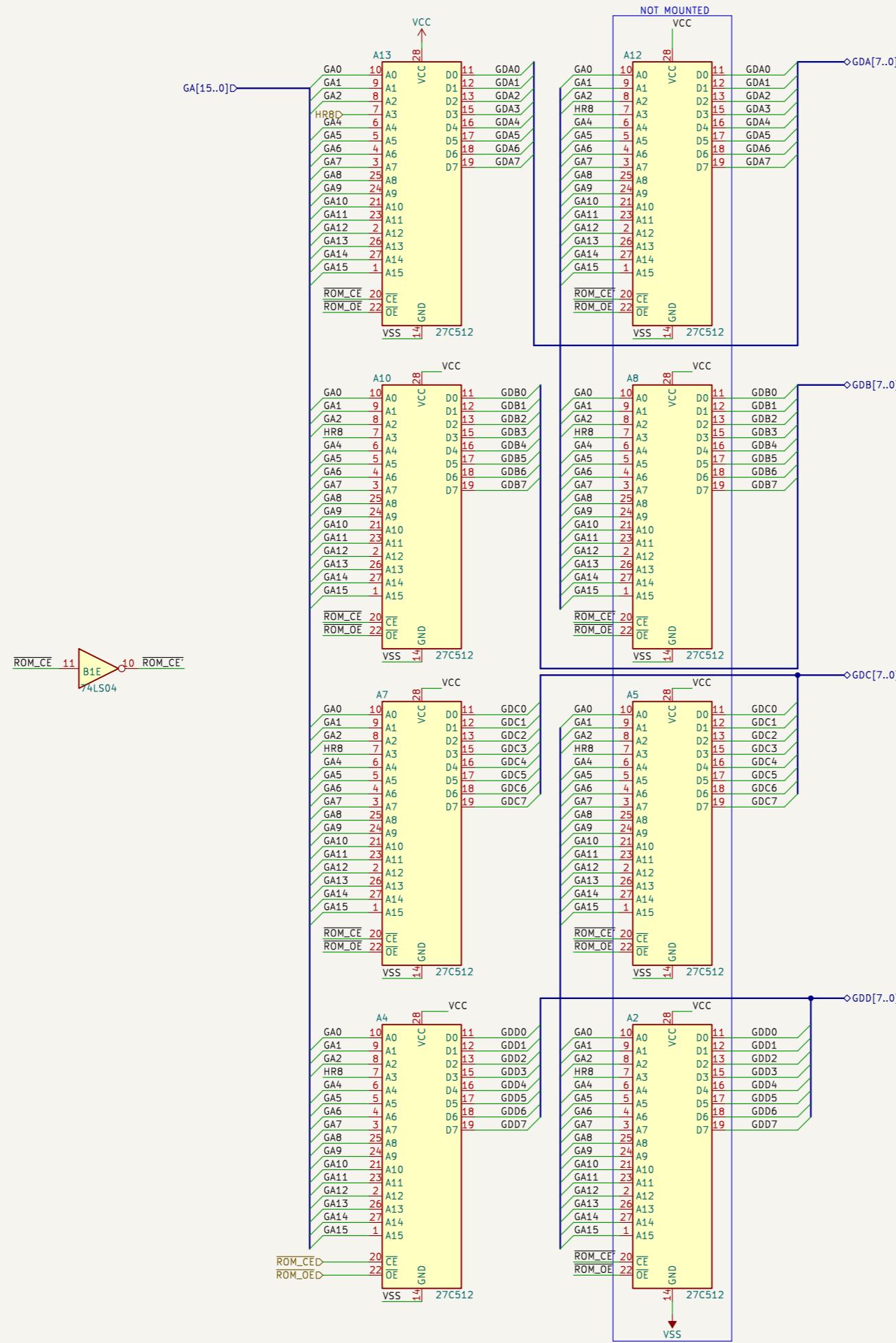
Size: A4 Date: 29/08/2022

KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1



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Sheet: /gfx/gfx_rom/
File: gfx_rom.kicad_sch

Title: EXTERMINATION

Size: A3 Date: 29/08/2023

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