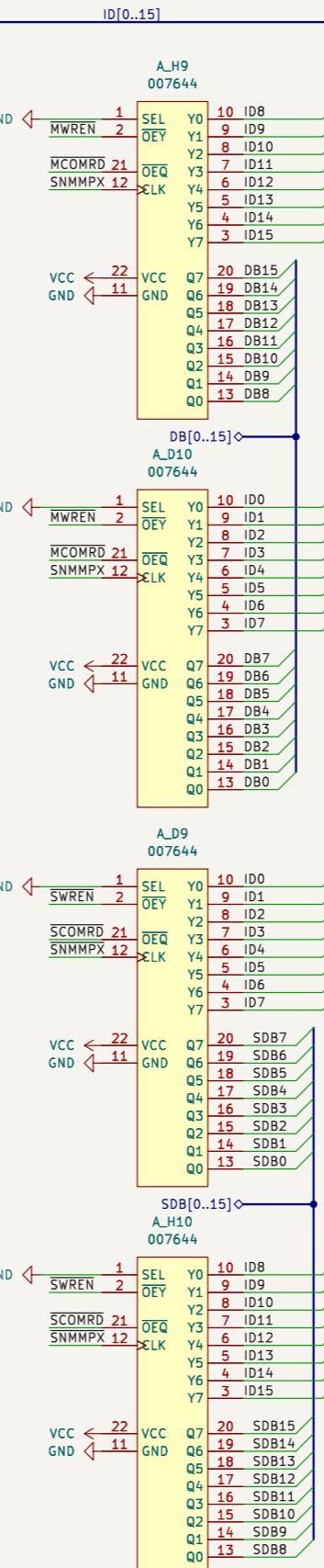
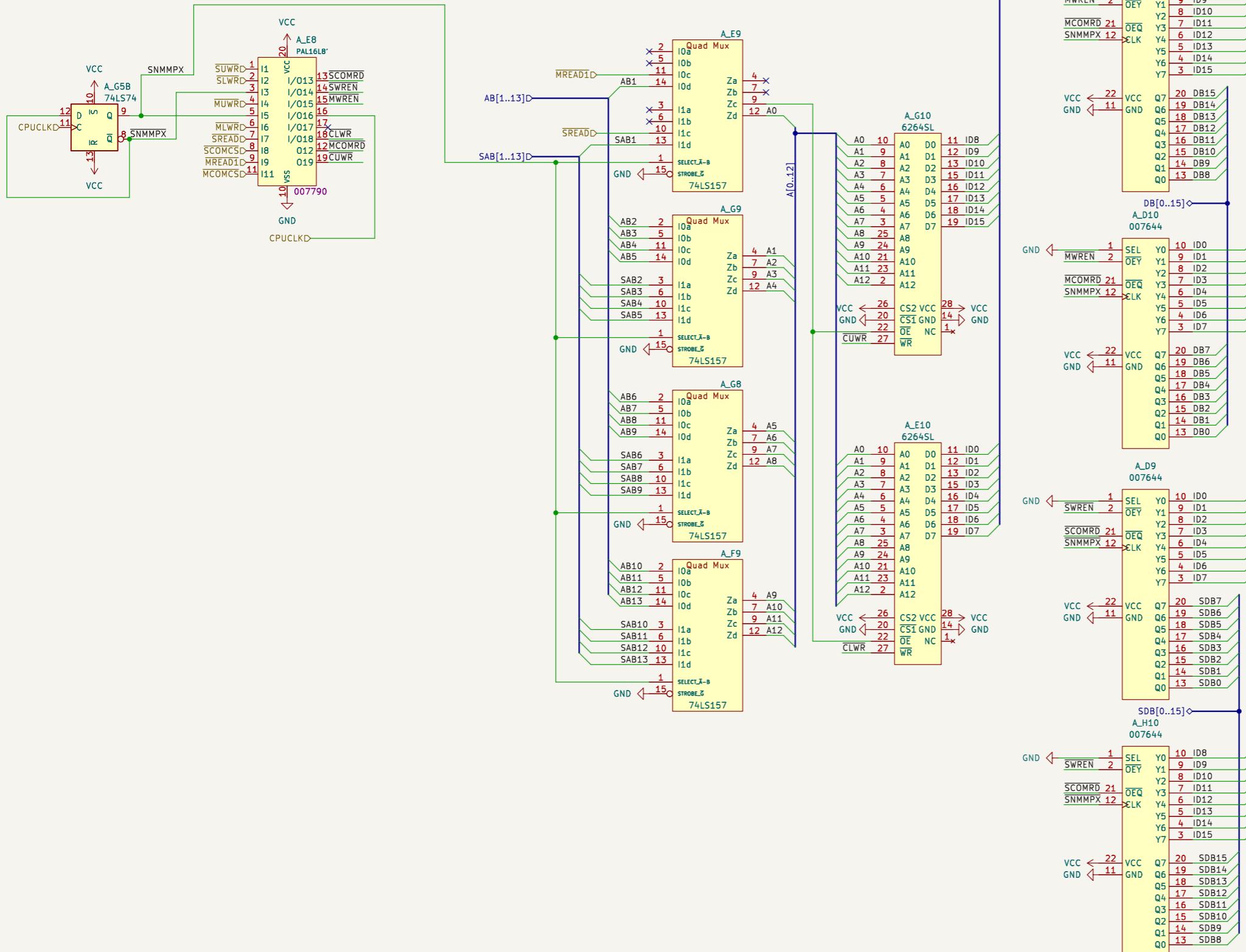


Konami 007790

$MCOMRD = \neg(MREAD1 \& \neg MCOMCS) = MREAD1 \mid MCOMCS$   
 $SCOMRD = \neg(SREAD \& \neg SCOMCS)$   
 $SWREN = \neg(SNMMPPX \& SREAD \& \neg SCOMCS)$   
 $MWREN = \neg(SNMMPPX \& MREAD1 \& \neg MCOMCS)$   
 $CLWR = \neg(CLWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$   
 $CUWR = \neg(CUWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg MUWR \& \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$

A All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16LB device it is kept in that form. The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.  
Pin 2 = OEY – Output enable for the Y outputs else they are inputs. Active LOW  
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW  
Pin 12 = CLK – Clock input

Pins 3–10 = Y outputs – normal outputs. If OEQ is LOW these pins become outputs mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.  
Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs. If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs. If SEL is LOW then the outputs will only change state on a rising edge CLK.

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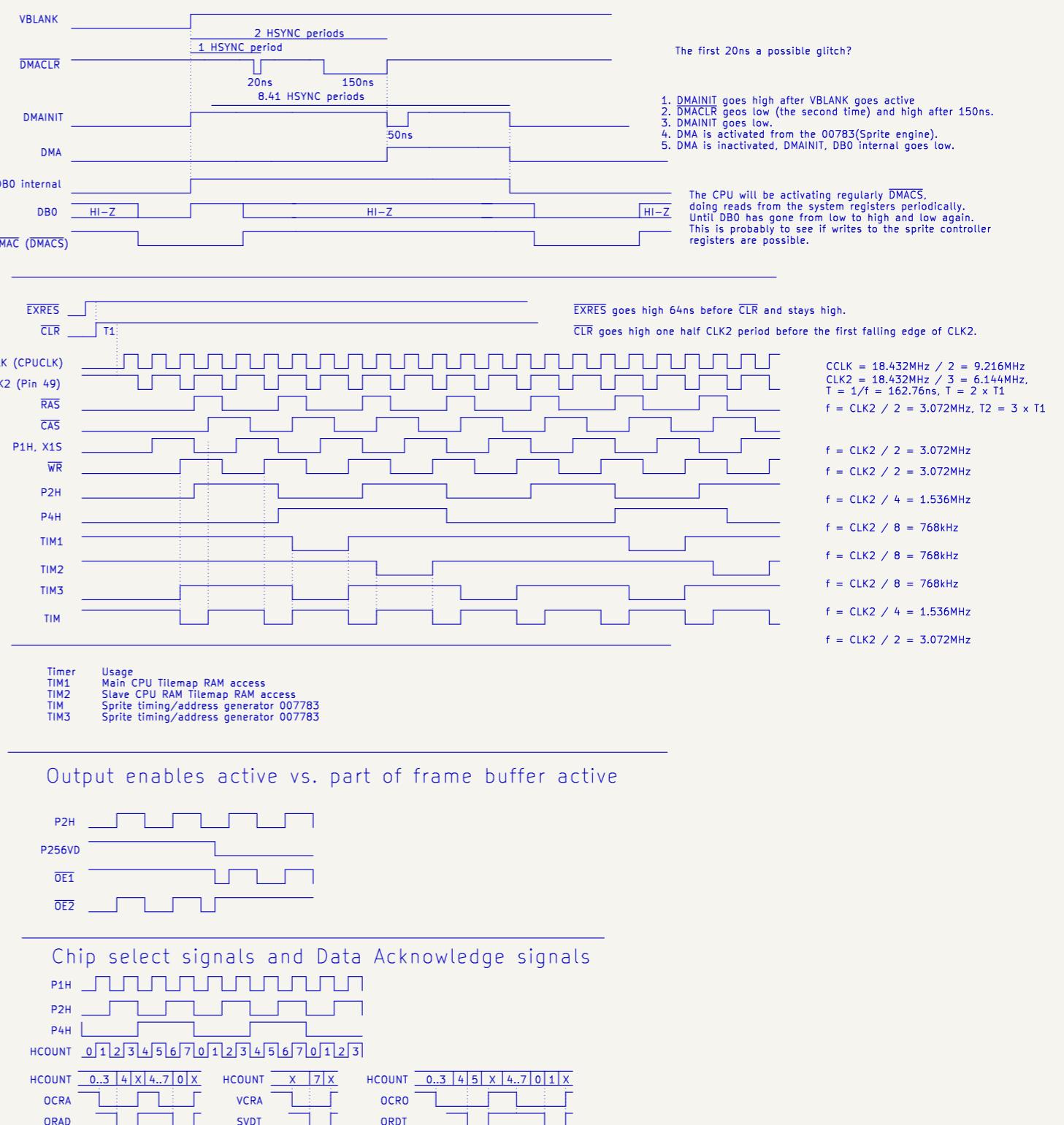
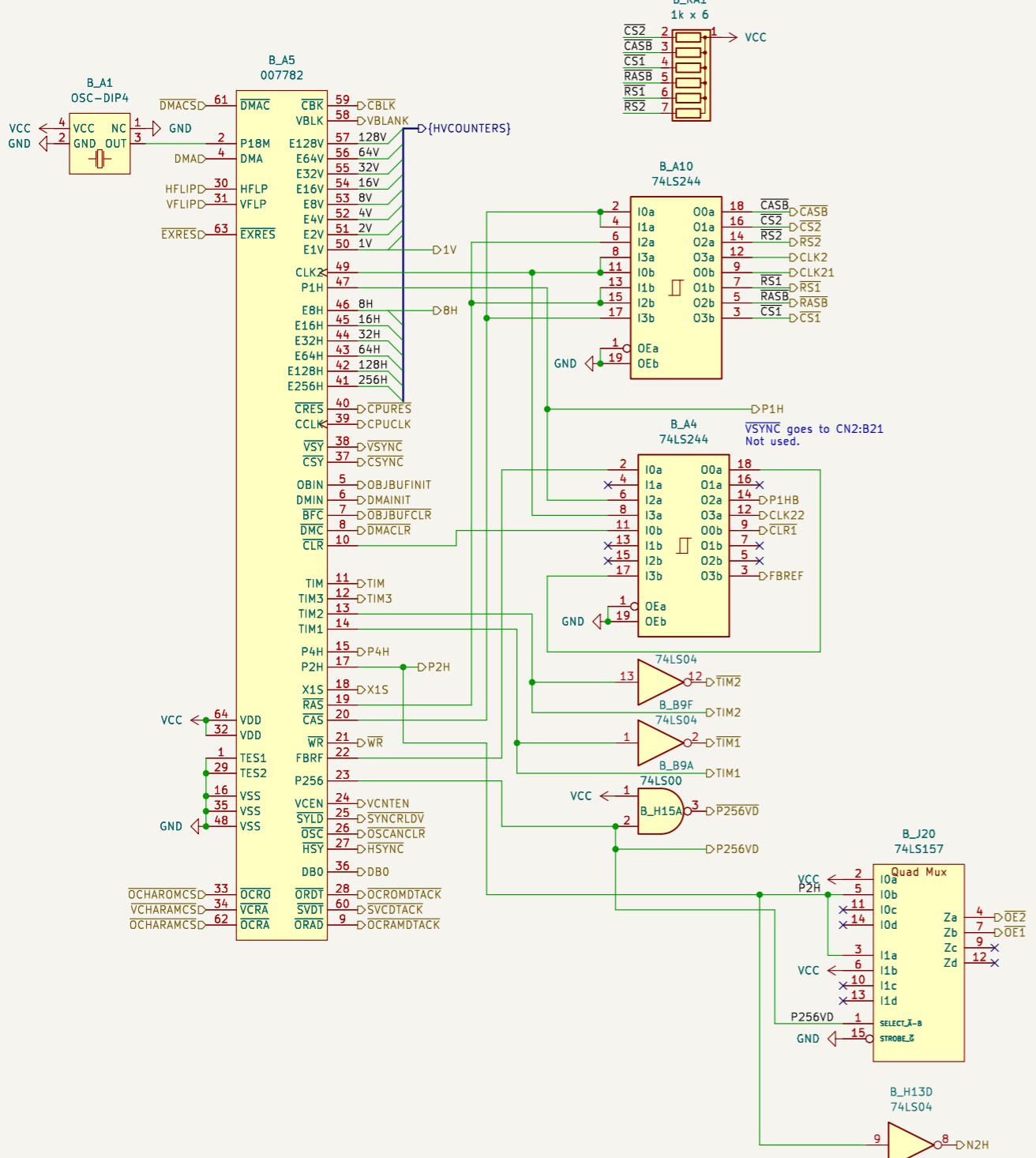
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## DMA Synchronization

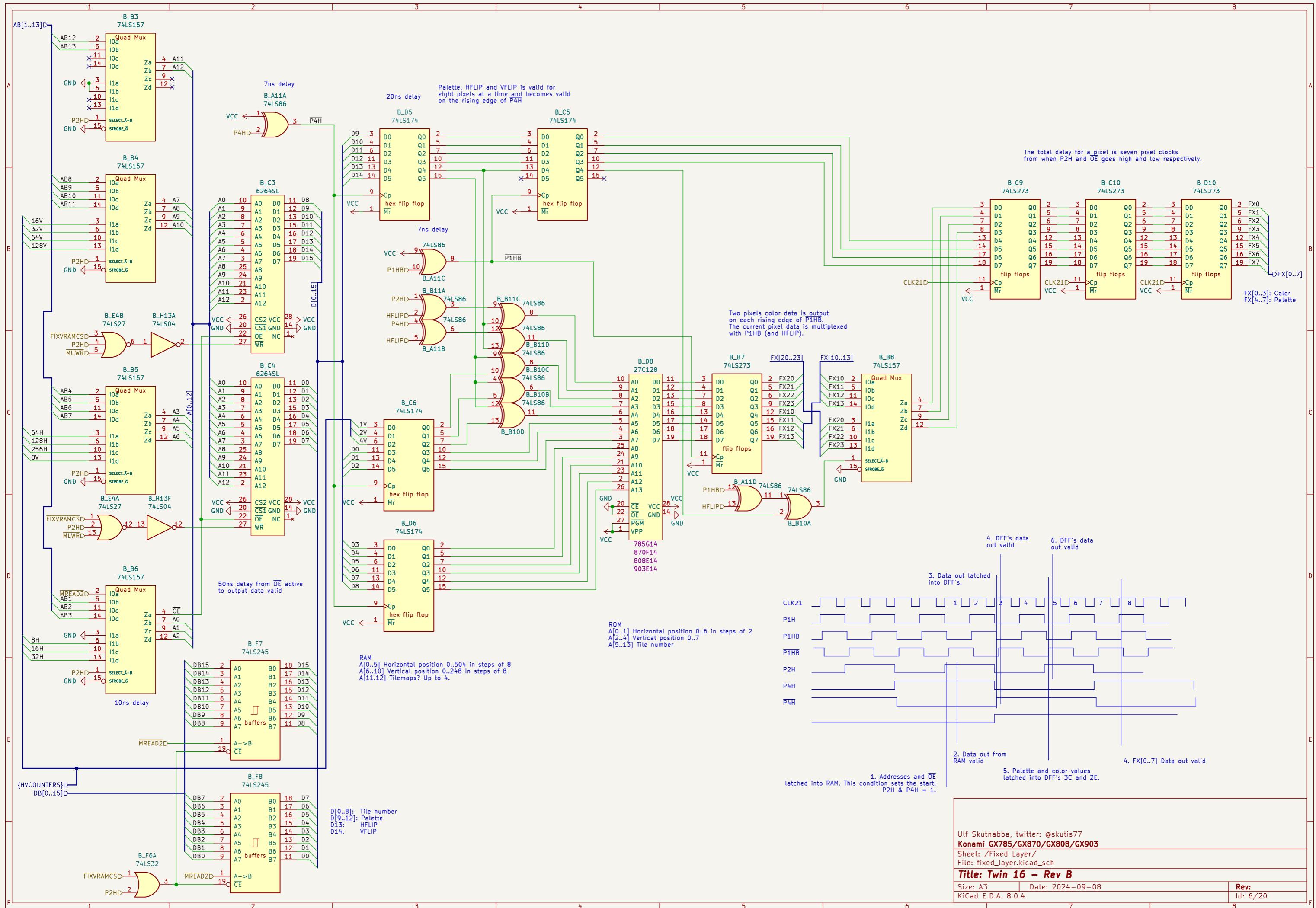


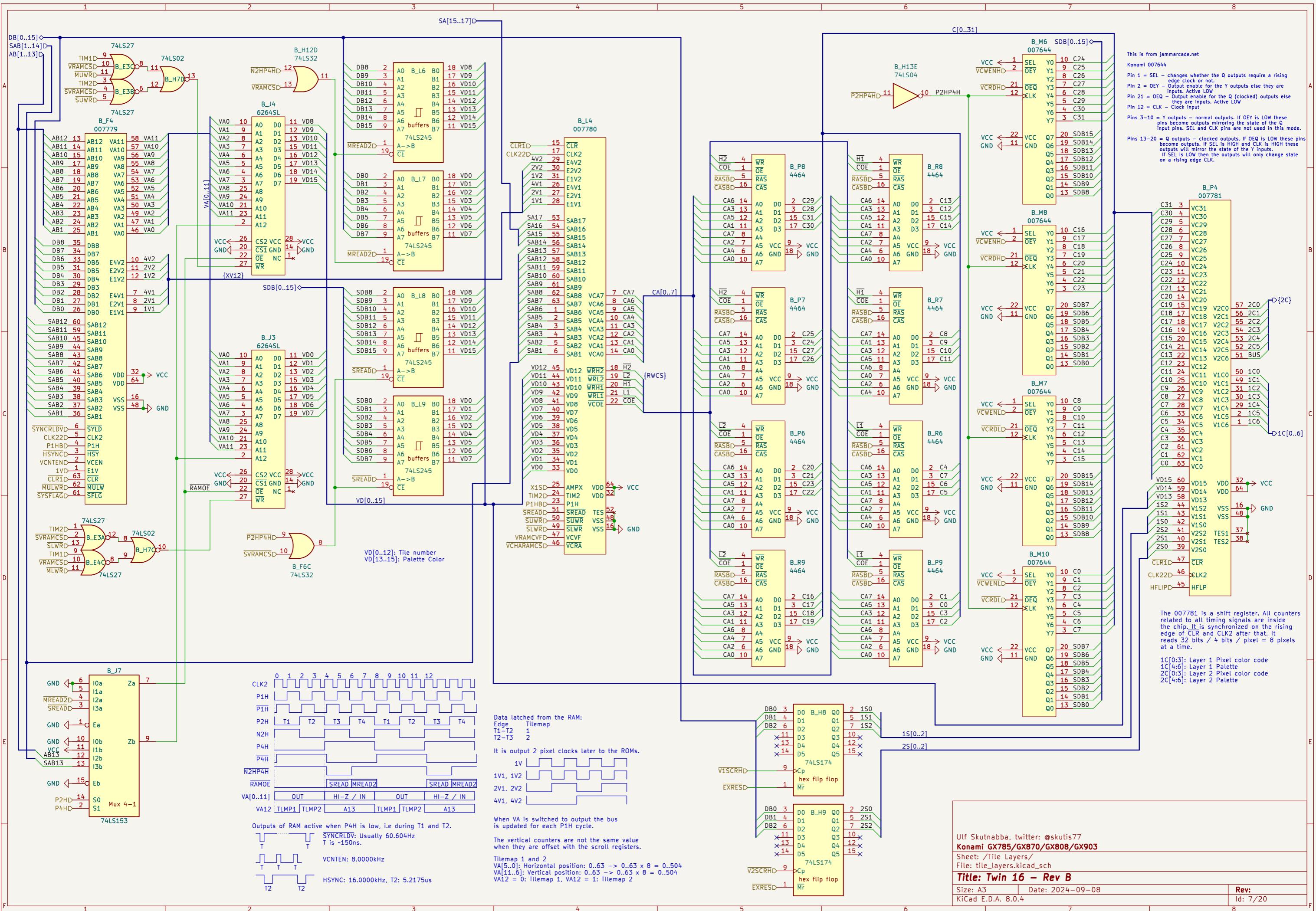
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**Konami GX785/GX870/GX808/GX903**  
Sheet: /Timing/  
File: timing.kicad\_sch

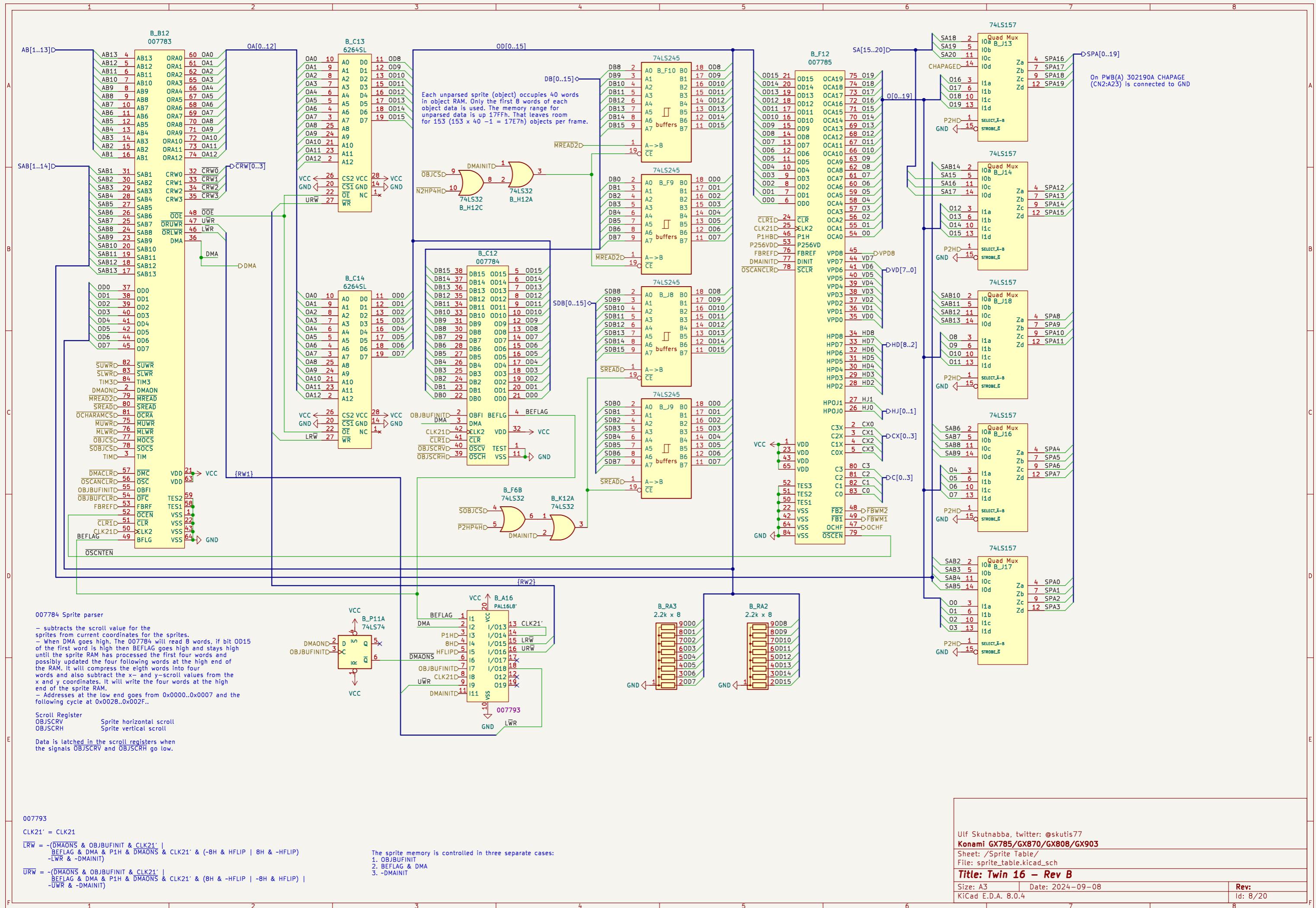
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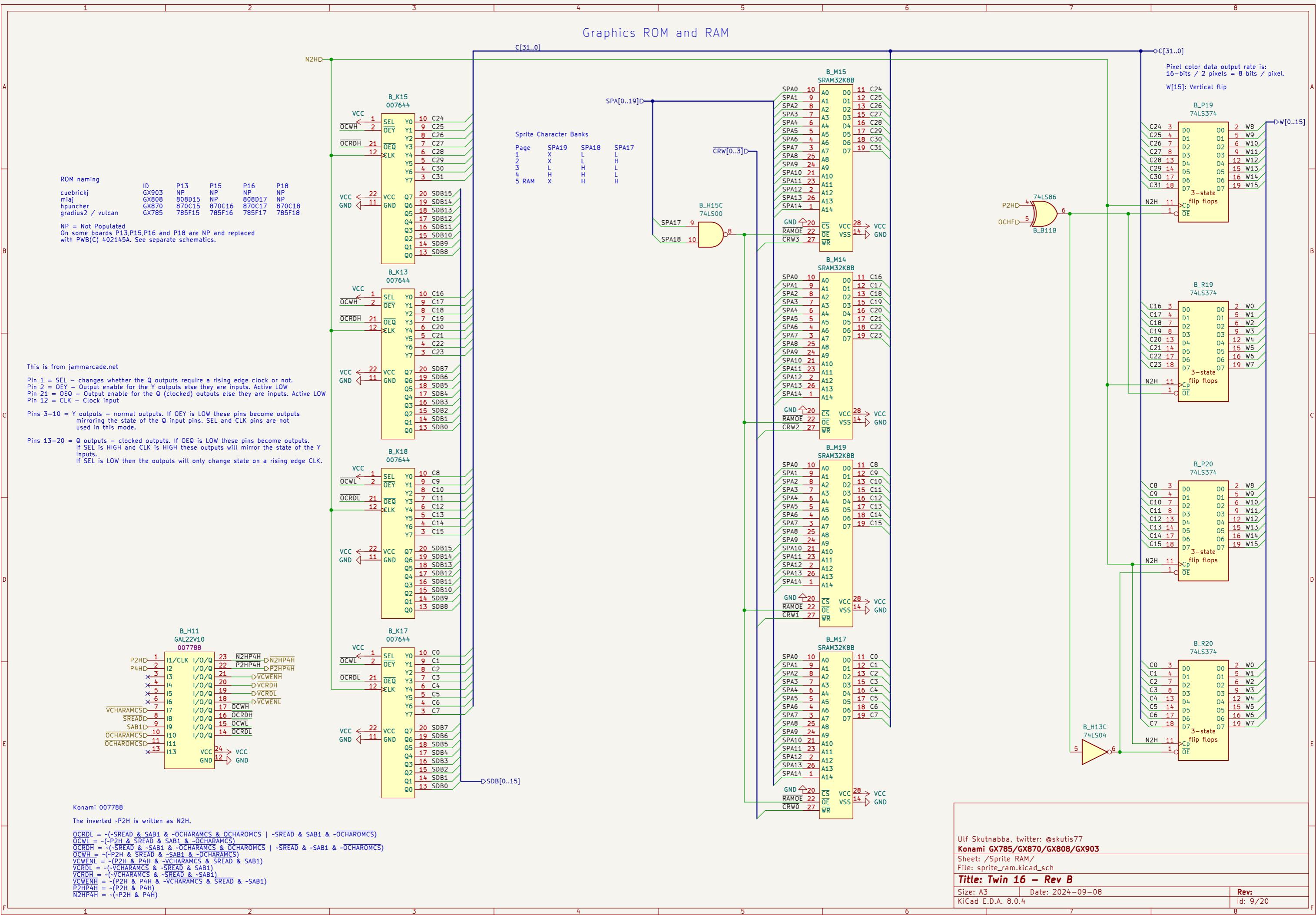
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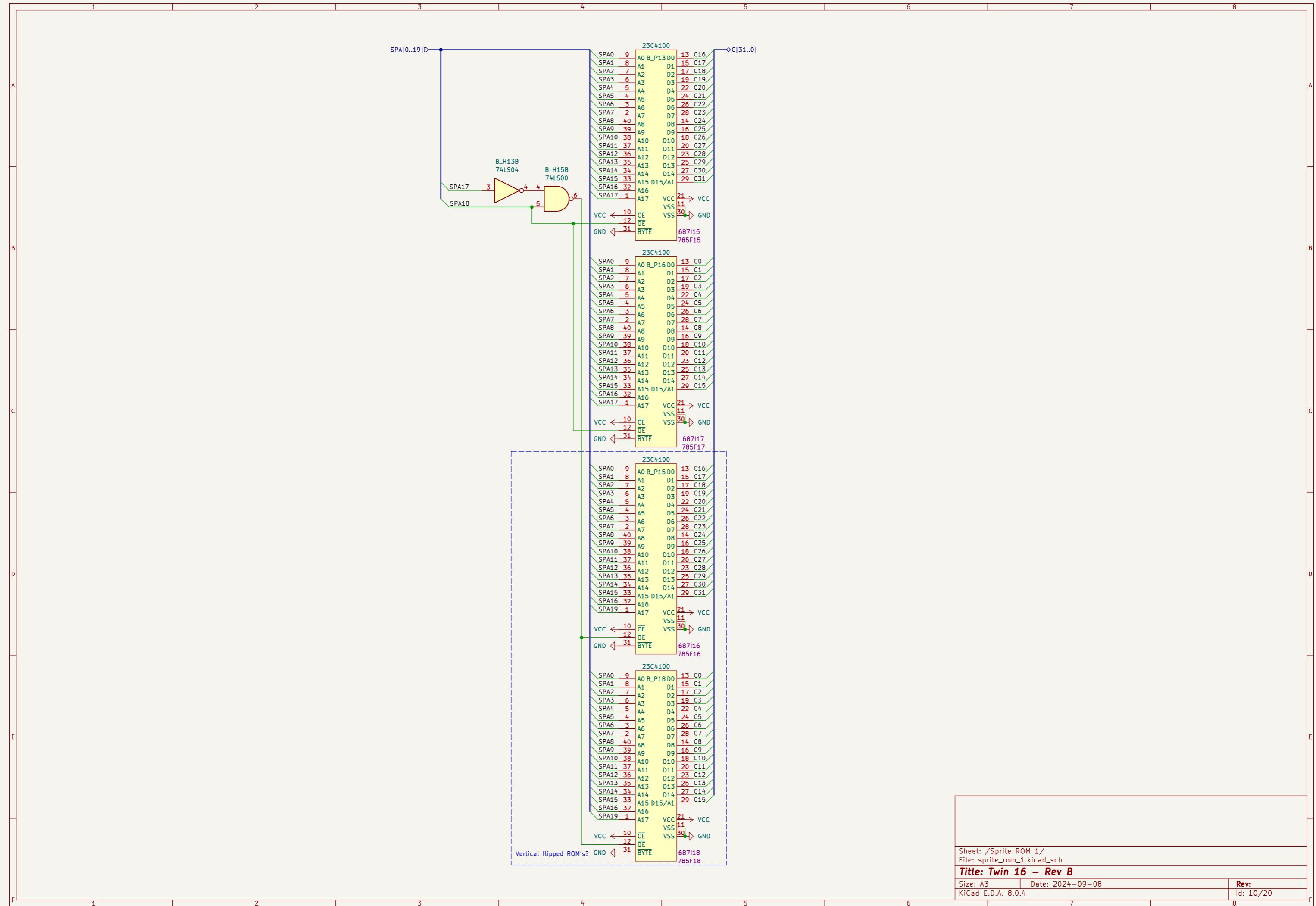


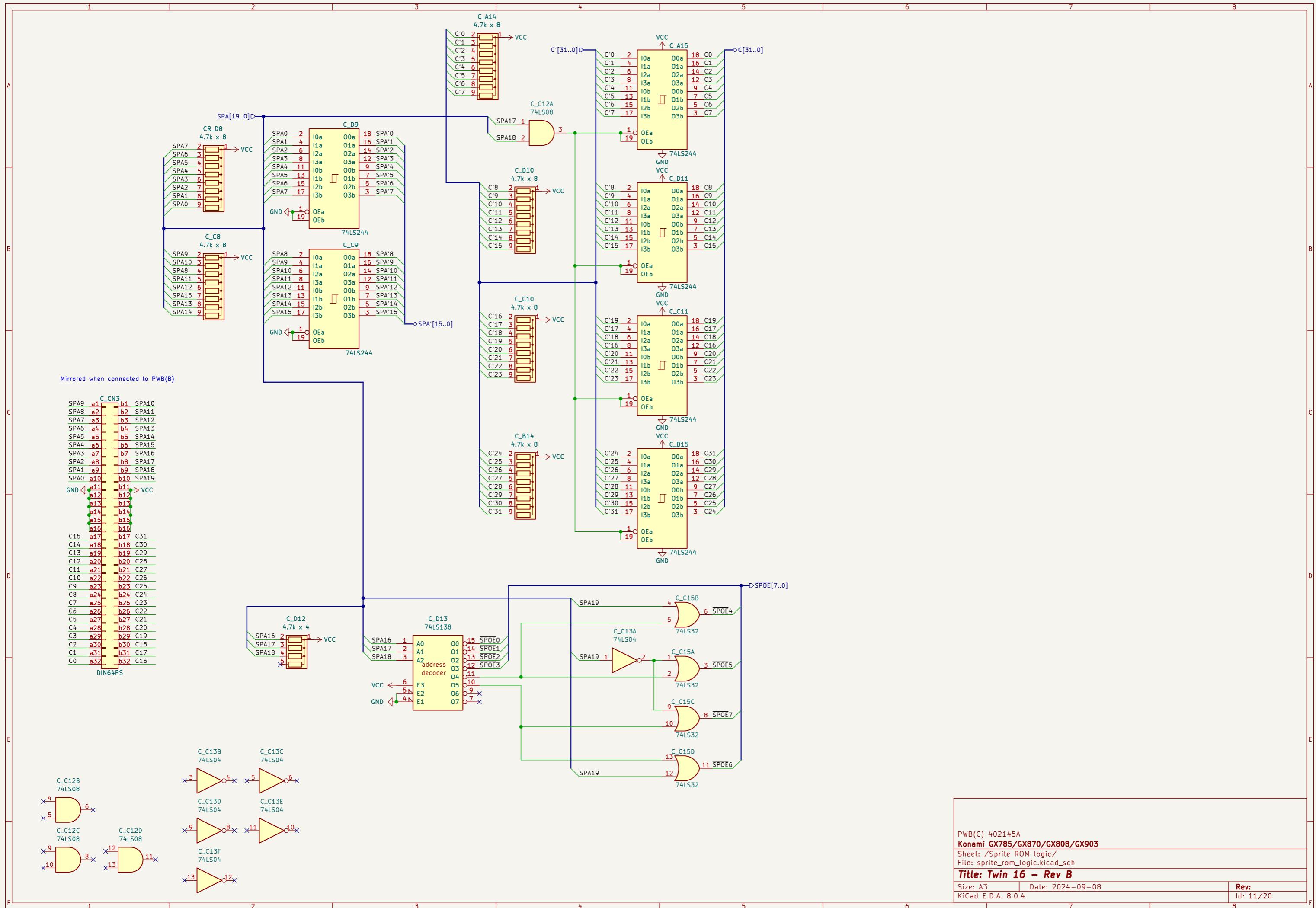


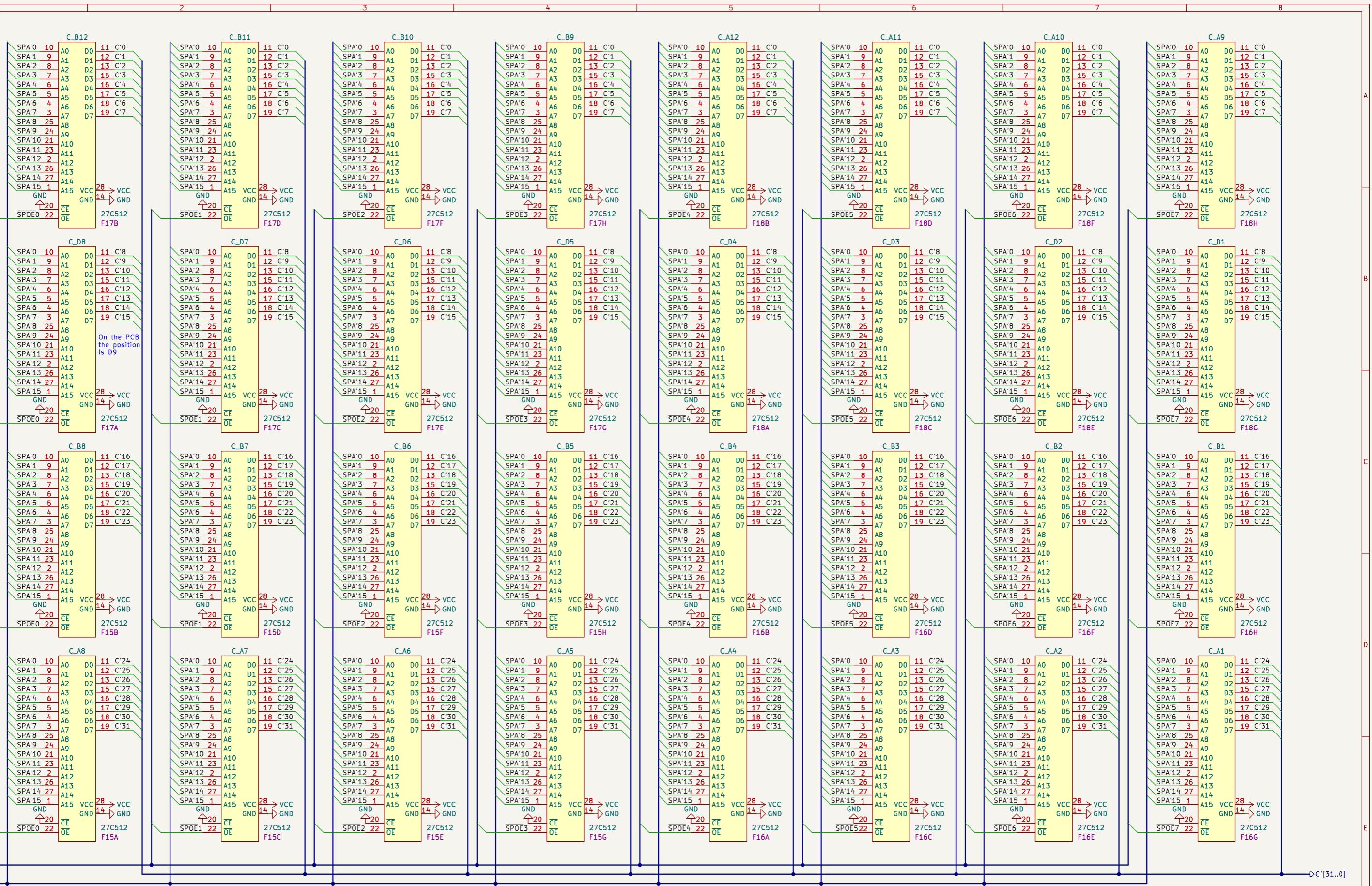


## Graphics ROM and RAM









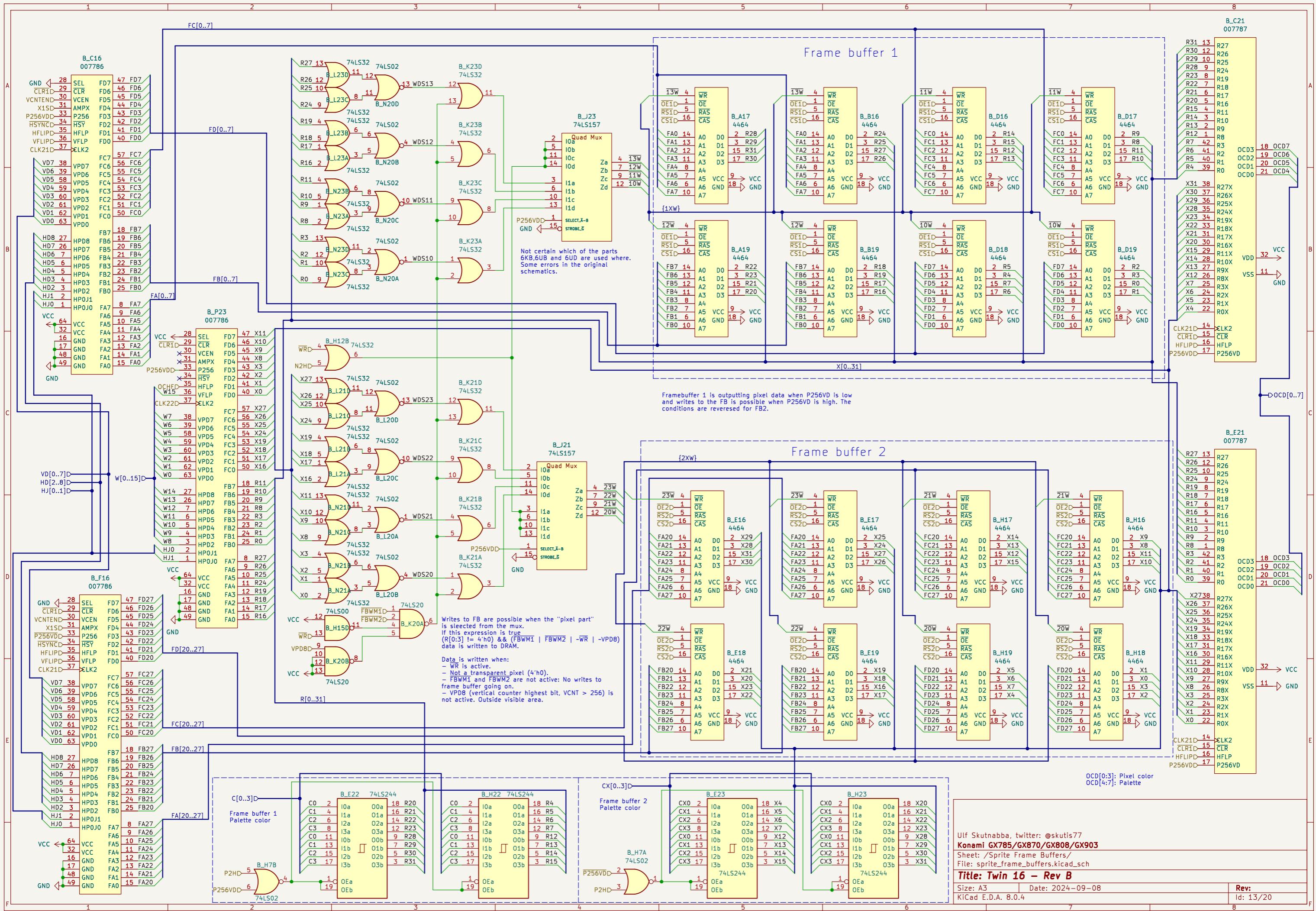
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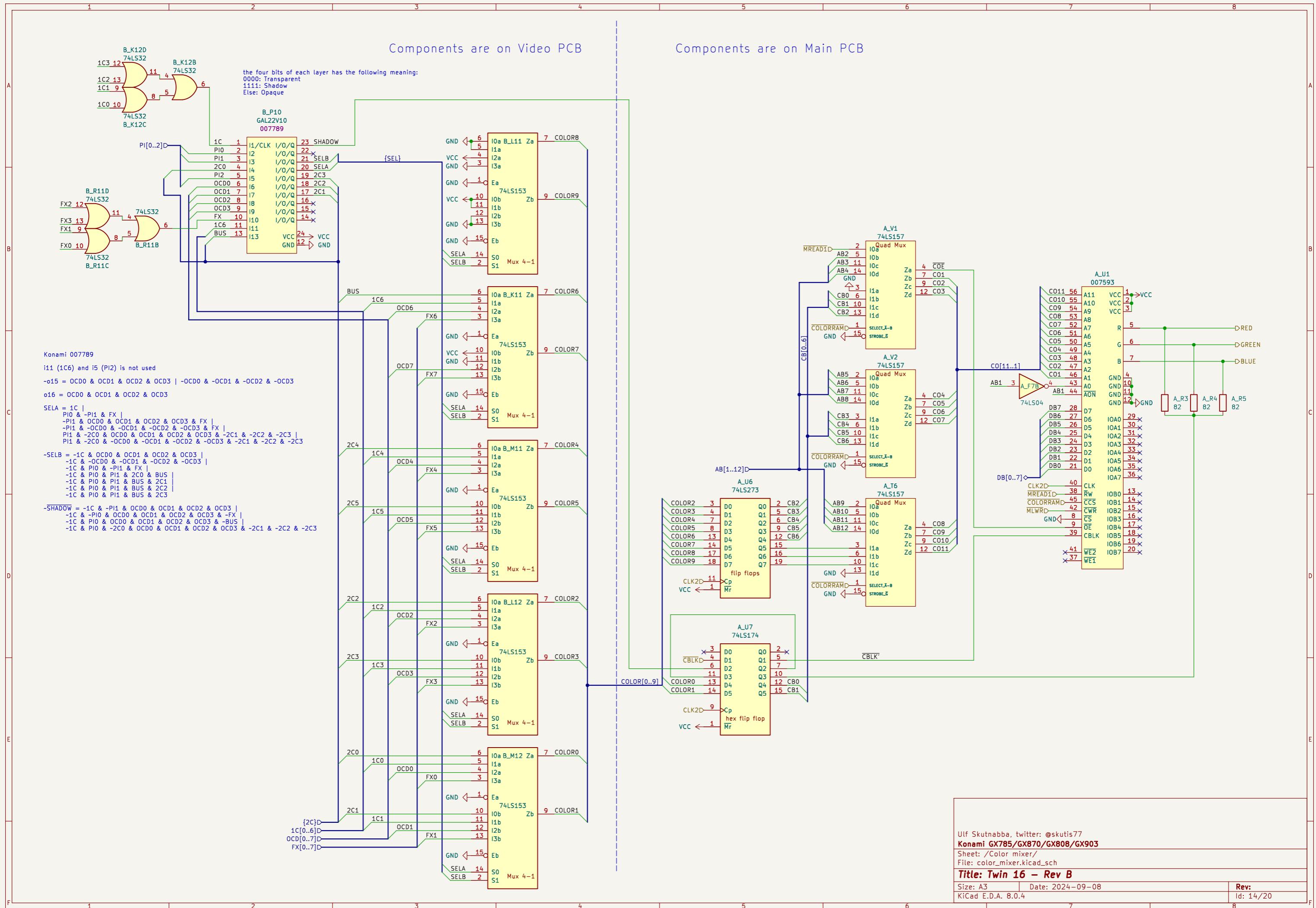
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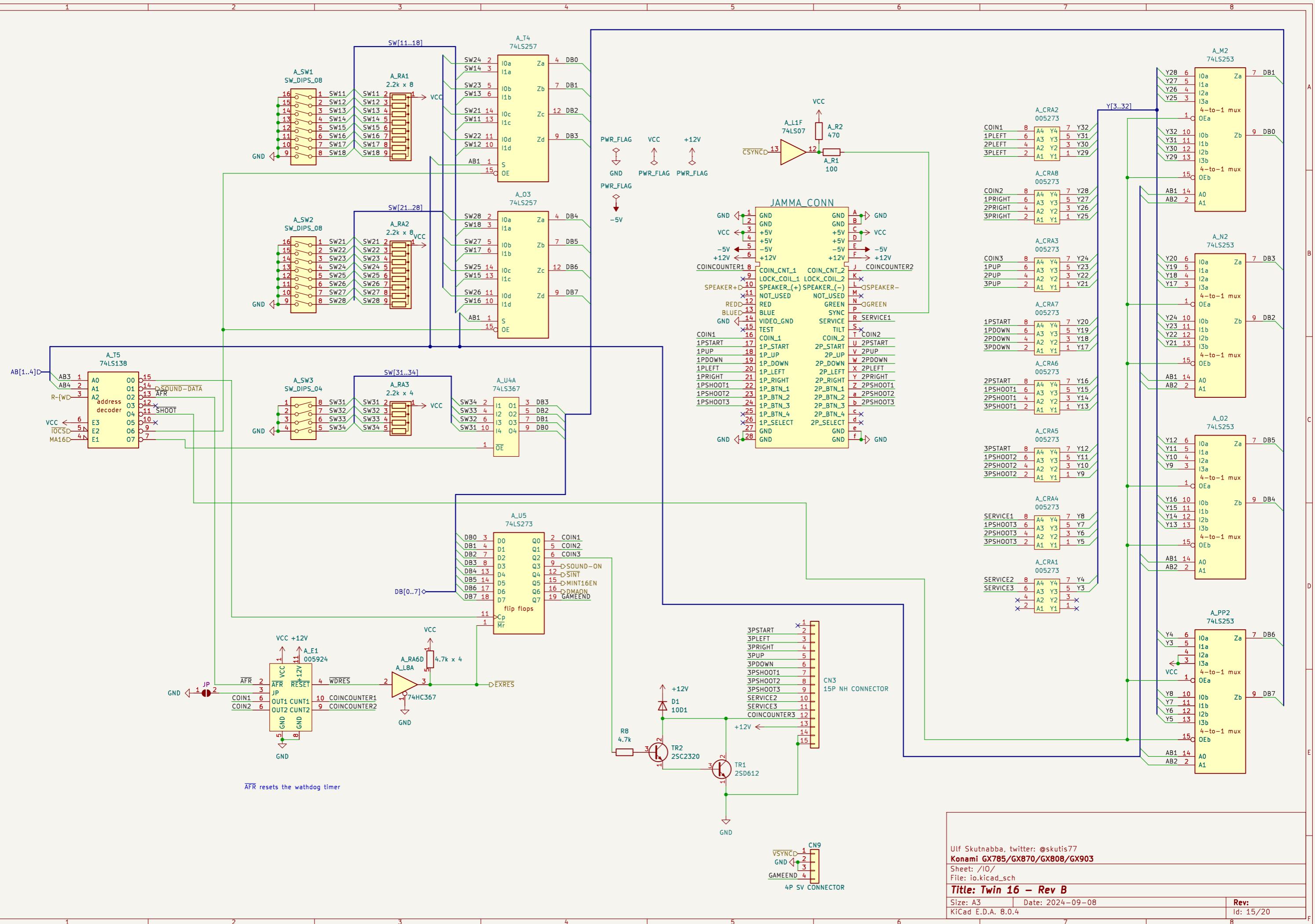
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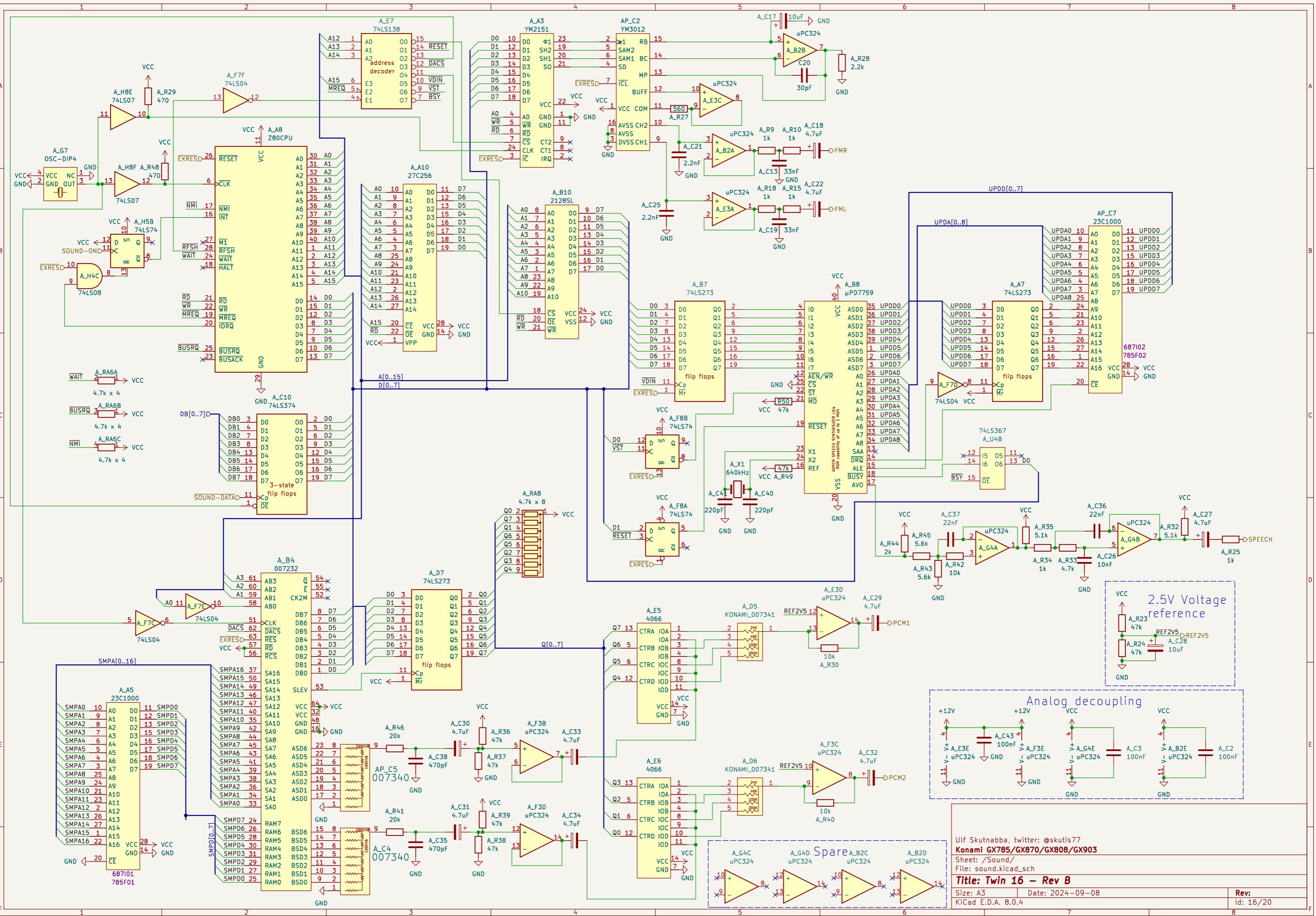
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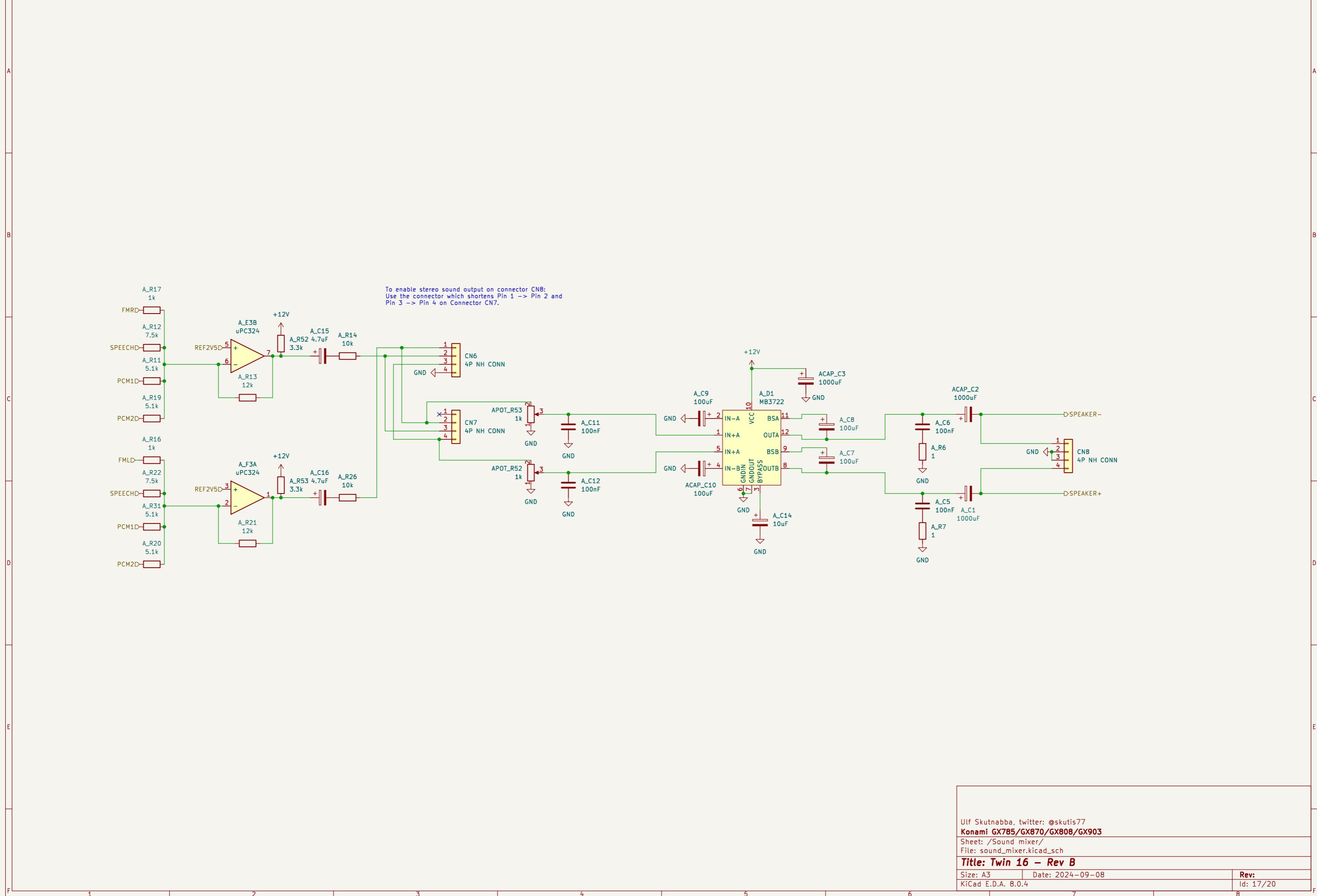








1 2 3 4 5 6 7 8



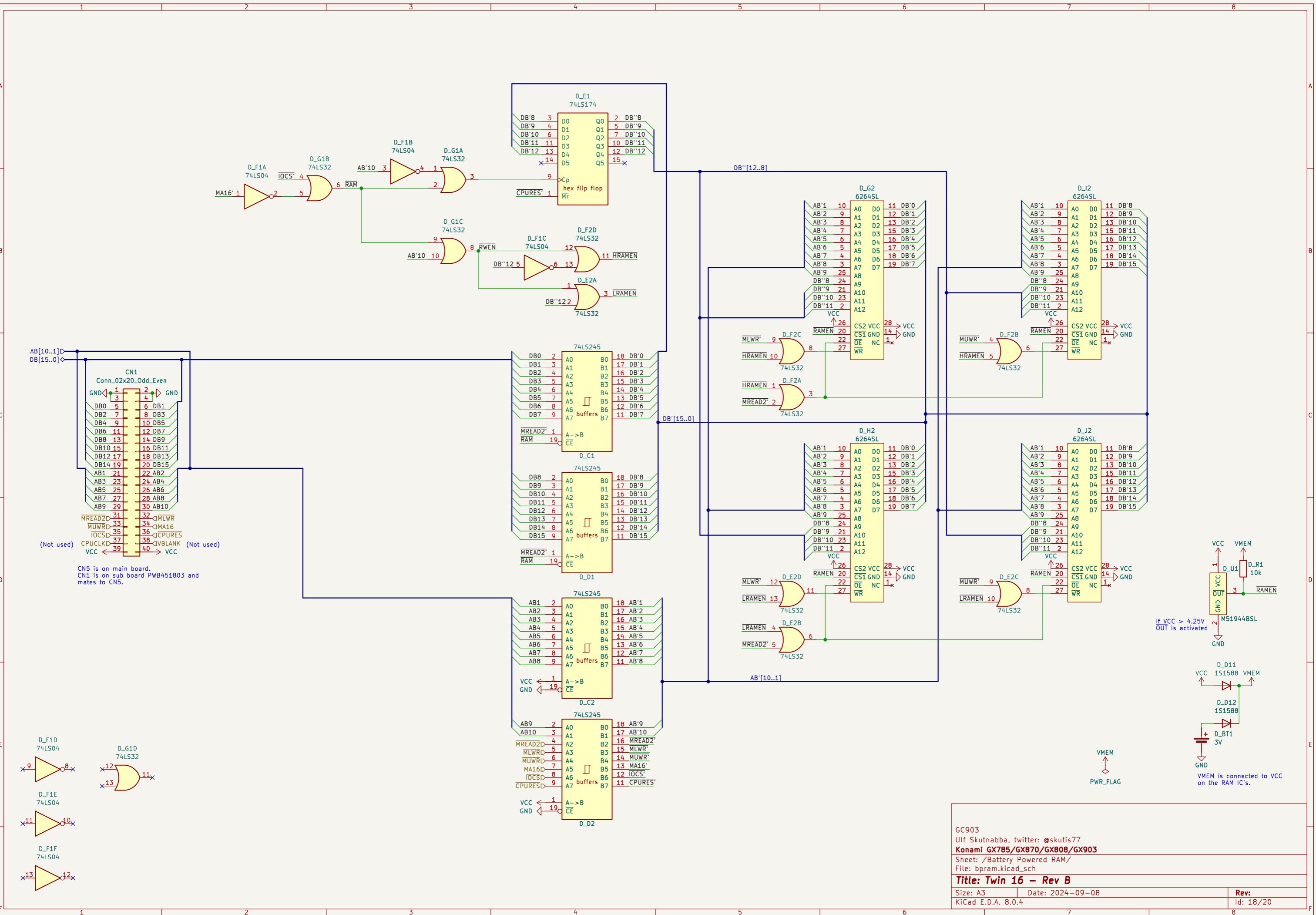
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Sheet: /Sound mixer/  
File: sound\_mixer.kicad\_sch

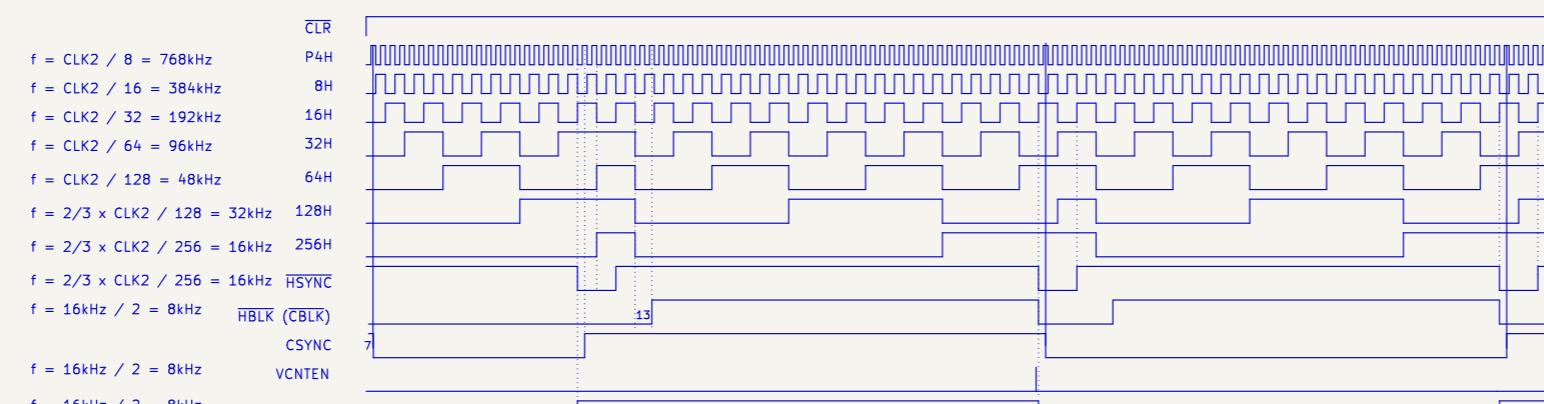
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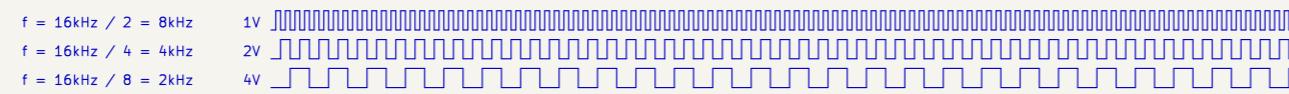
## Horizontal signals



– The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals



Every 16th pulse is long.  
Every 8th pulse is long.  
Every 4th pulse is long.  
Every 2nd pulse is long.  
High period is longer

VBLANK High:  $7 \times 16 \times 2 = 224$ , Low:  $5 \times 4 \times 2 = 40$   
SYNCRLDV goes low 140ns before FBREF goes low.  
SYNCRLDV goes high again when FBREF goes low.

OBJBUFCLR goes low one pixel clock before the rising edge  
of VBLANK and high again when VBLANK goes high.

60.606Hz, OSCANCLR goes low for 140ns ~ One pixel clock cycle.  
P256VD goes high/low one  
P4H cycle (8 pixels) after VSYNC goes high.

FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

## Horizontal and vertical synch timing diagrams

Pixel clock CLK2 =  $18.432\text{MHz} / 3 = 6.144\text{MHz}$

Horizontal lines

HSYNC freq =  $6.144\text{MHz} / 384 = 16\text{kHz}$

HSYNC period =  $1 / 16\text{kHz} = 62.5\text{us}$

Pixels / line: 384

Active pixels: 320

Blank pixels: 64

Vertical lines

VSYNC freq =  $16\text{kHz} / 264 = 60.606060\text{Hz}$

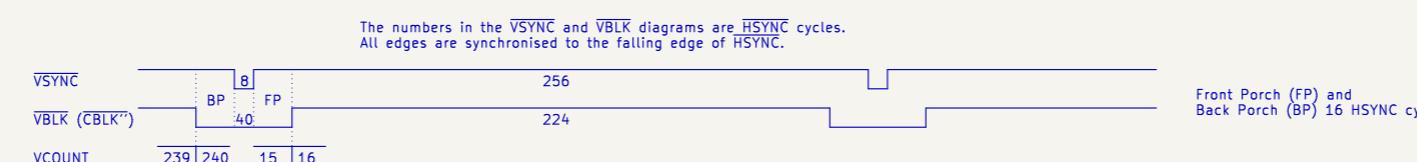
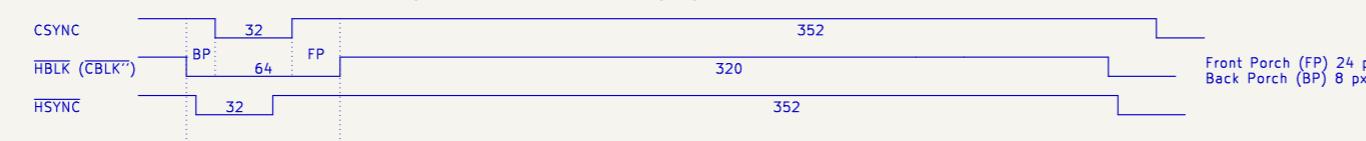
VSYNC period =  $1 / f = 264 / 16\text{kHz} = 16.5\text{ms}$

scanlines / frame: 264

Active lines: 224

Blank lines: 40

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.  
All edges are synchronised to the rising edge of CLK2.



HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]  
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK'' is at the output of color mixer 007593.  
CBLK' is shifted inside the 007593 one pixel clock.

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A

B

C

D

E

F

A

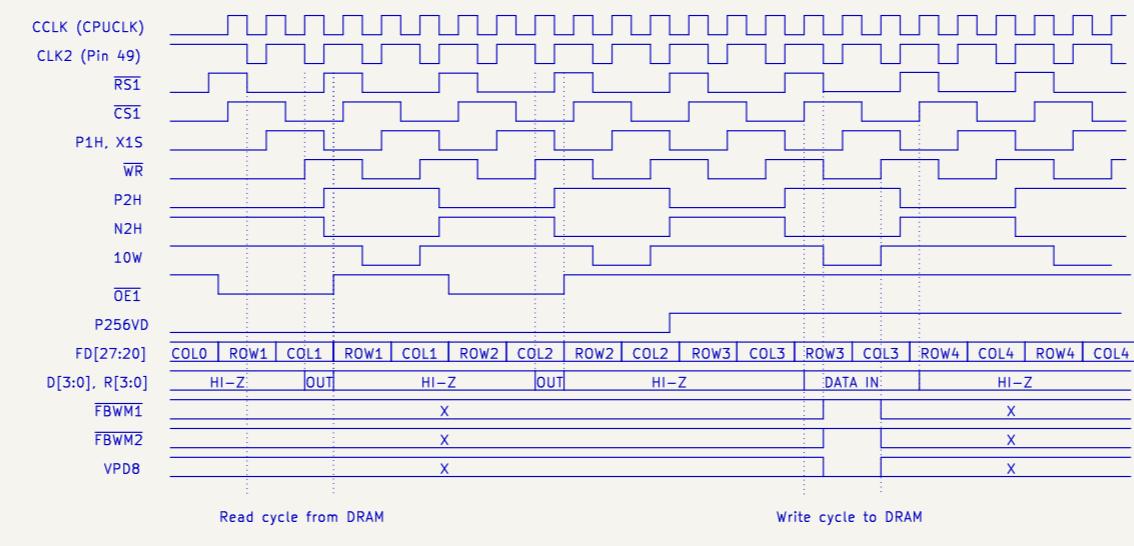
B

C

D

E

F



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Sheet: /Sprite timing diagrams/  
File: sprite\_timing\_diagrams.kicad\_sch

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Id: 20/20