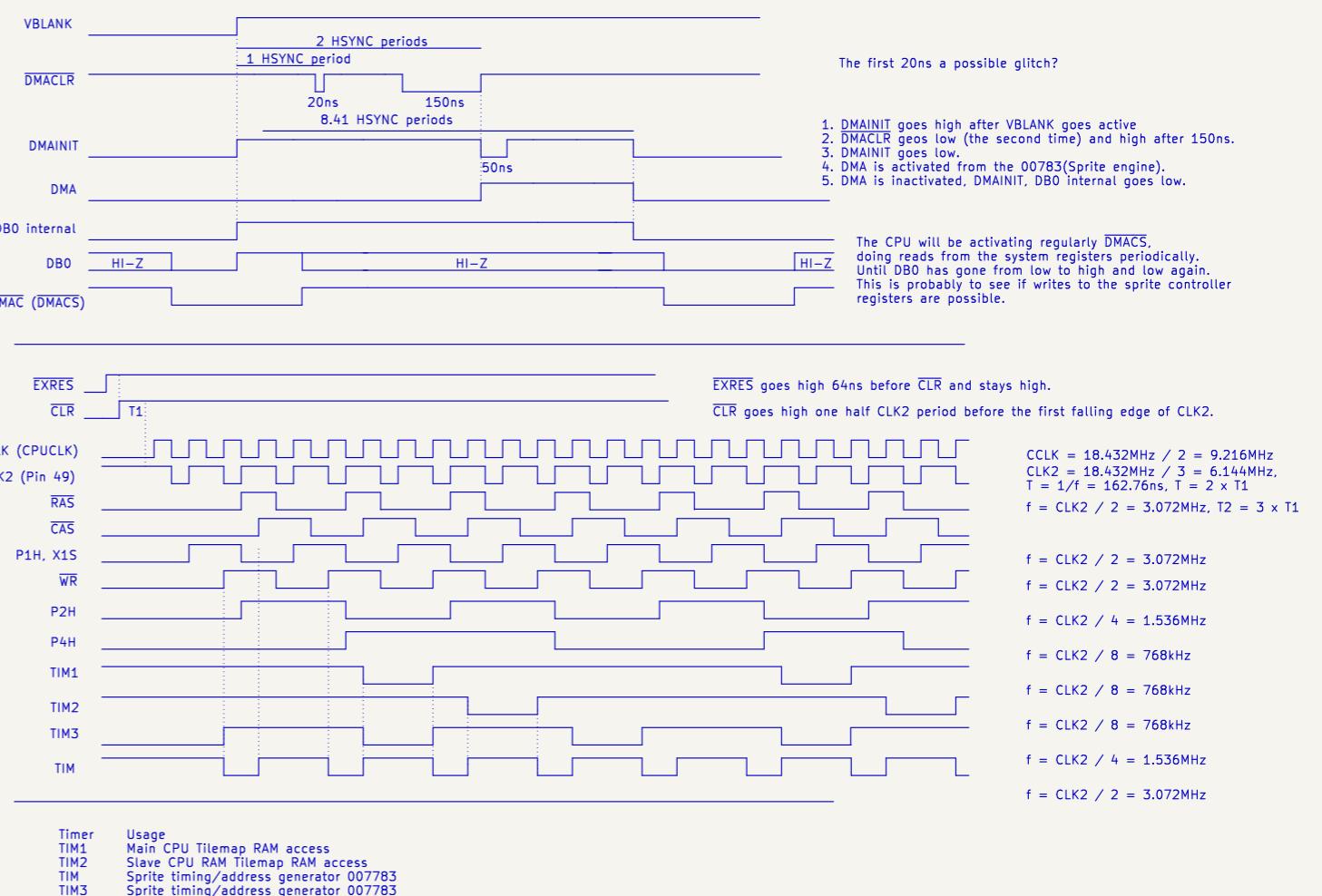
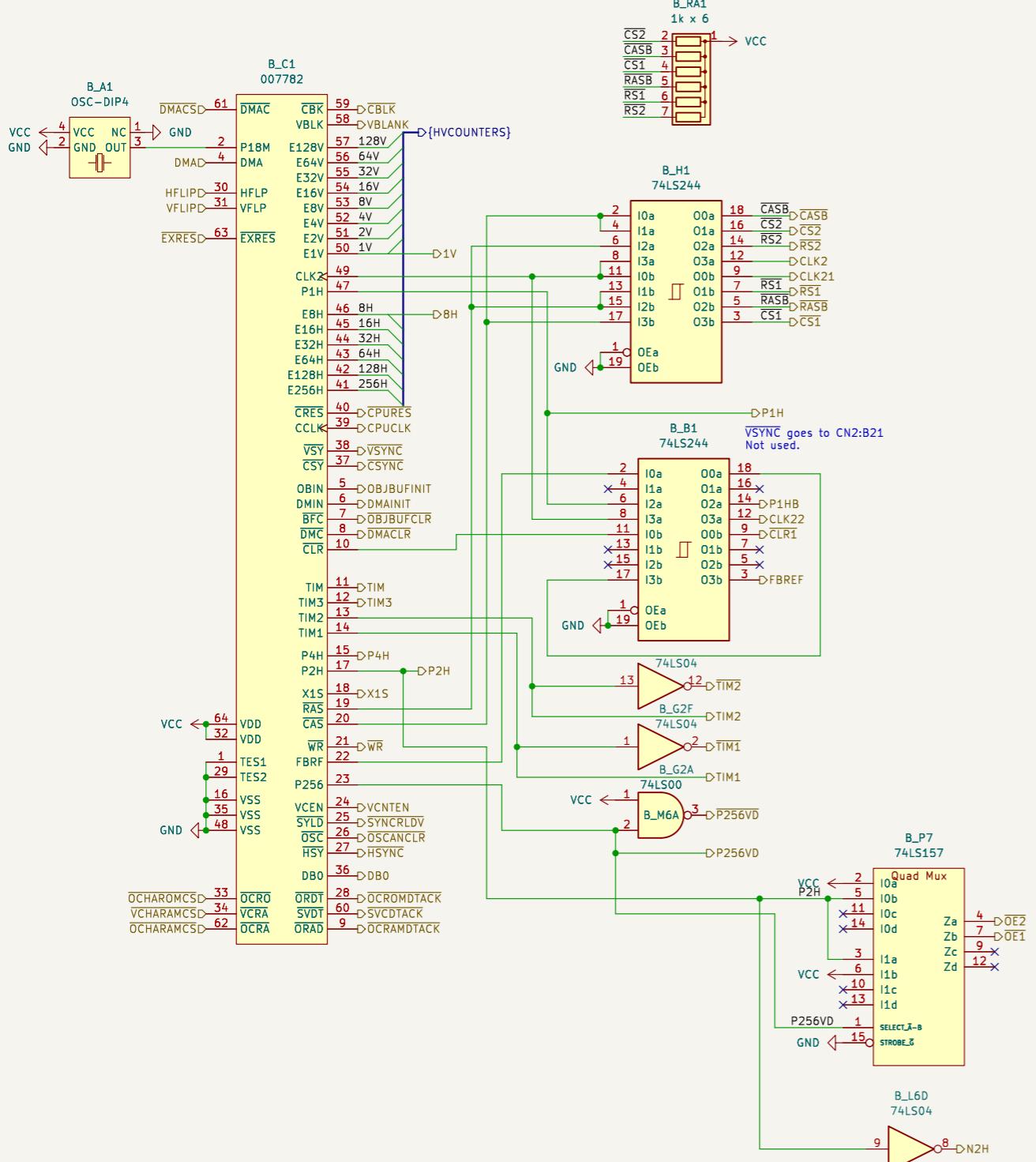
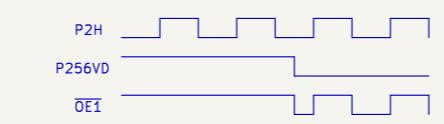


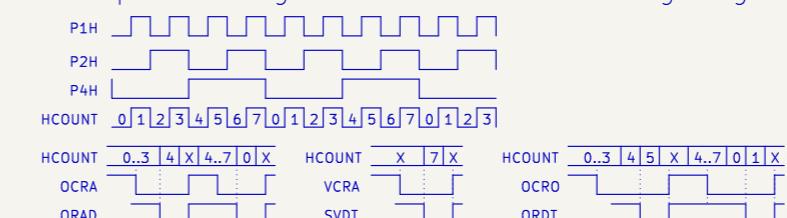
DMA Synchronization



Output enables active vs. part of frame buffer active



Chip select signals and Data Acknowledge signals



Ulf Skutnabba, twitter: @skutis77

Konami GX687 / GX785

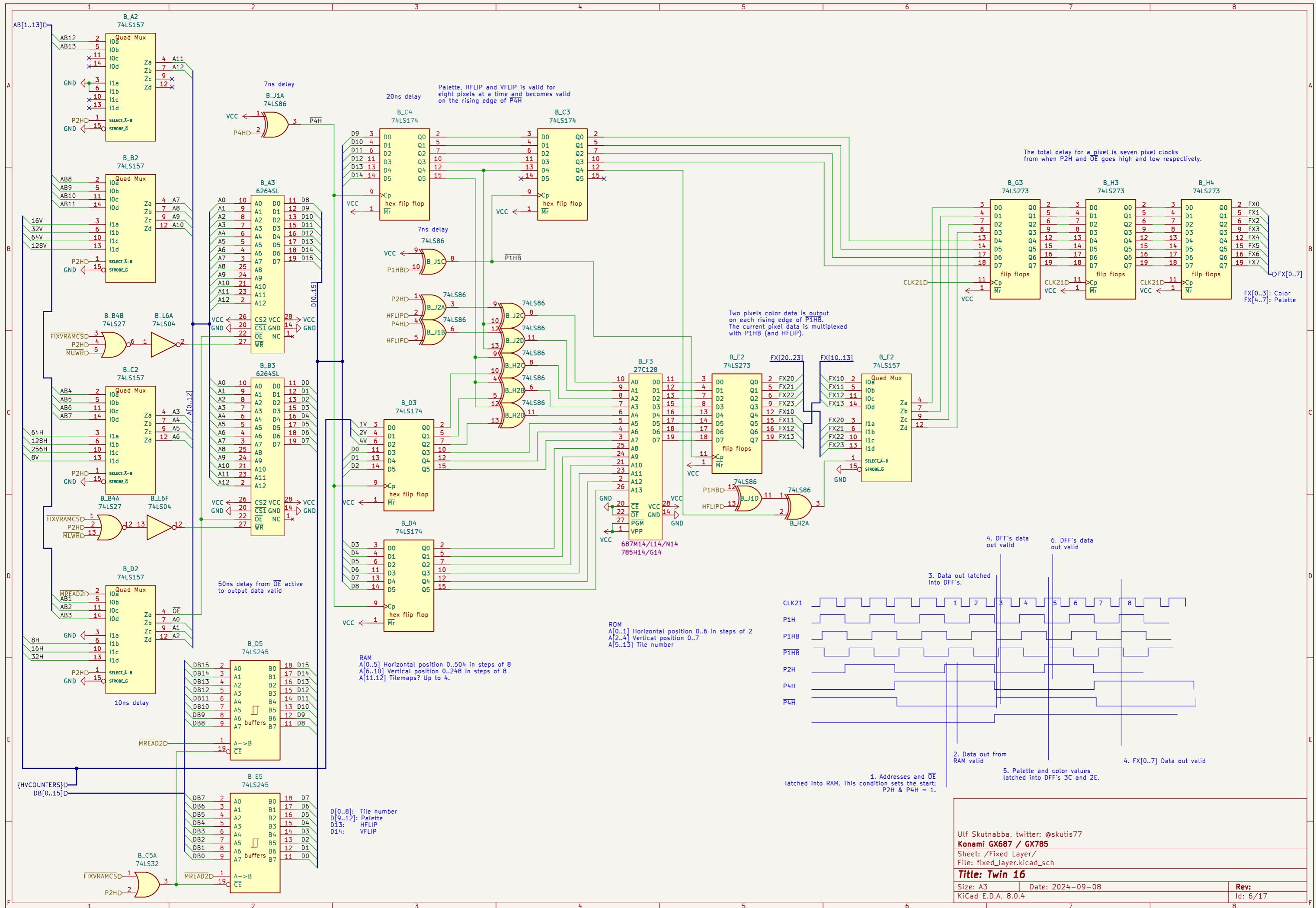
Sheet: /Timing/

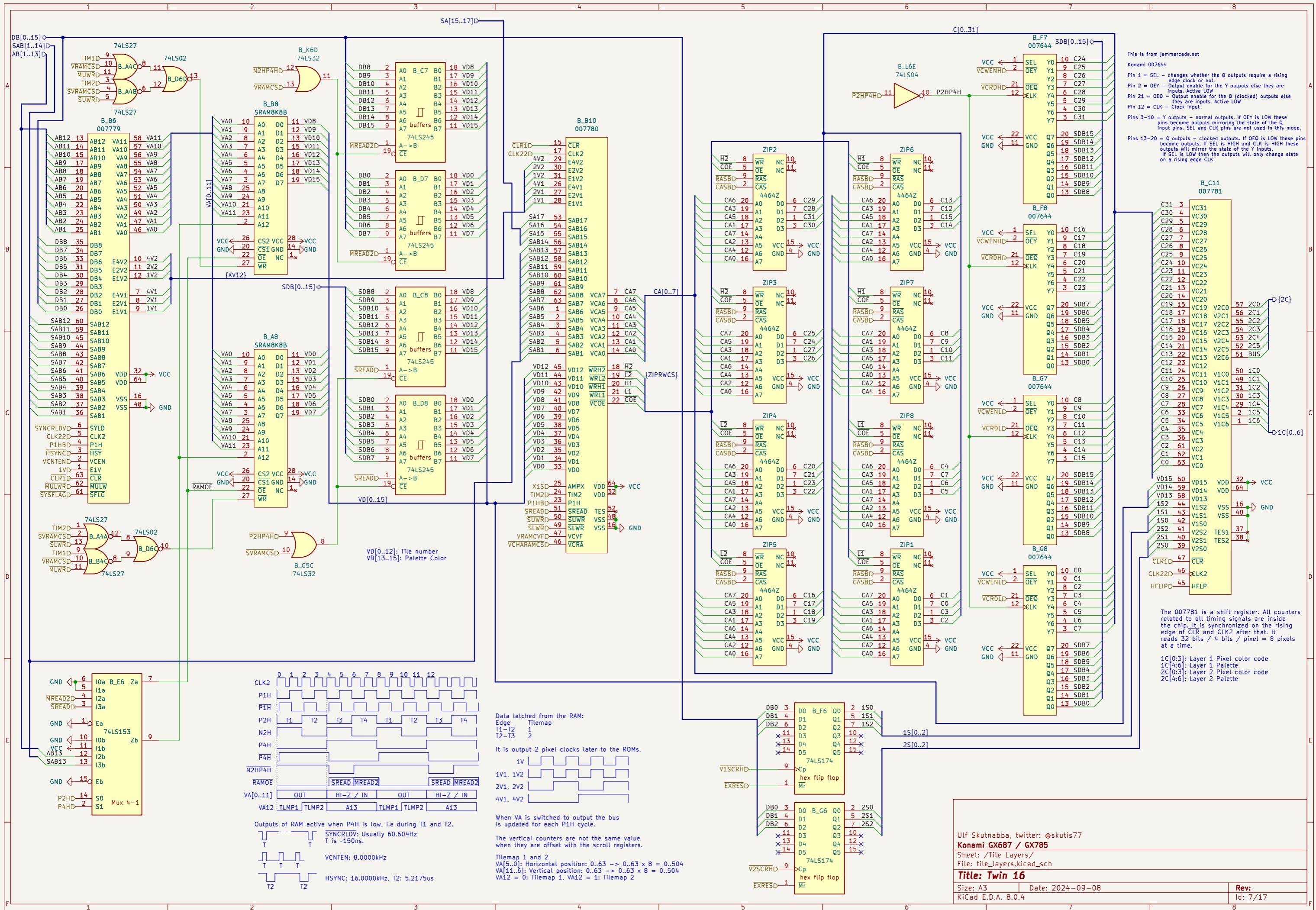
File: timing.kicad_sch

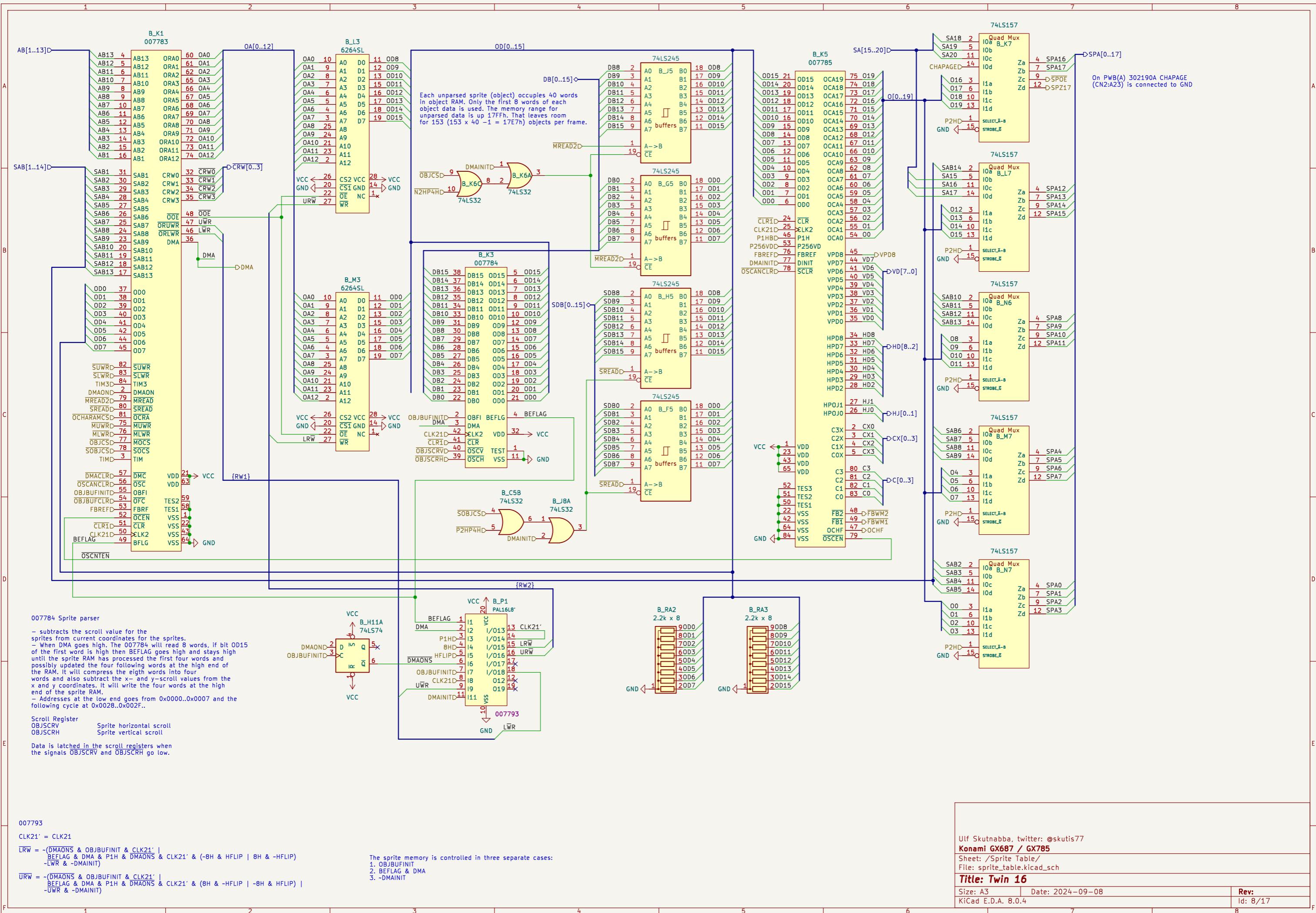
Title: Twin 16

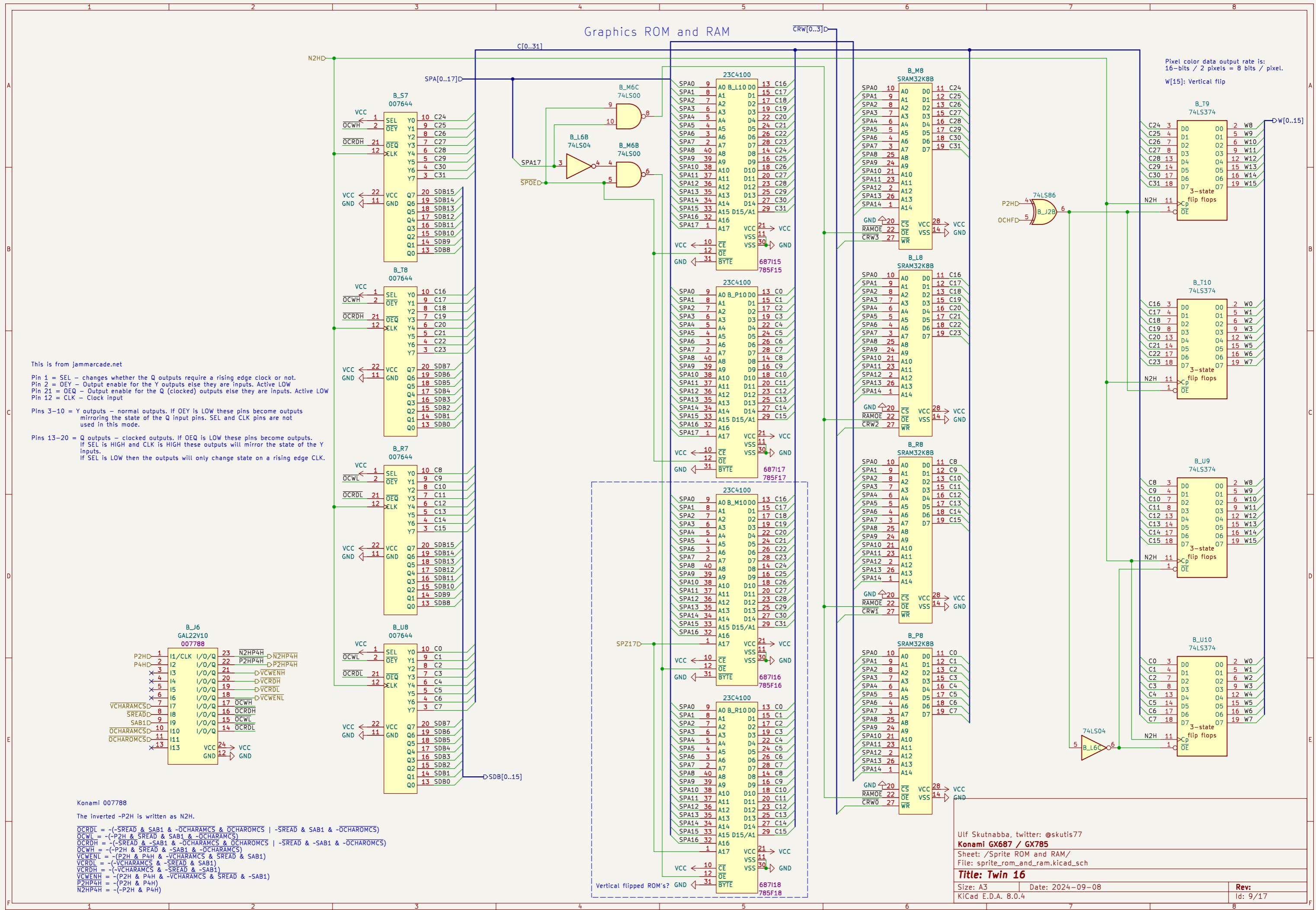
Size: A3 Date: 2024-09-08
KiCad E.D.A. 8.0.4

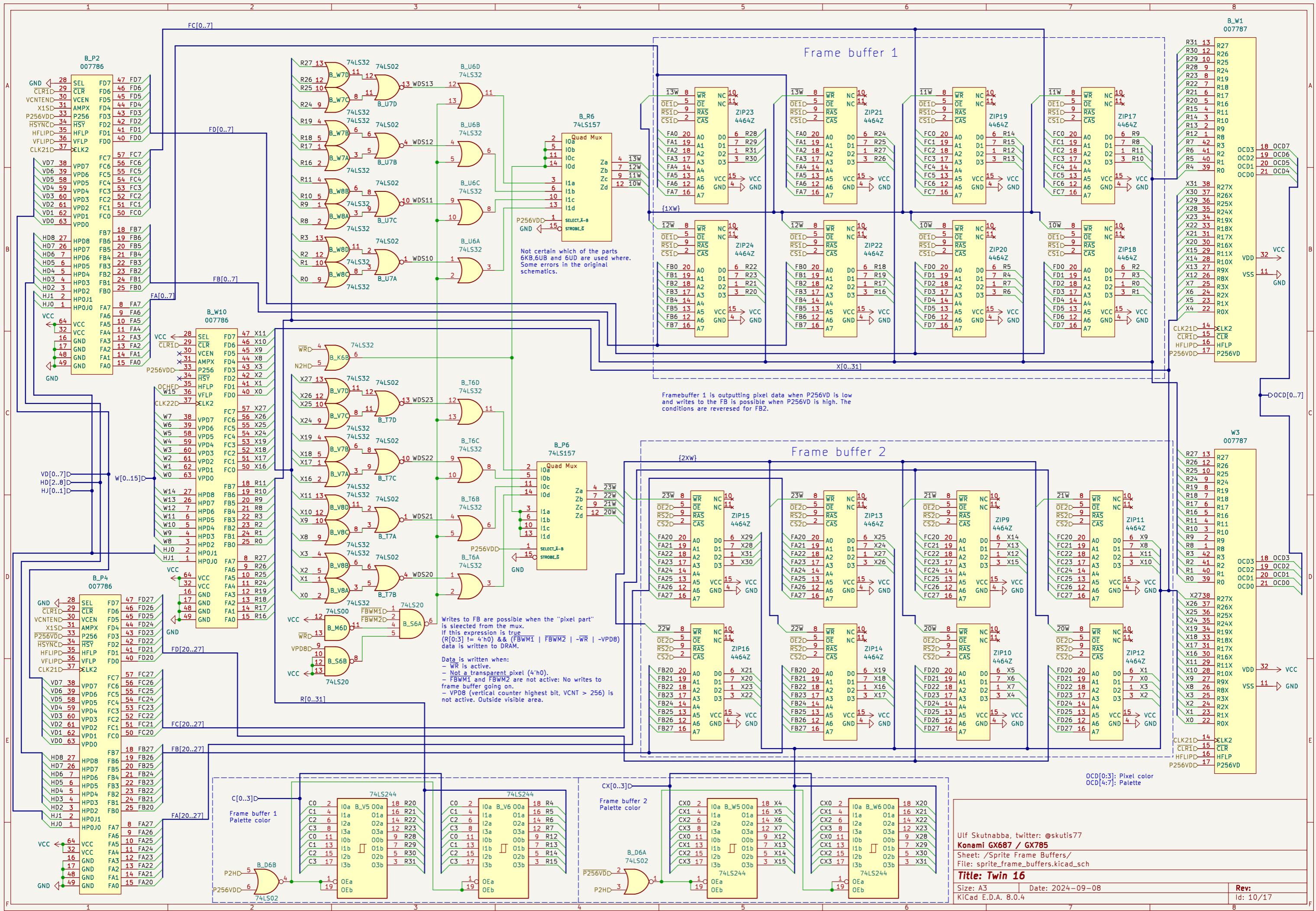
Rev: Id: 5/17

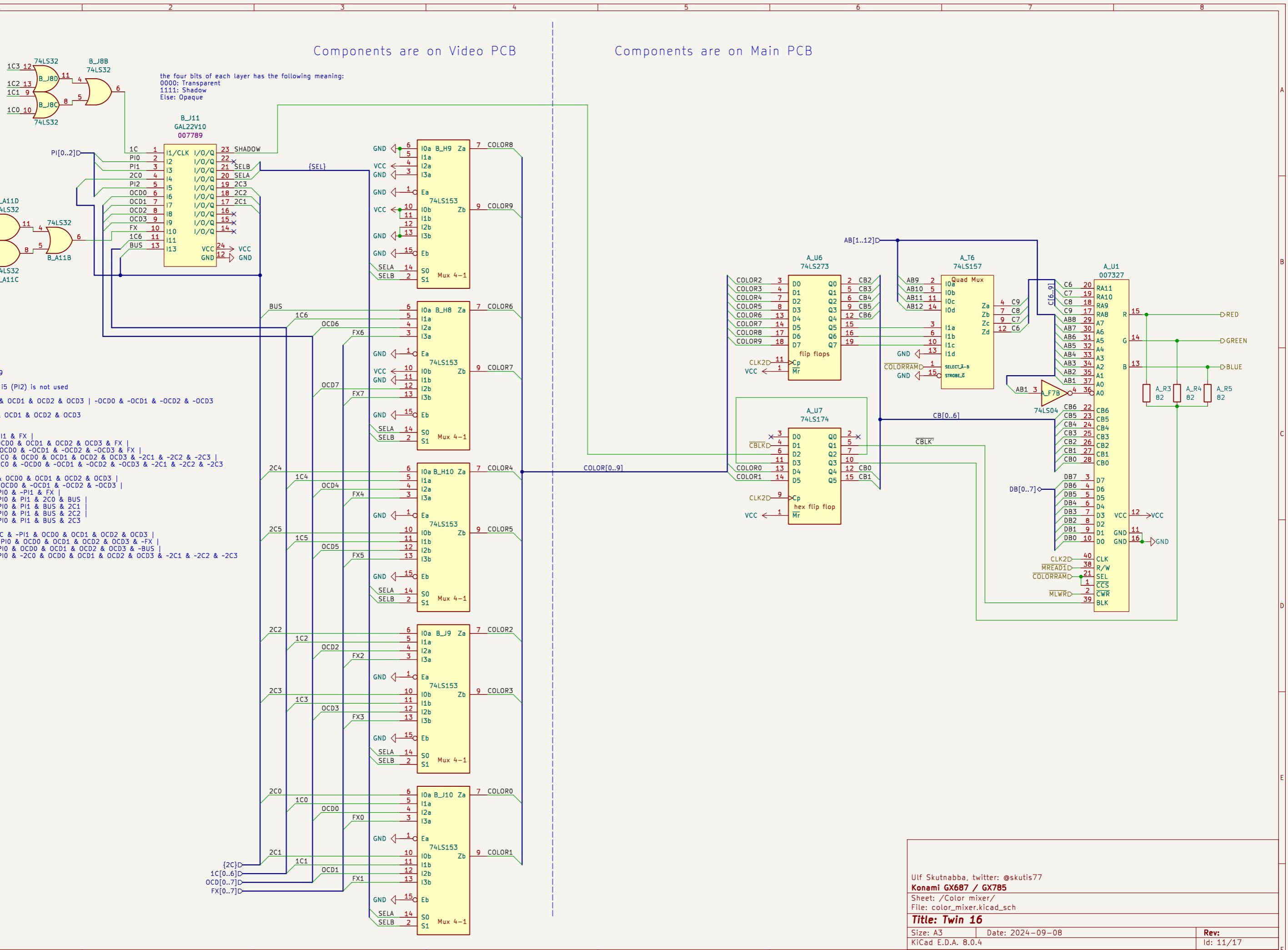


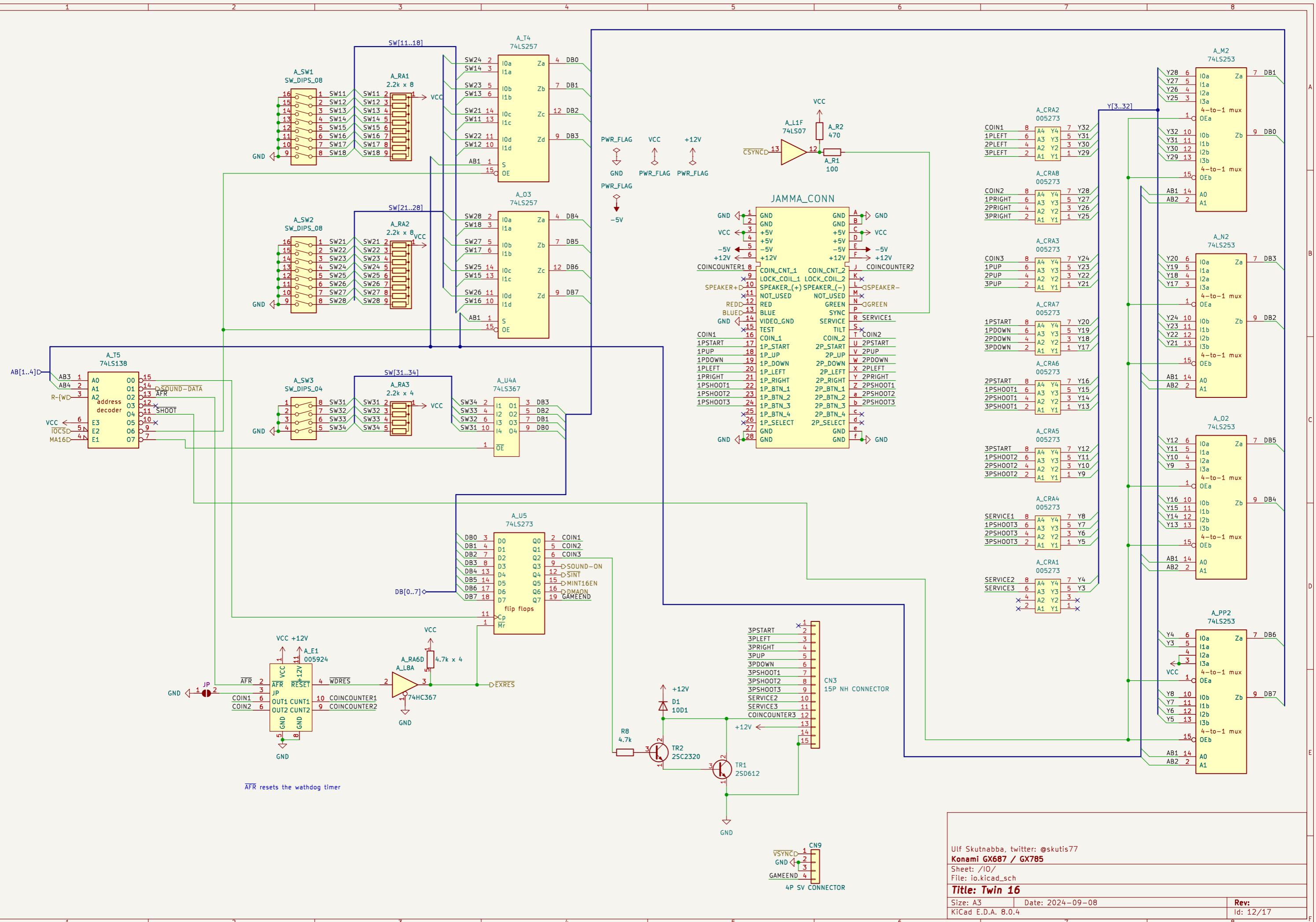


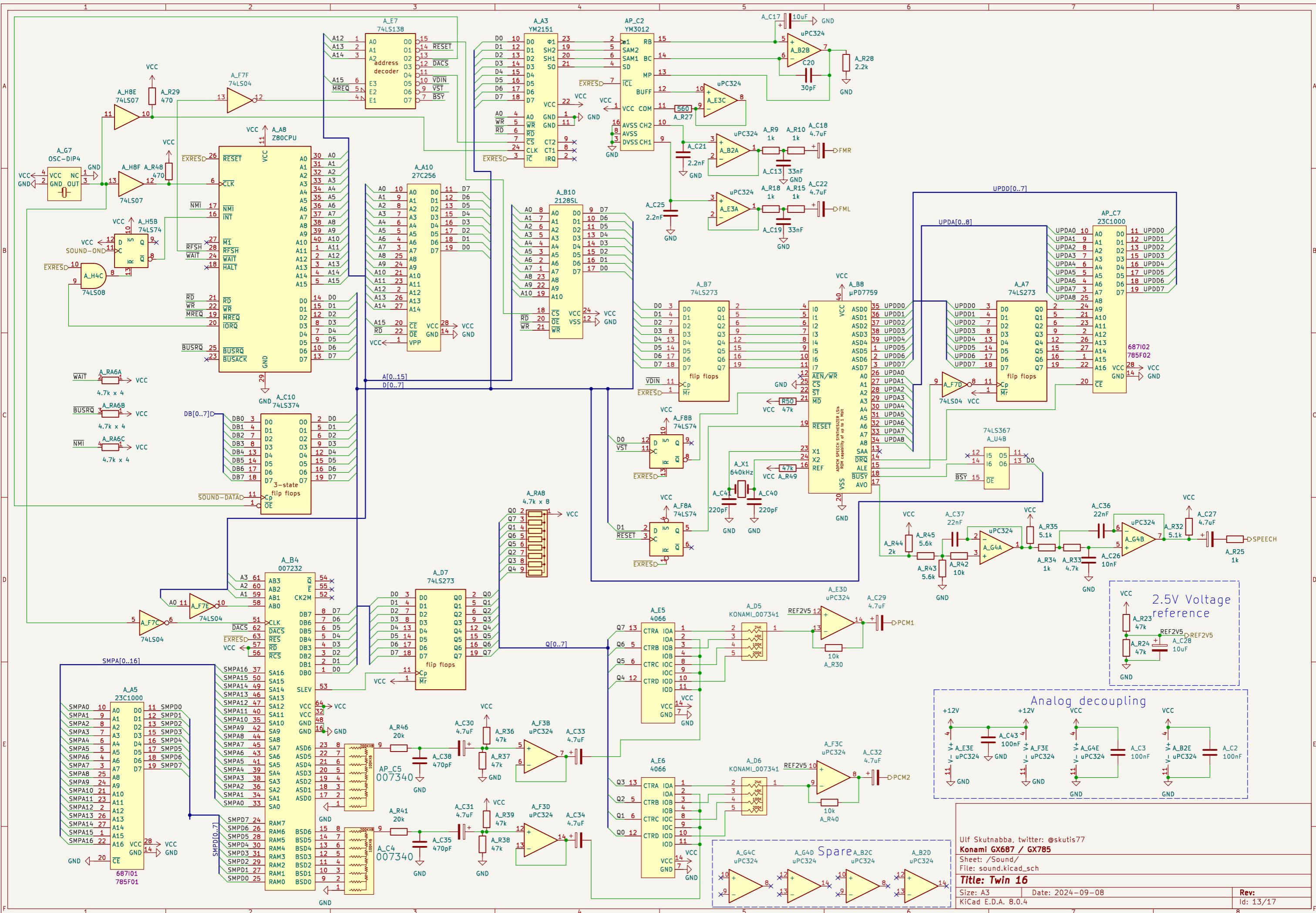




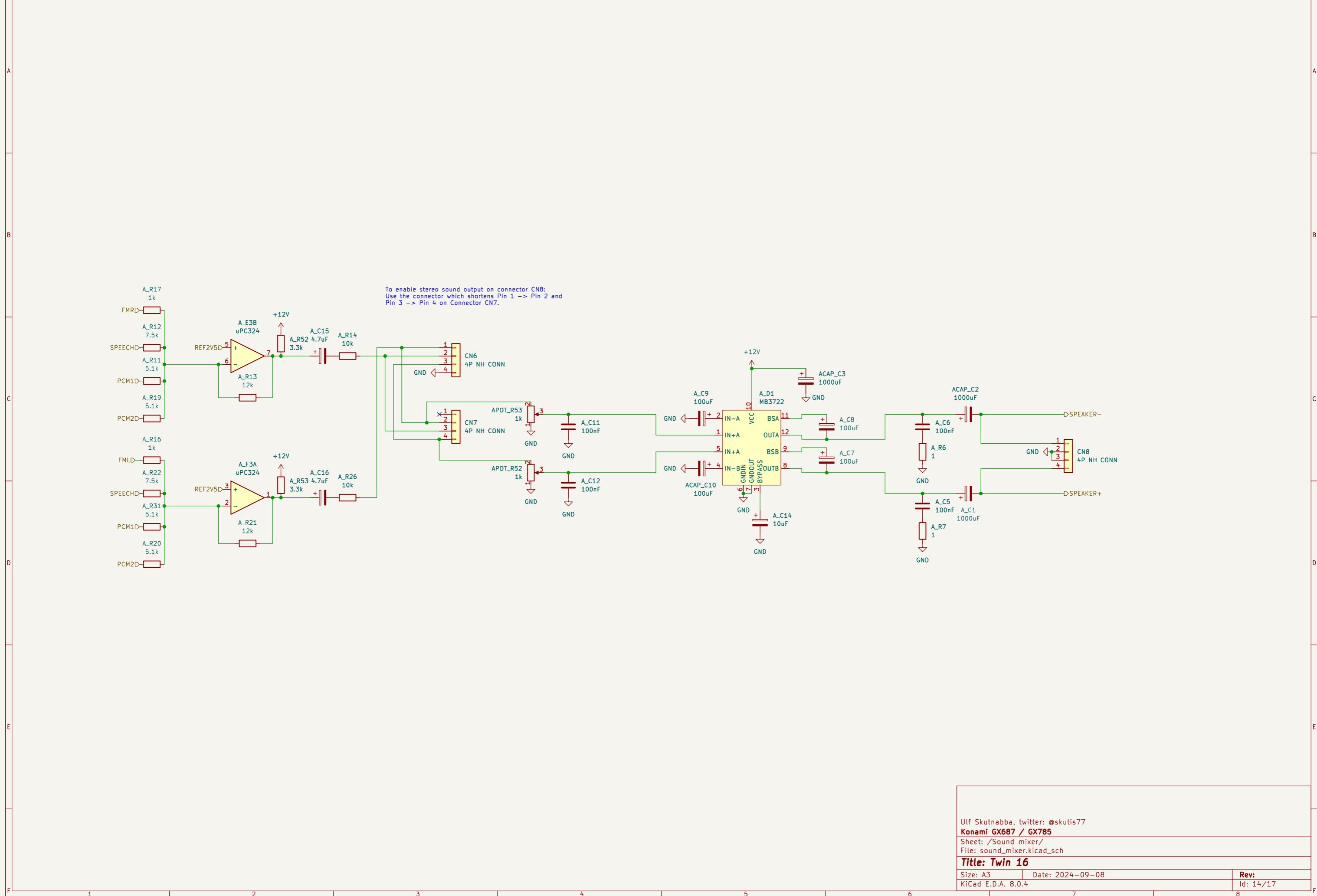




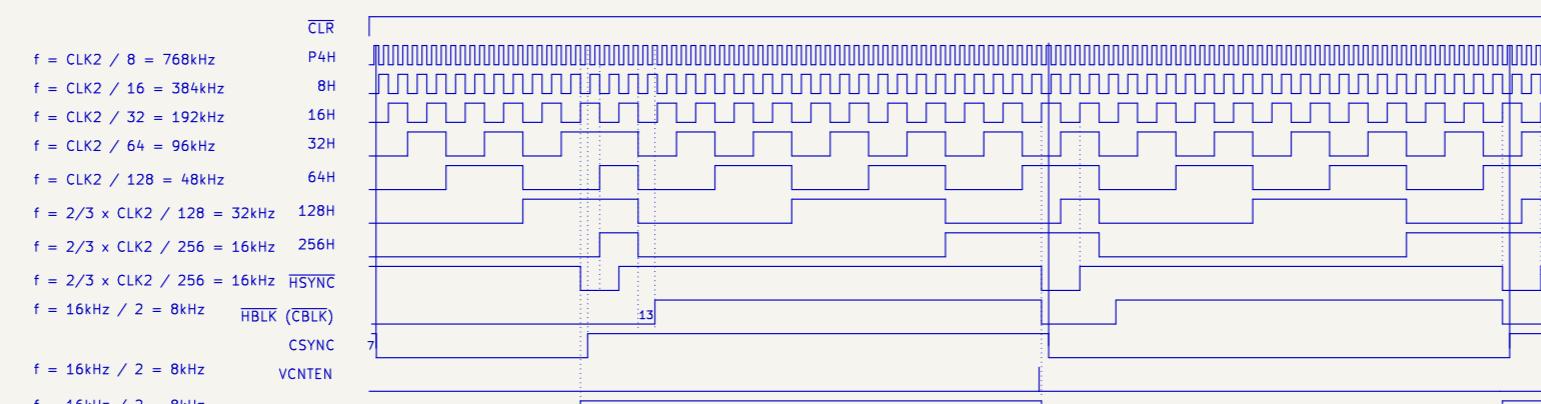




1 2 3 4 5 6 7 8



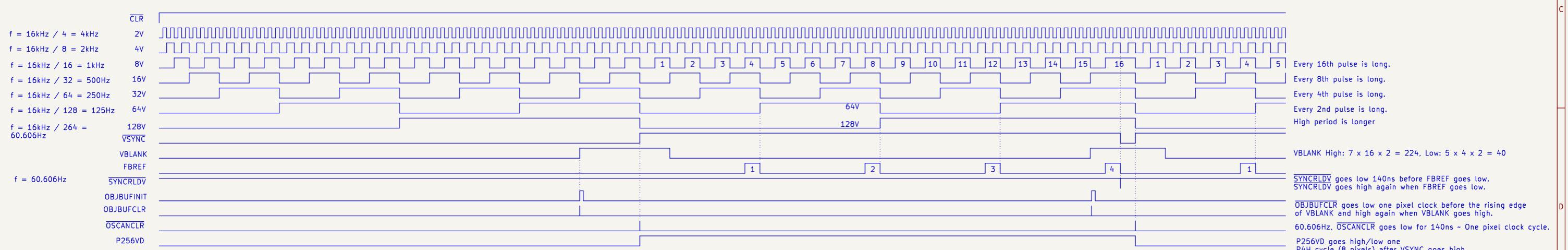
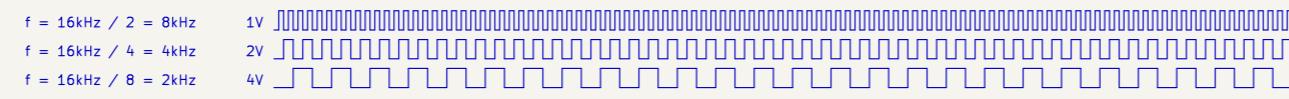
Horizontal signals



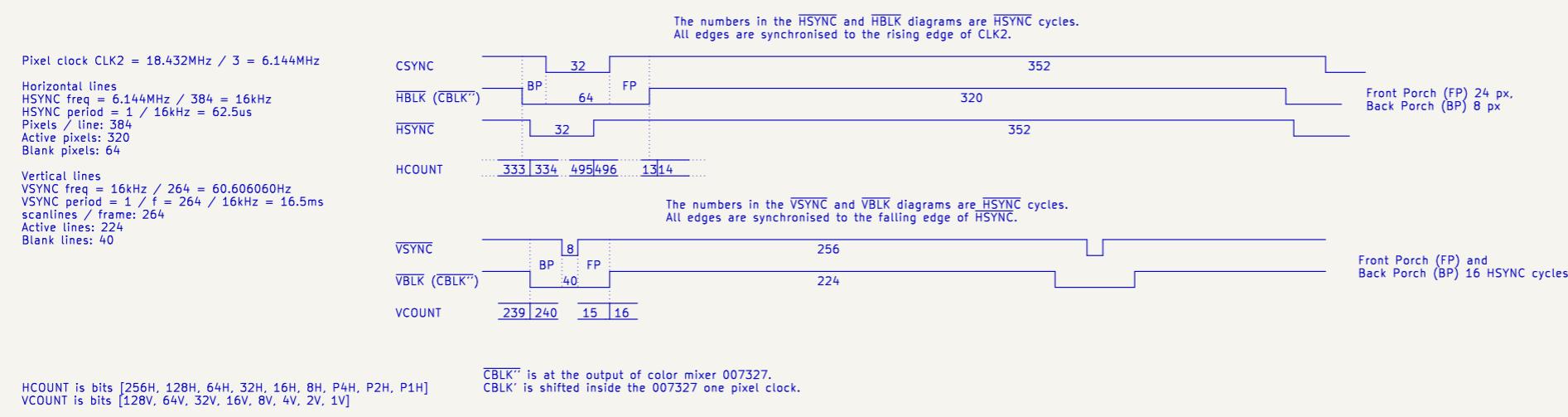
– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



Horizontal and vertical synch timing diagrams



Ulf Skutnabba, twitter: @skutis77

Konami GX687 / GX785

Sheet: /Timing diagrams/

File: timing_diagrams.kicad_sch

Title: Twin 16

Size: A3 Date: 2024-09-08

KiCad E.D.A. 8.0.4

Rev:

Id: 15/17

A

B

C

D

E

F

A

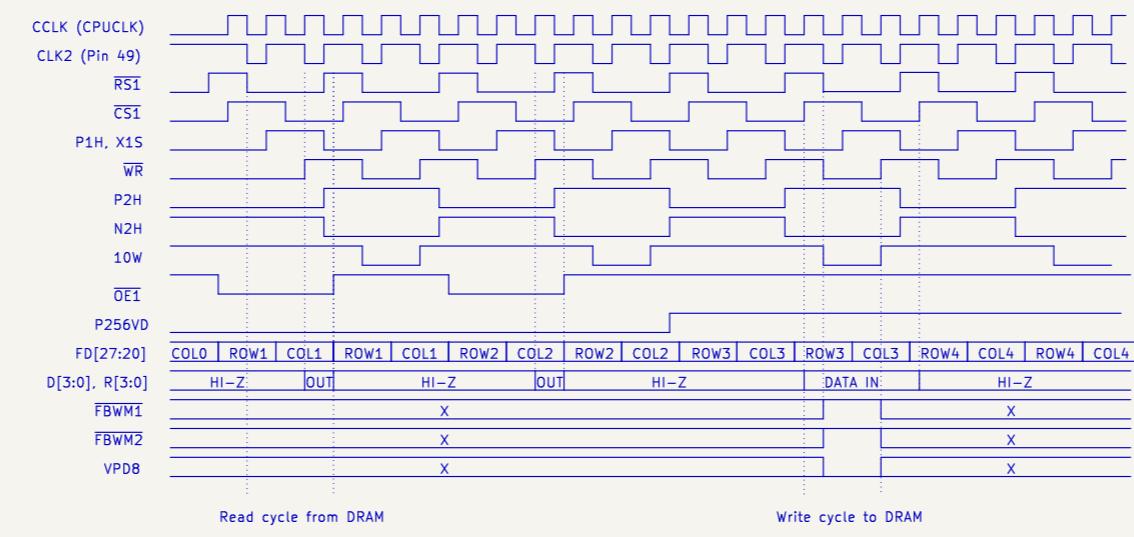
B

C

D

E

F



Ulf Skutnabba, twitter: @skutis77

Konami GX687 / GX785Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch**Title: Twin 16**Size: A3 | Date: 2024-09-08
KiCad E.D.A. 8.0.4Rev:
Id: 16/17

