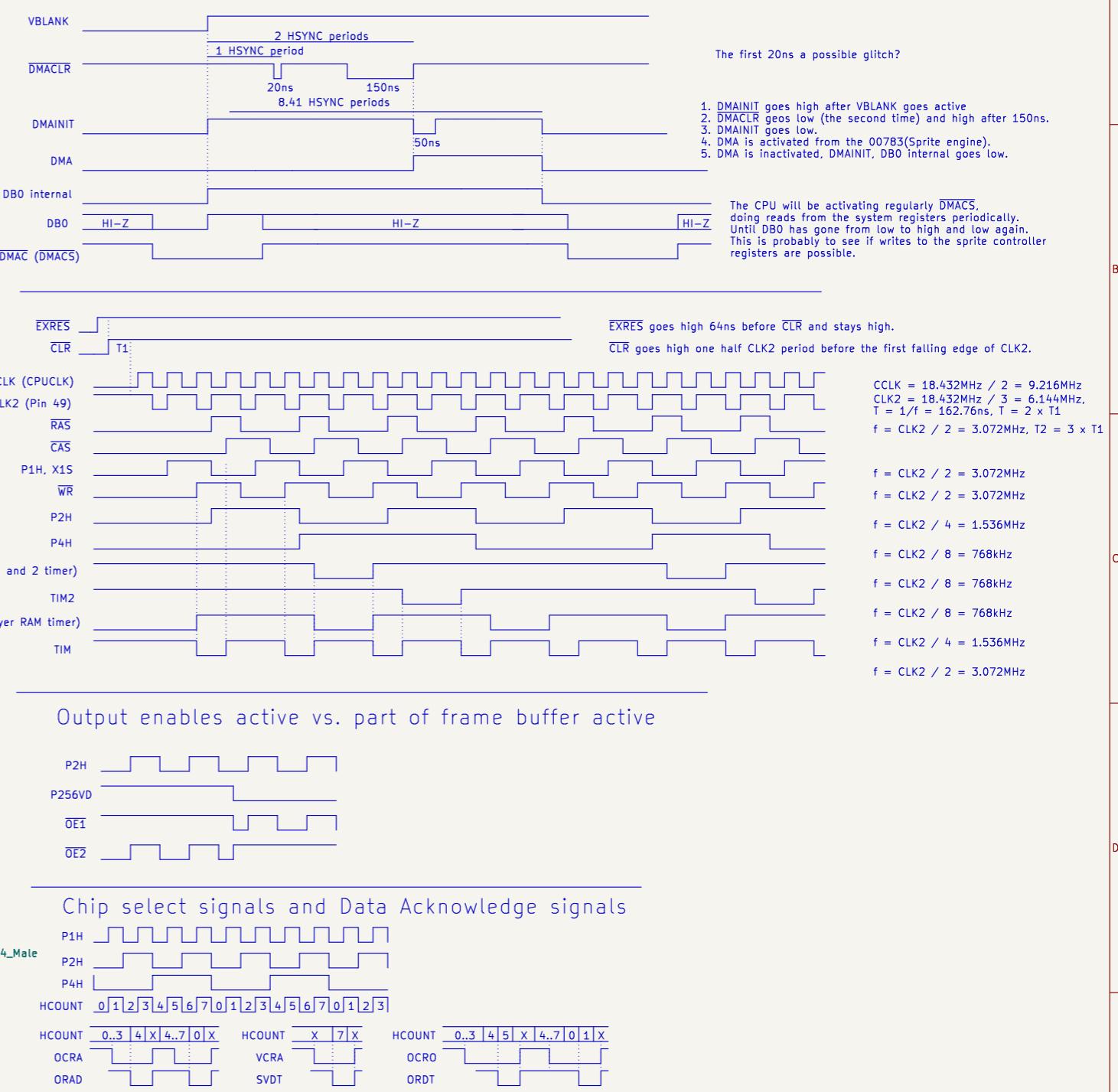
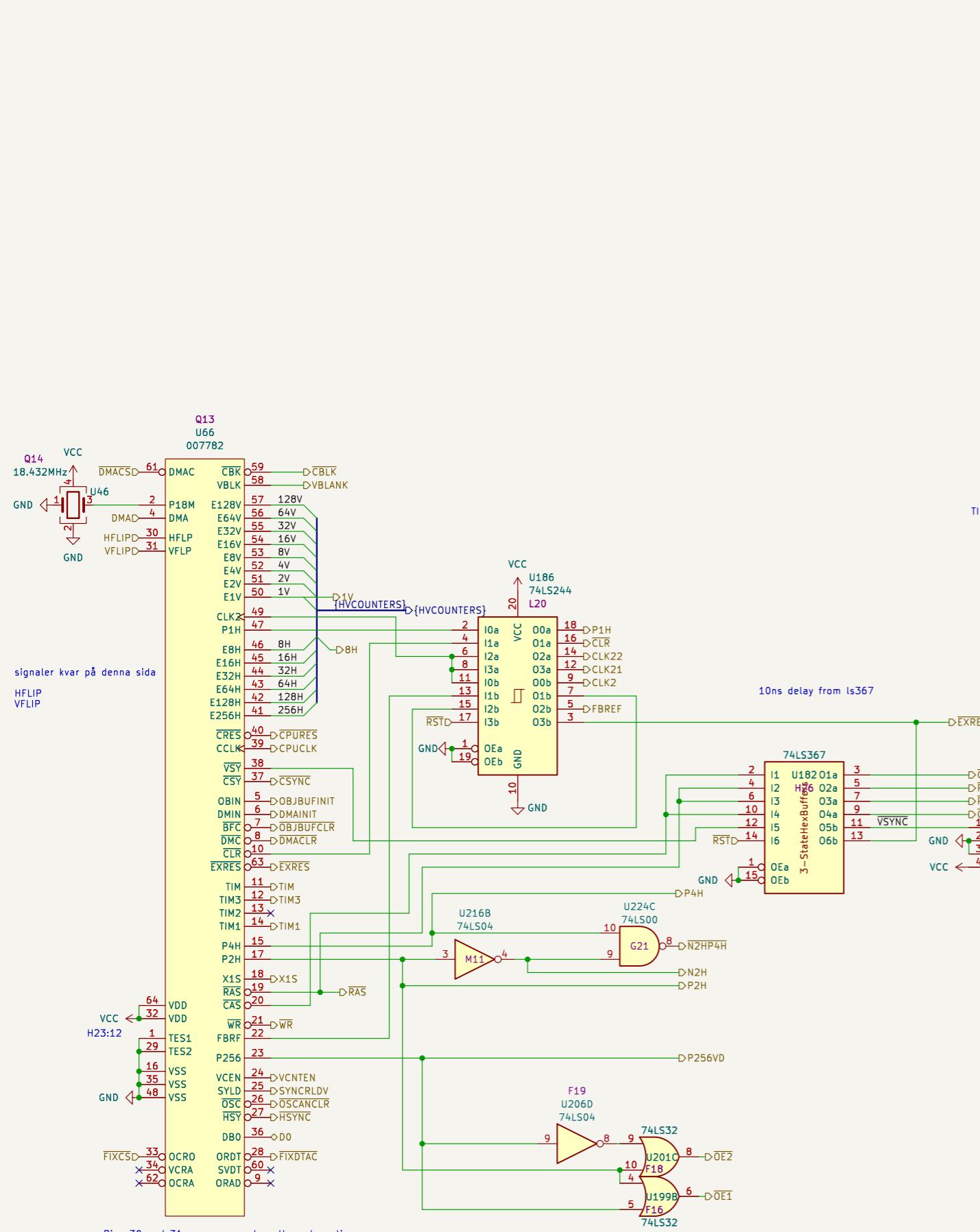


DMA Synchronization



Pins 30 and 31 were swapped on the schematics.

Hiring
Konami GX870

Sheet: /Timing/
File: [Timing.html](#)

File: timing.kicad_sch
Title: Title Final

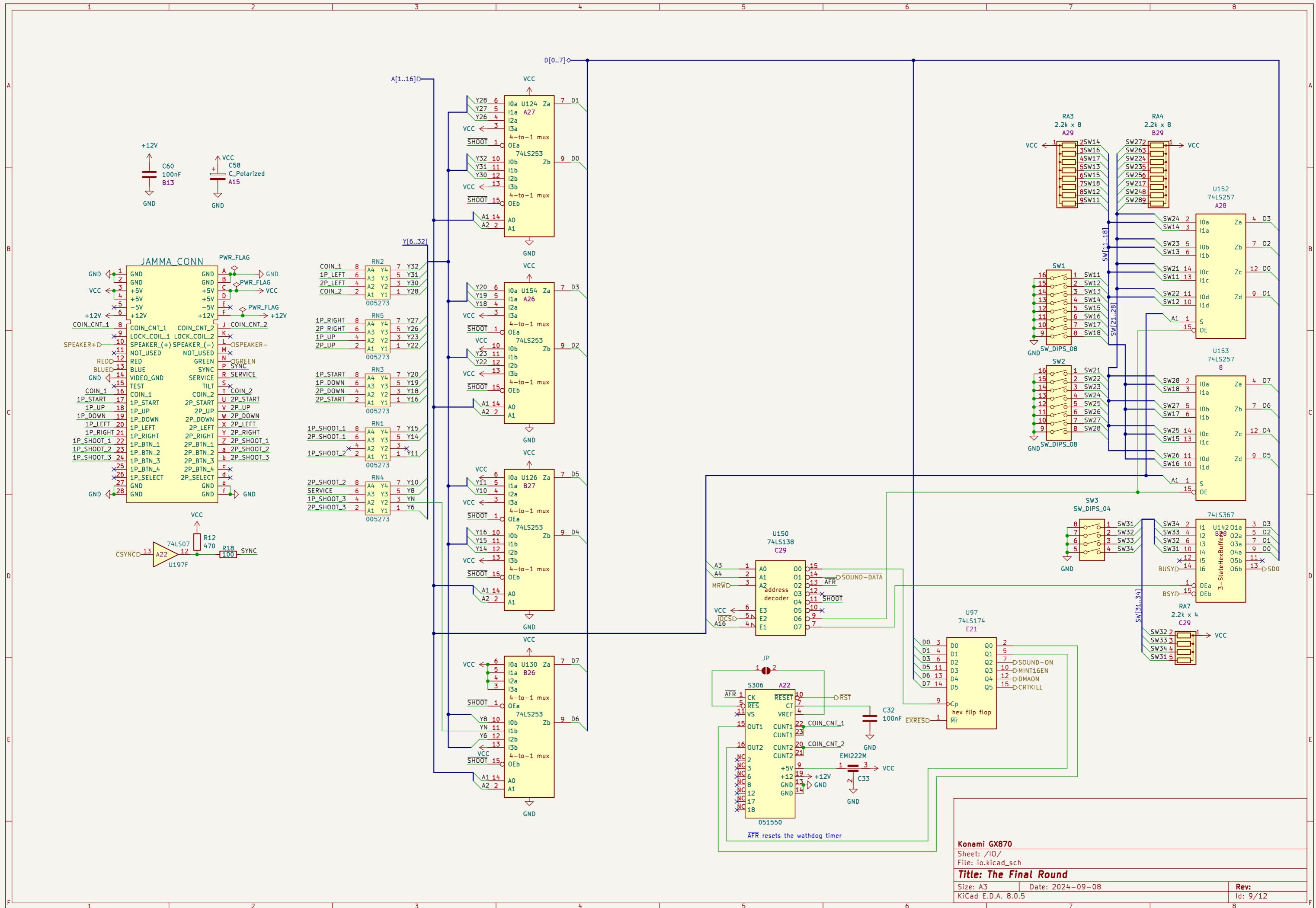
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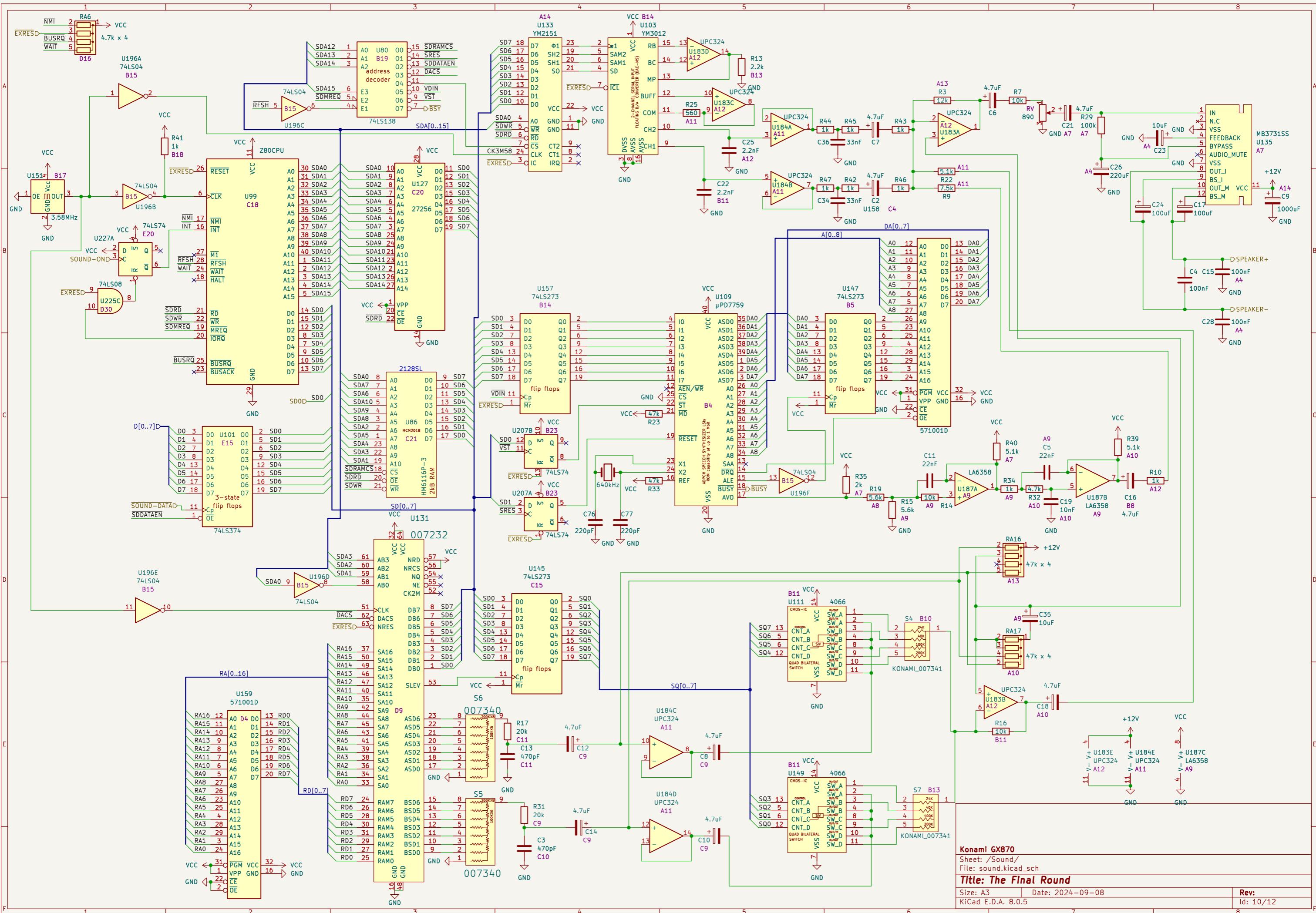
Size: A3 Date: 2024-09-01
KiCad EDA 8.0.5

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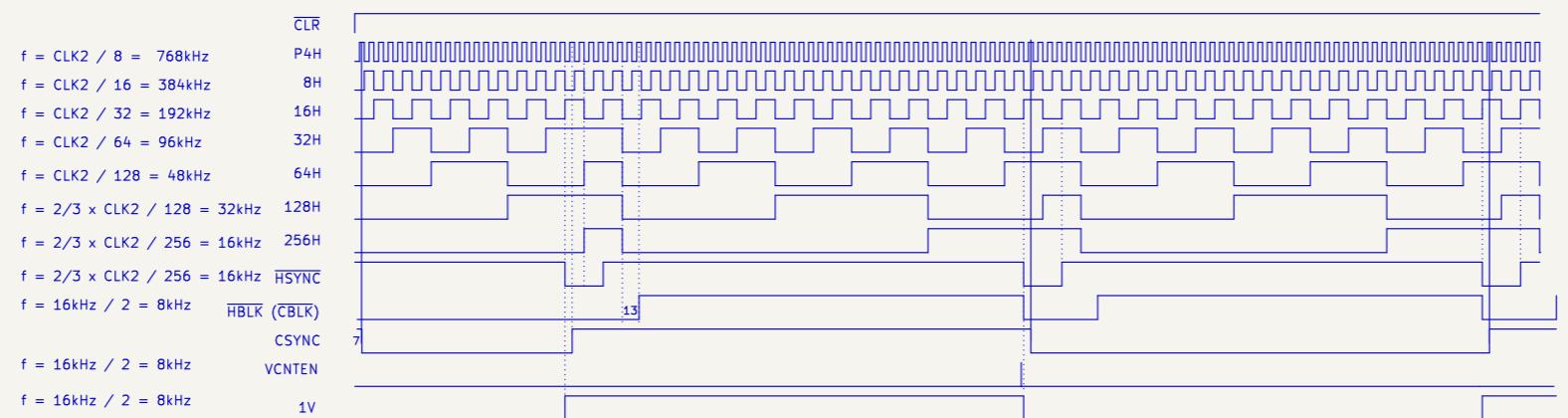
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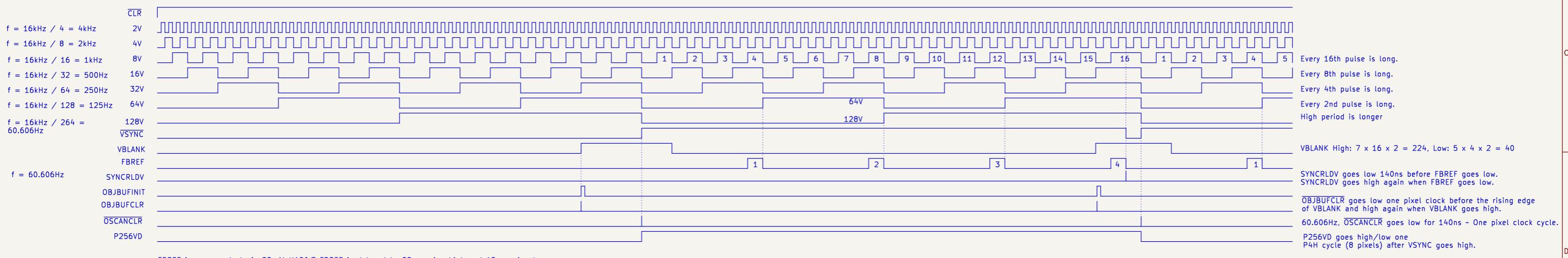
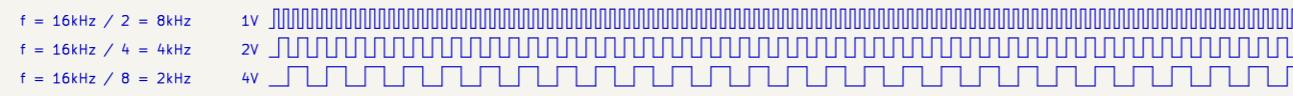
Horizontal signals

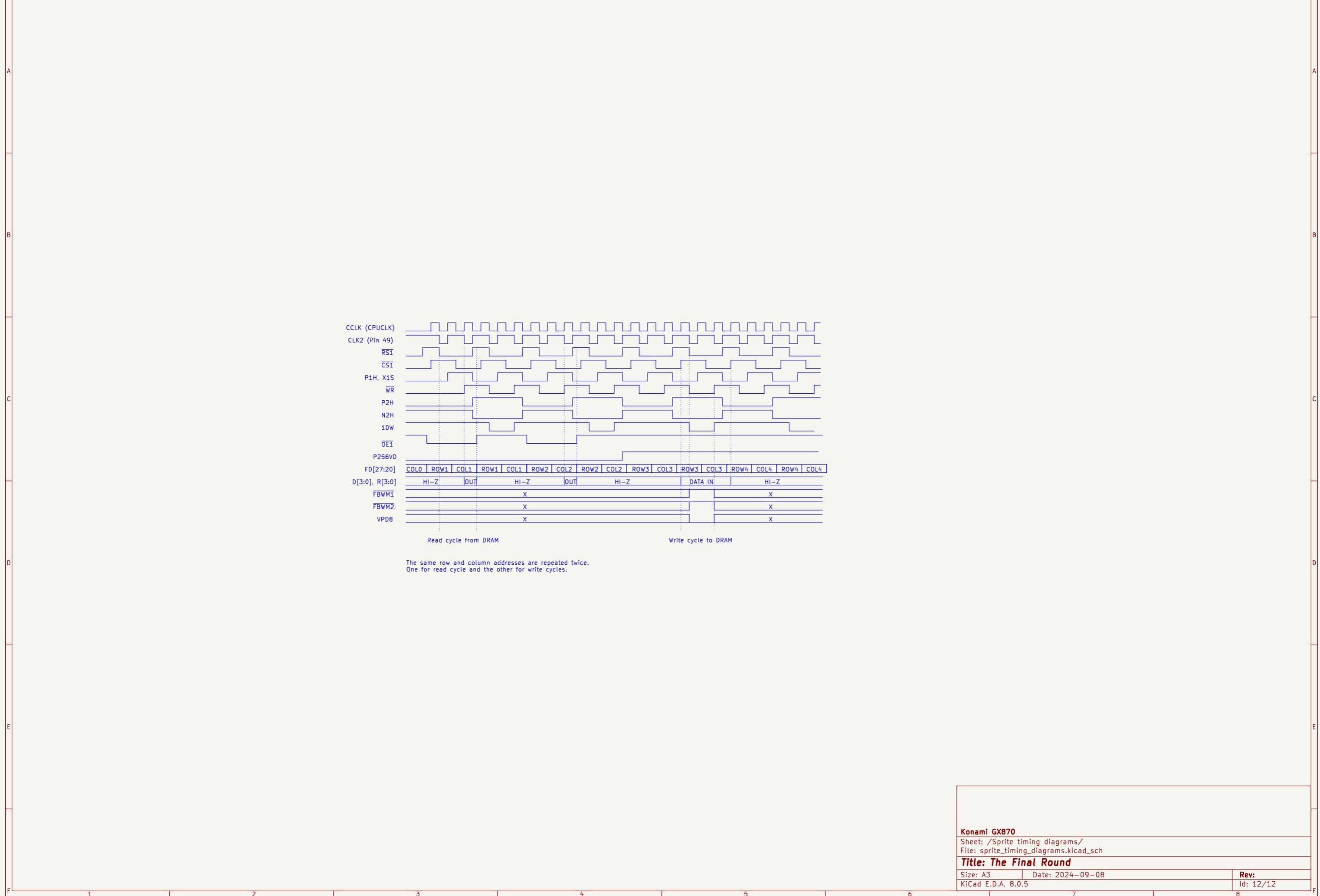


- The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

- CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



**Konami GX870**

Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: The Final Round

Size: A3 | Date: 2024-09-08
KiCad E.D.A. 8.0.5

Rev: | Id: 12/12