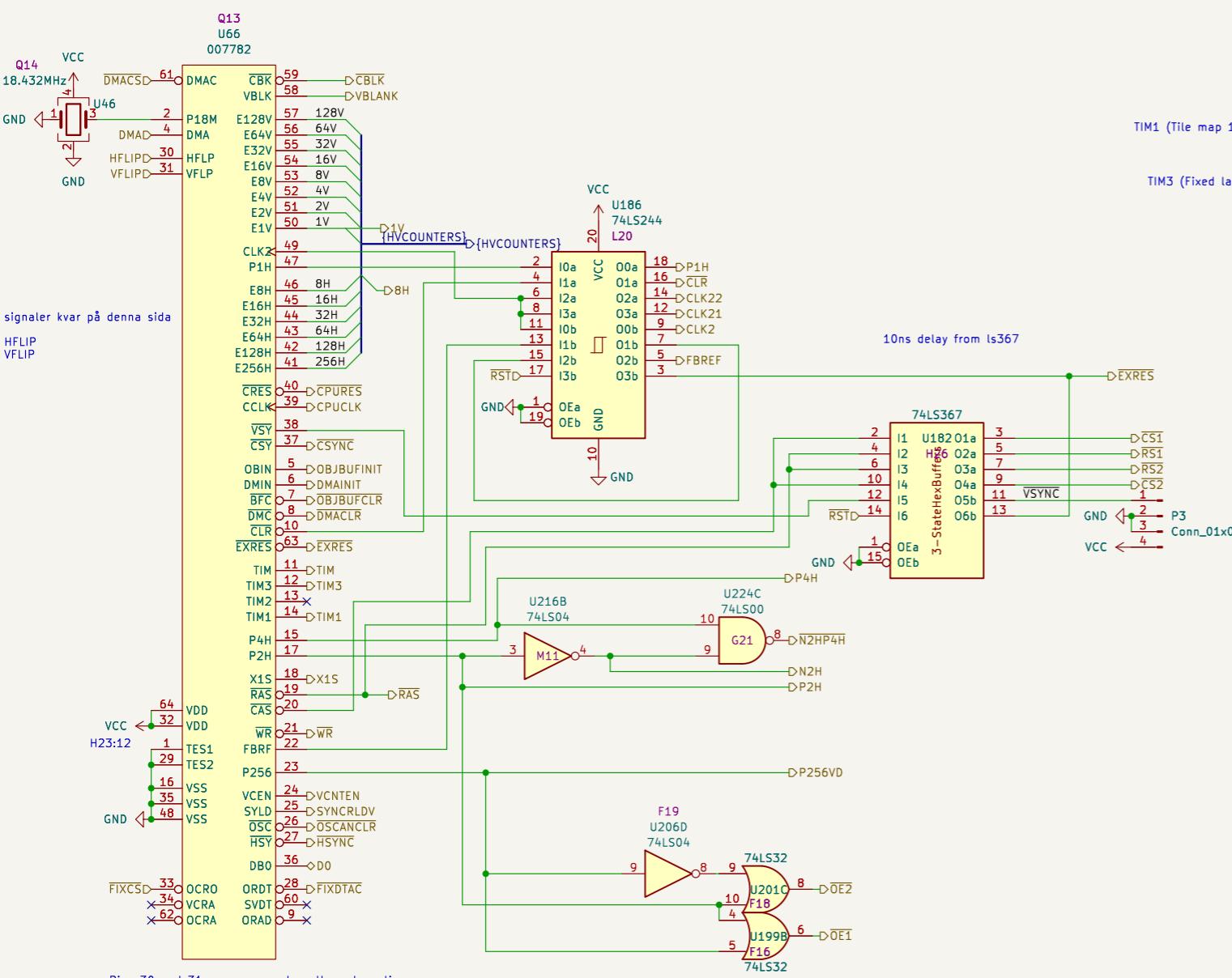
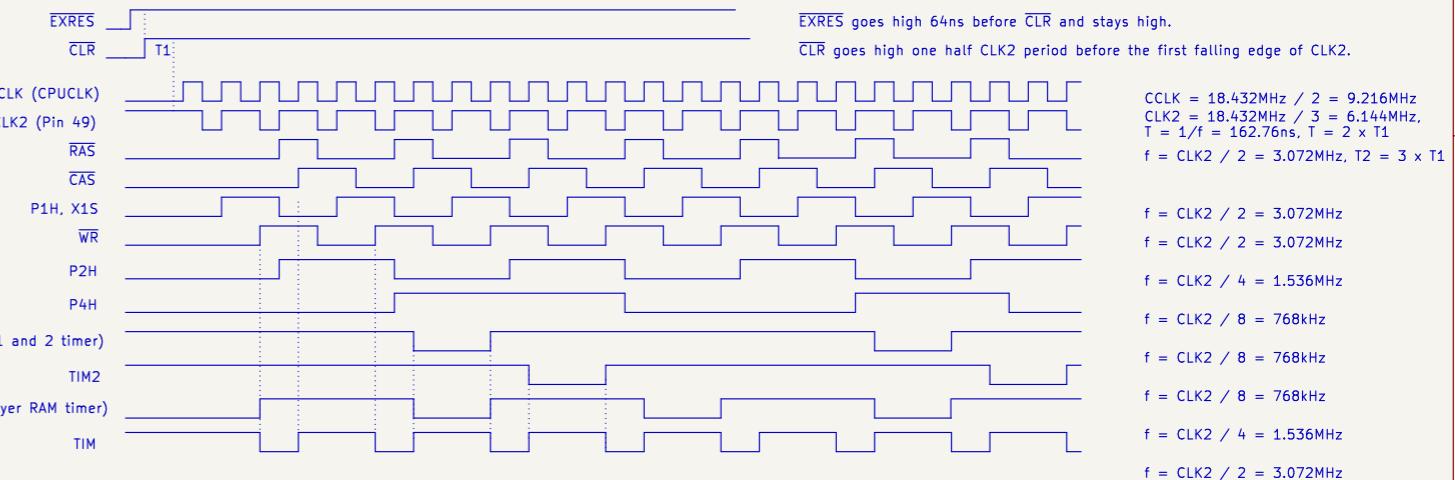
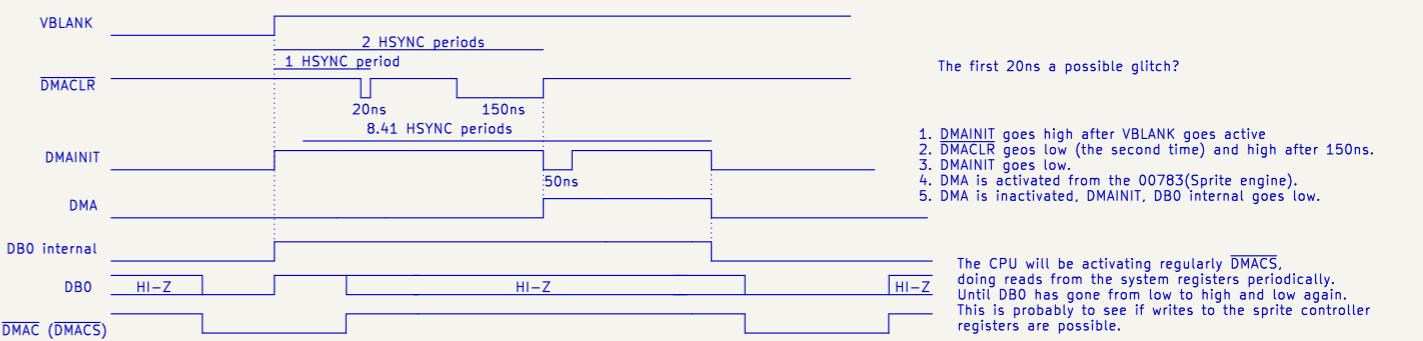
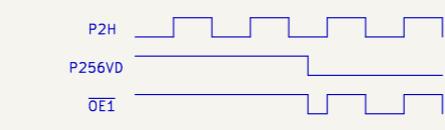


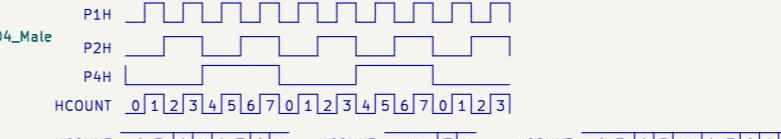
# DMA Synchronization



Output enables active vs. part of frame buffer active



Chip select signals and Data Acknowledge signals



## Timing

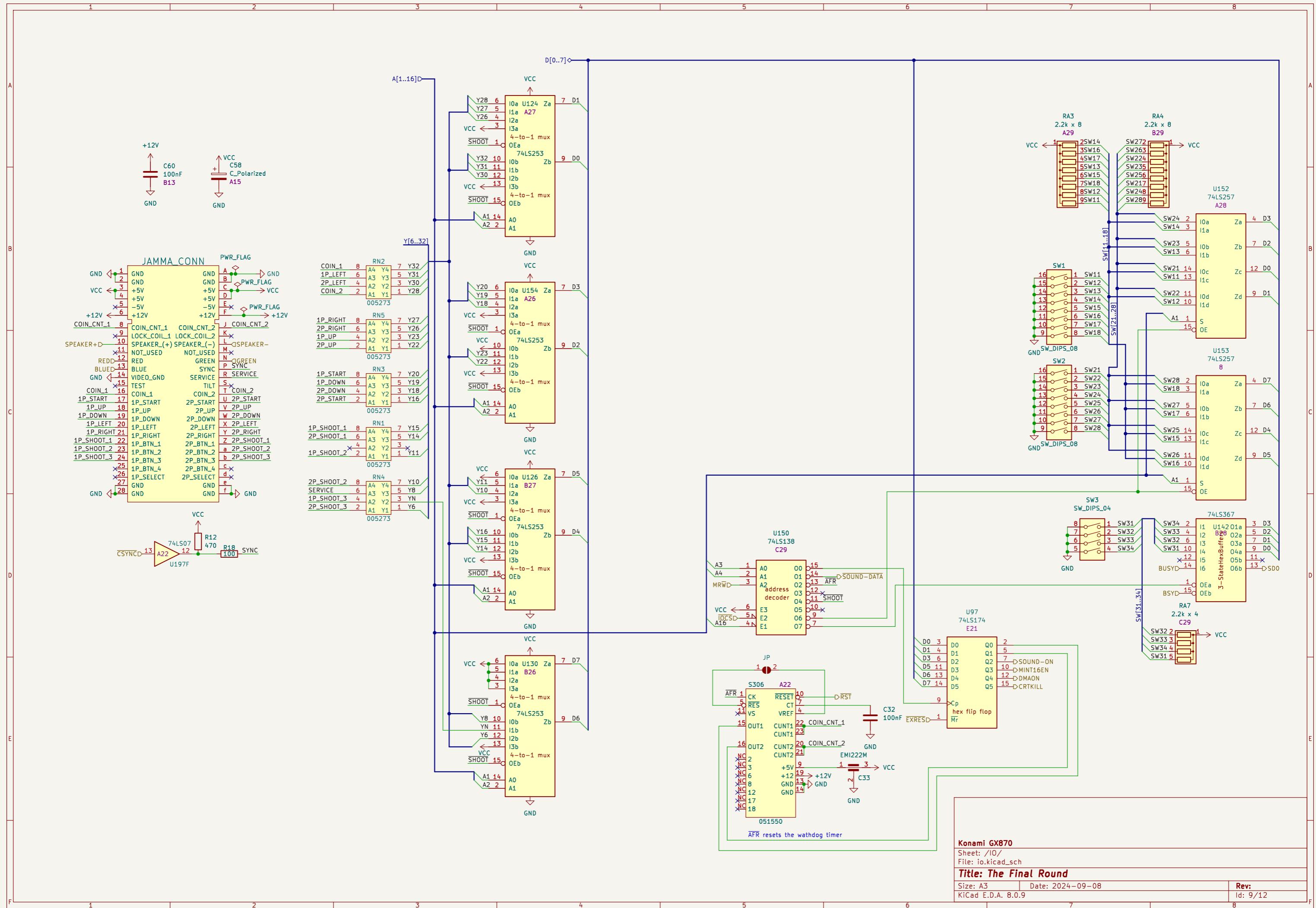
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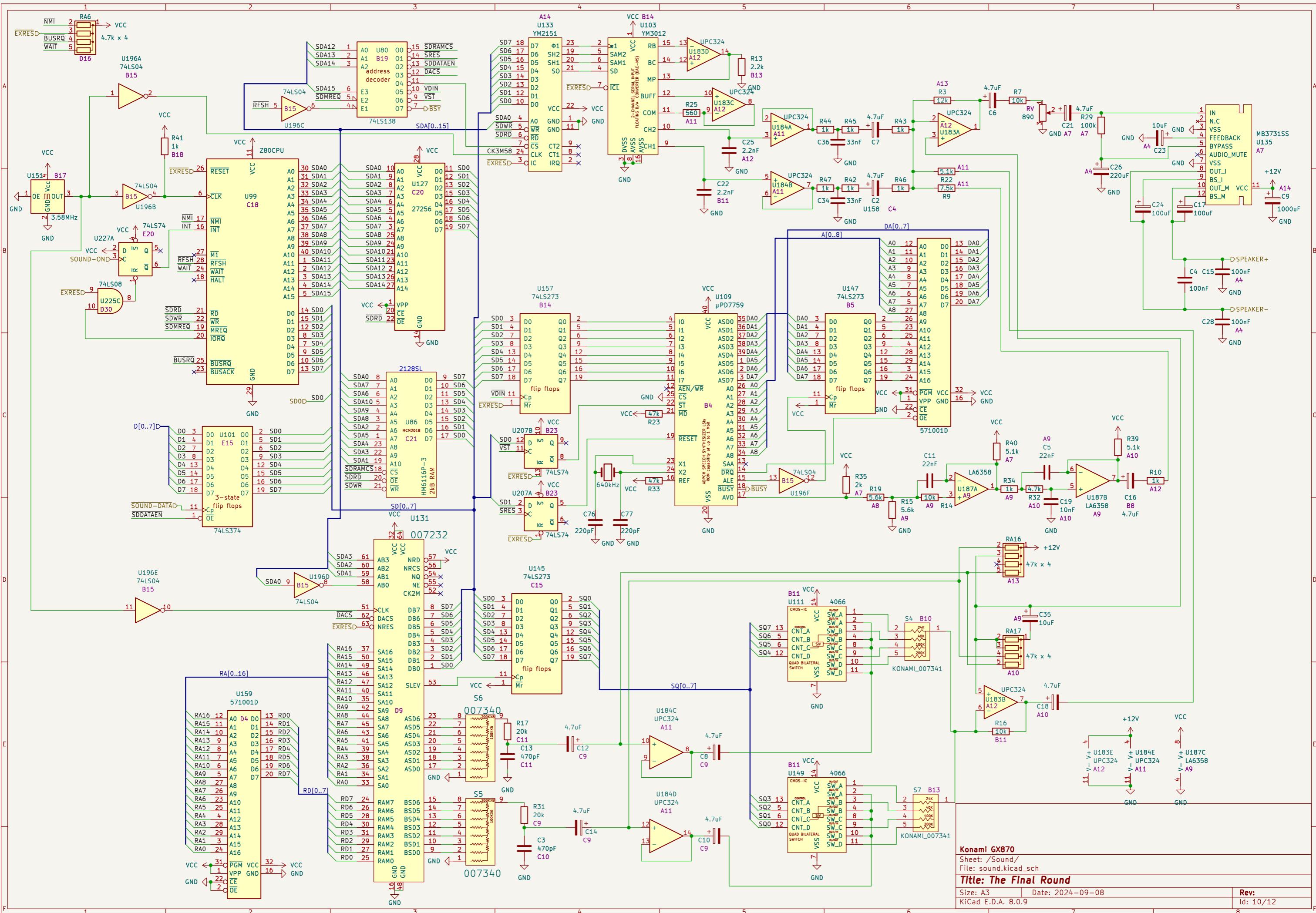
Sheet: /Timing/  
File: timing.kicad\_sch

Title: The Final Round

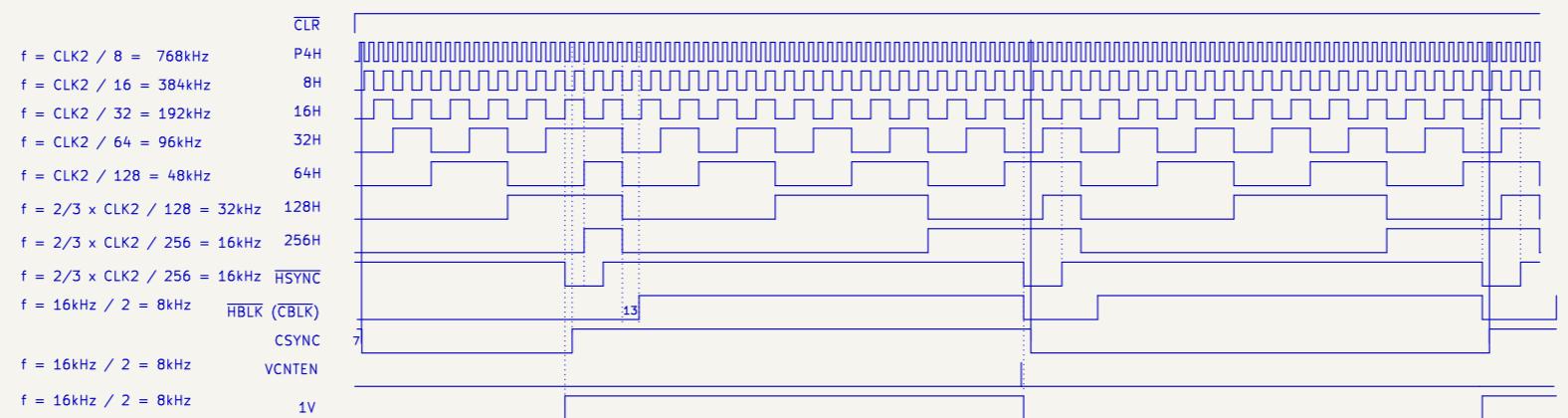
Size: A3 | Date: 2024-09-08  
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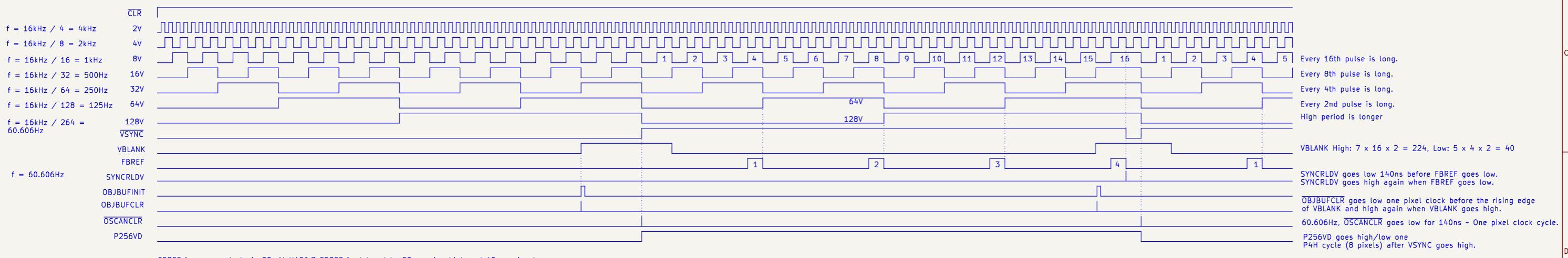
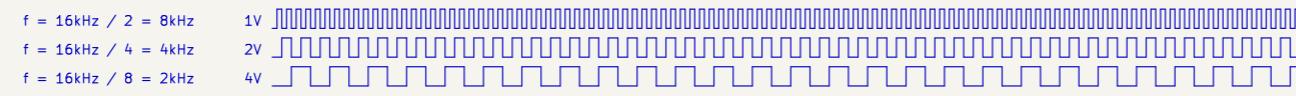
## Horizontal signals



- The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

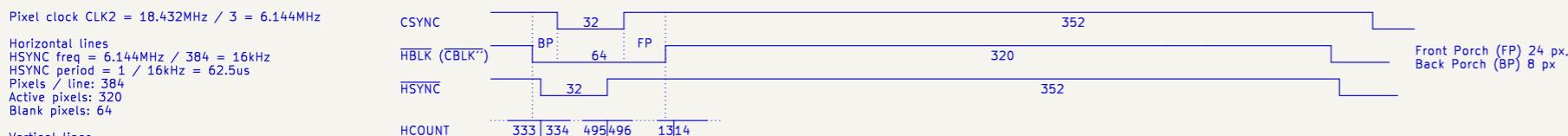
- CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals



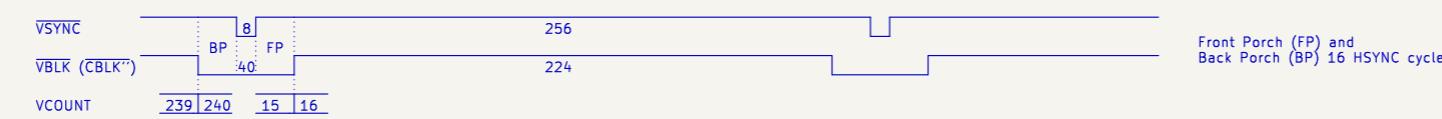
## Horizontal and vertical synch timing diagrams

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.  
All edges are synchronised to the rising edge of CLK2.



Front Porch (FP) 24 px,  
Back Porch (BP) 8 px

The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.  
All edges are synchronised to the falling edge of HSYNC.



Front Porch (FP) and  
Back Porch (BP) 16 HSYNC cycles.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]  
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK<sup>''</sup> is at the output of color mixer.

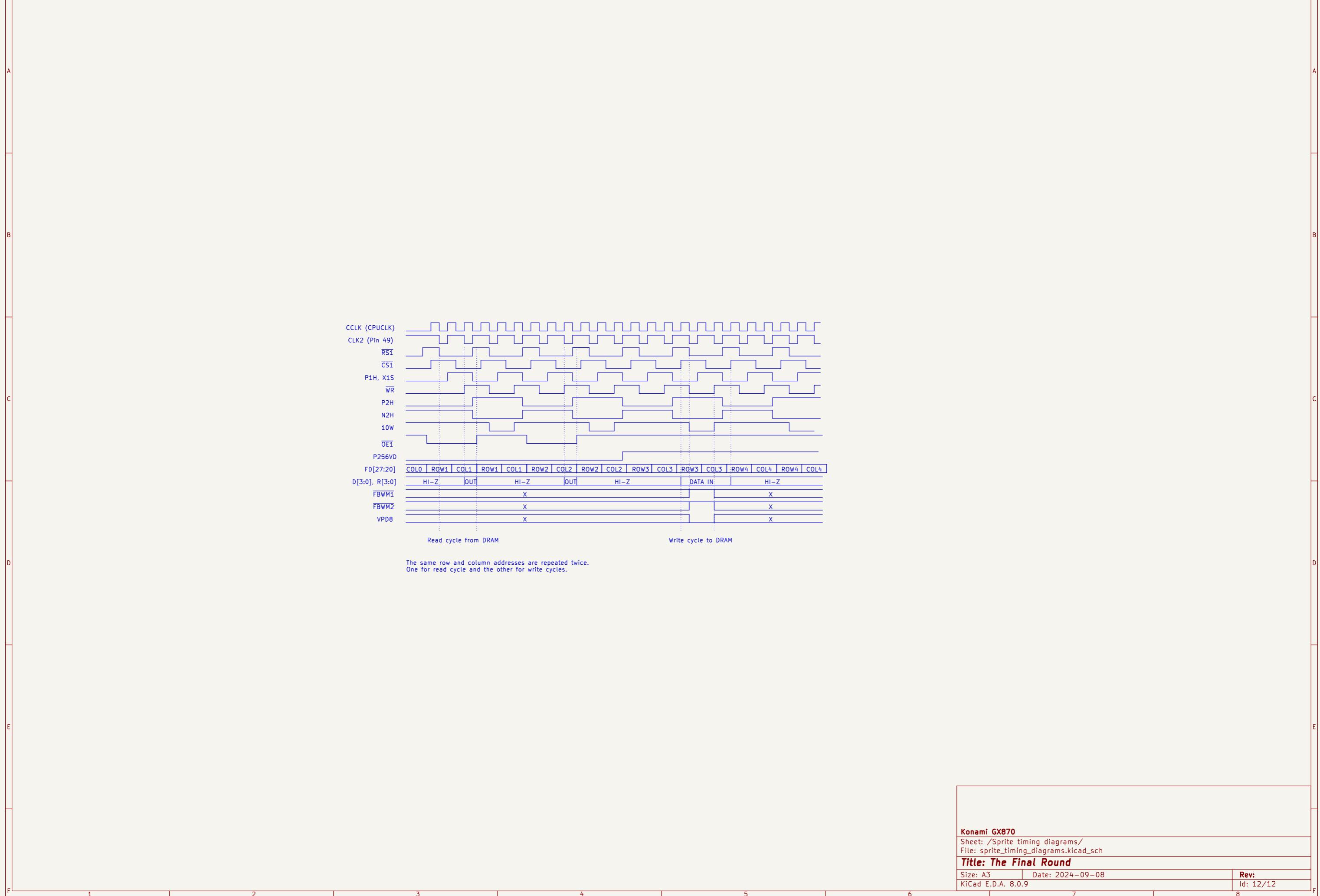
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Sheet: /Timing diagrams/  
File: timing\_diagrams.kicad\_sch

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Sheet: /Sprite timing diagrams/  
File: sprite\_timing\_diagrams.kicad\_sch

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