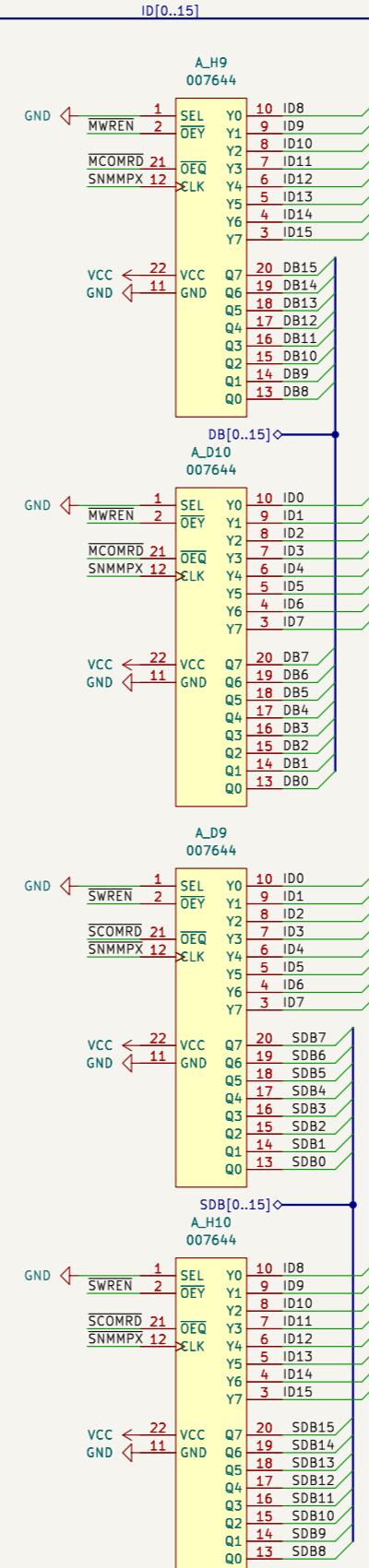
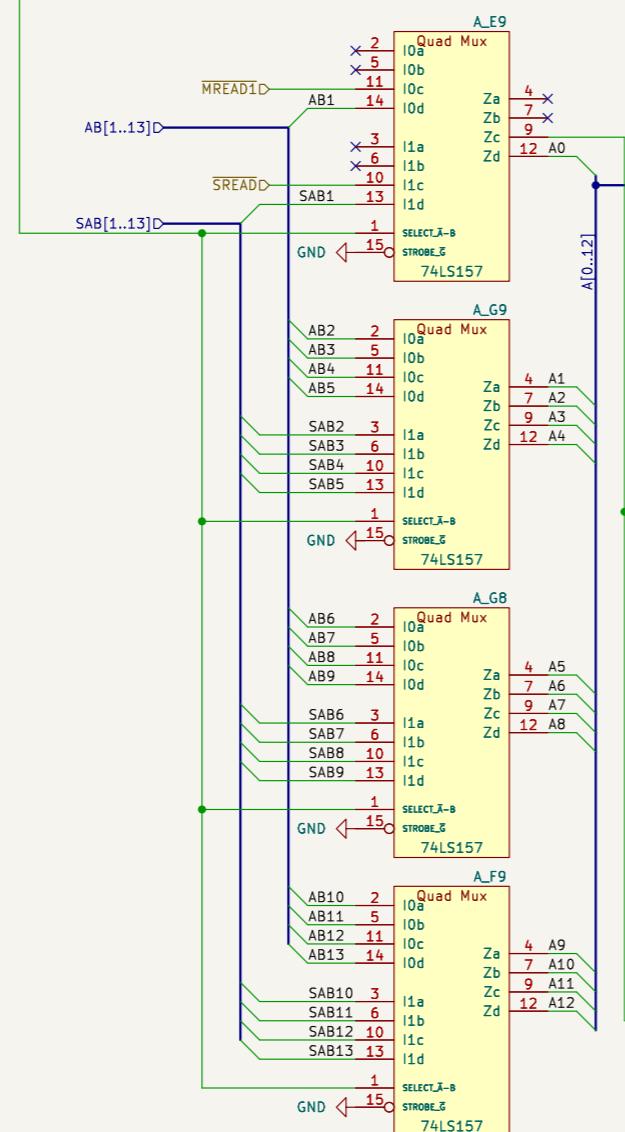
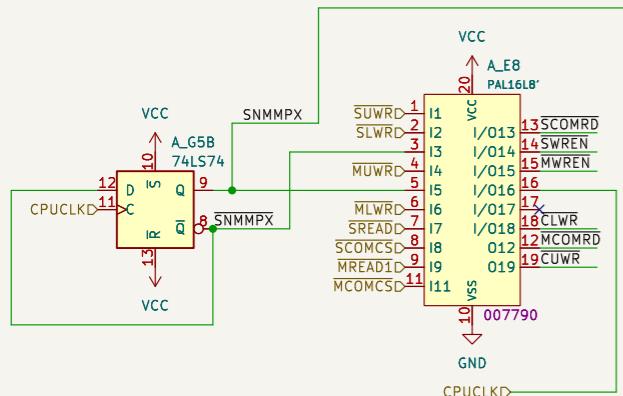


Konami 007790

$MCOMRD = \neg(MREAD1 \& \neg MCOMCS) = MREAD1 \mid MCOMCS$
 $SCOMRD = \neg(SREAD \& \neg SCOMCS)$
 $SWREN = \neg(SNMMPPX \& SREAD \& \neg SCOMCS)$
 $MWREN = \neg(SNMMPPX \& MREAD1 \& \neg MCOMCS)$
 $CLWR = \neg(CLWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$
 $CUWR = \neg(CUWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg MUWR \& \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$

A All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16LB device it is kept in that form. The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



A_H9
007644

GND 1 SEL Y0 10 ID8
MWREN 2 OEN Y1 9 ID9
SCOMRD 21 OEQ Y2 8 ID10
SNMMPPX 12 CLK Y3 7 ID11
Y4 6 ID12
Y5 5 ID13
Y6 4 ID14
Y7 3 ID15

VCC 22 VCC Q7 20 DB15
GND 11 GND Q6 19 DB14
Q5 18 DB13
Q4 17 DB12
Q3 16 DB11
Q2 15 DB10
Q1 14 DB9
Q0 13 DB8

DB[0..15] 10 ID8
A_D10 007644

GND 1 SEL Y0 10 ID0
MWREN 2 OEN Y1 9 ID1
SCOMRD 21 OEQ Y2 8 ID2
SNMMPPX 12 CLK Y3 7 ID3
Y4 6 ID4
Y5 5 ID5
Y6 4 ID6
Y7 3 ID7

VCC 22 VCC Q7 20 DB7
GND 11 GND Q6 19 DB6
Q5 18 DB5
Q4 17 DB4
Q3 16 DB3
Q2 15 DB2
Q1 14 DB1
Q0 13 DB0

A_D9 007644

GND 1 SEL Y0 10 ID0
SWREN 2 OEN Y1 9 ID1
SCOMRD 21 OEQ Y2 8 ID2
SNMMPPX 12 CLK Y3 7 ID3
Y4 6 ID4
Y5 5 ID5
Y6 4 ID6
Y7 3 ID7

VCC 22 VCC Q7 20 SDB7
GND 11 GND Q6 19 SDB6
Q5 18 SDB5
Q4 17 SDB4
Q3 16 SDB3
Q2 15 SDB2
Q1 14 SDB1
Q0 13 SDB0

SDB[0..15] 10 ID8
A_H10 007644

GND 1 SEL Y0 10 ID8
SWREN 2 OEN Y1 9 ID9
SCOMRD 21 OEQ Y2 8 ID10
SNMMPPX 12 CLK Y3 7 ID11
Y4 6 ID12
Y5 5 ID13
Y6 4 ID14
Y7 3 ID15

VCC 22 VCC Q7 20 SDB15
GND 11 GND Q6 19 SDB14
Q5 18 SDB13
Q4 17 SDB12
Q3 16 SDB11
Q2 15 SDB10
Q1 14 SDB9
Q0 13 SDB8

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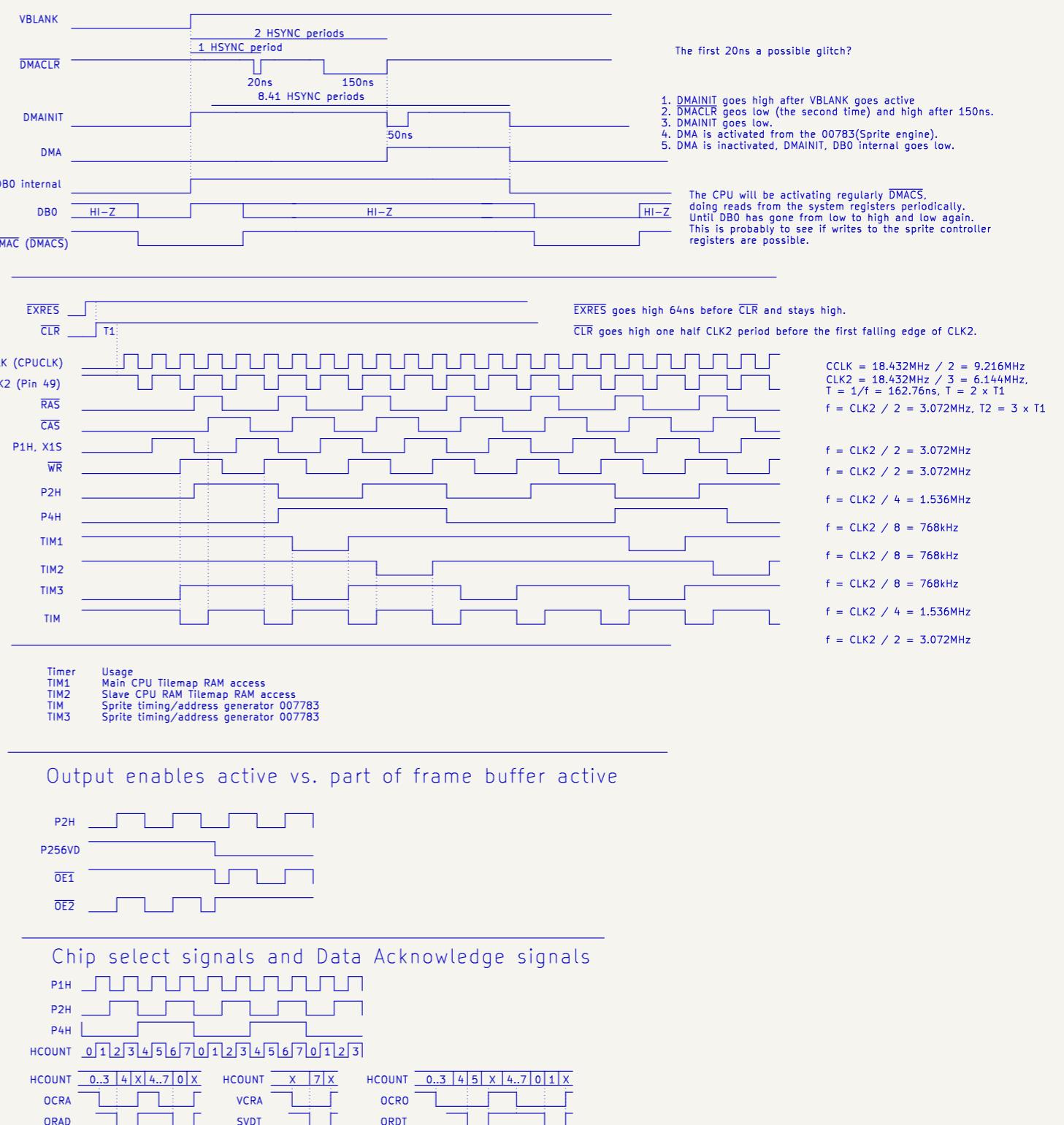
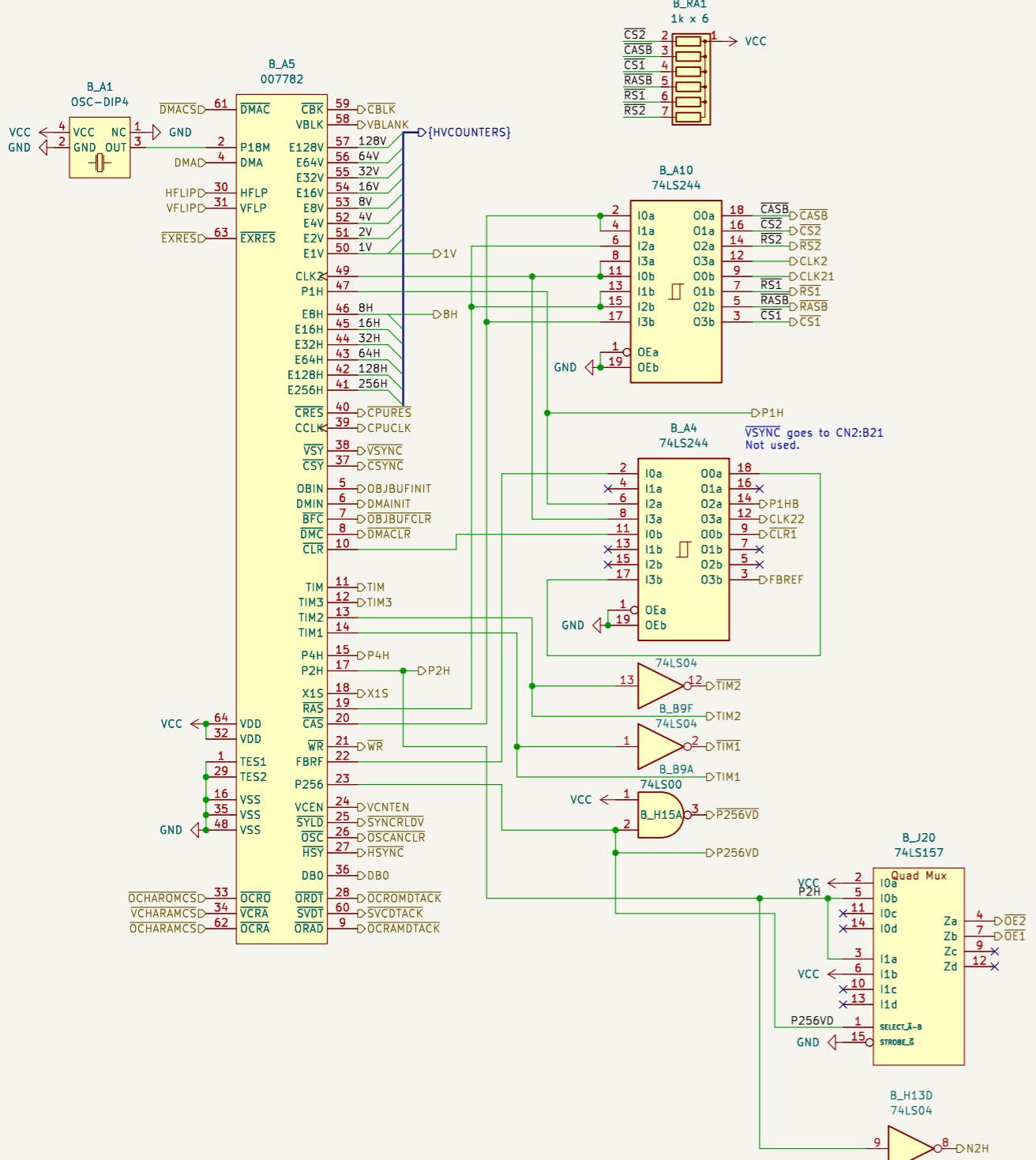
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File: shared_resources.kicad_sch

Title: Twin 16 – Rev B

Size: A3 Date: 2024-08-04
KiCad E.D.A. 8.0.4

Rev: Id: 4/20

DMA Synchronization



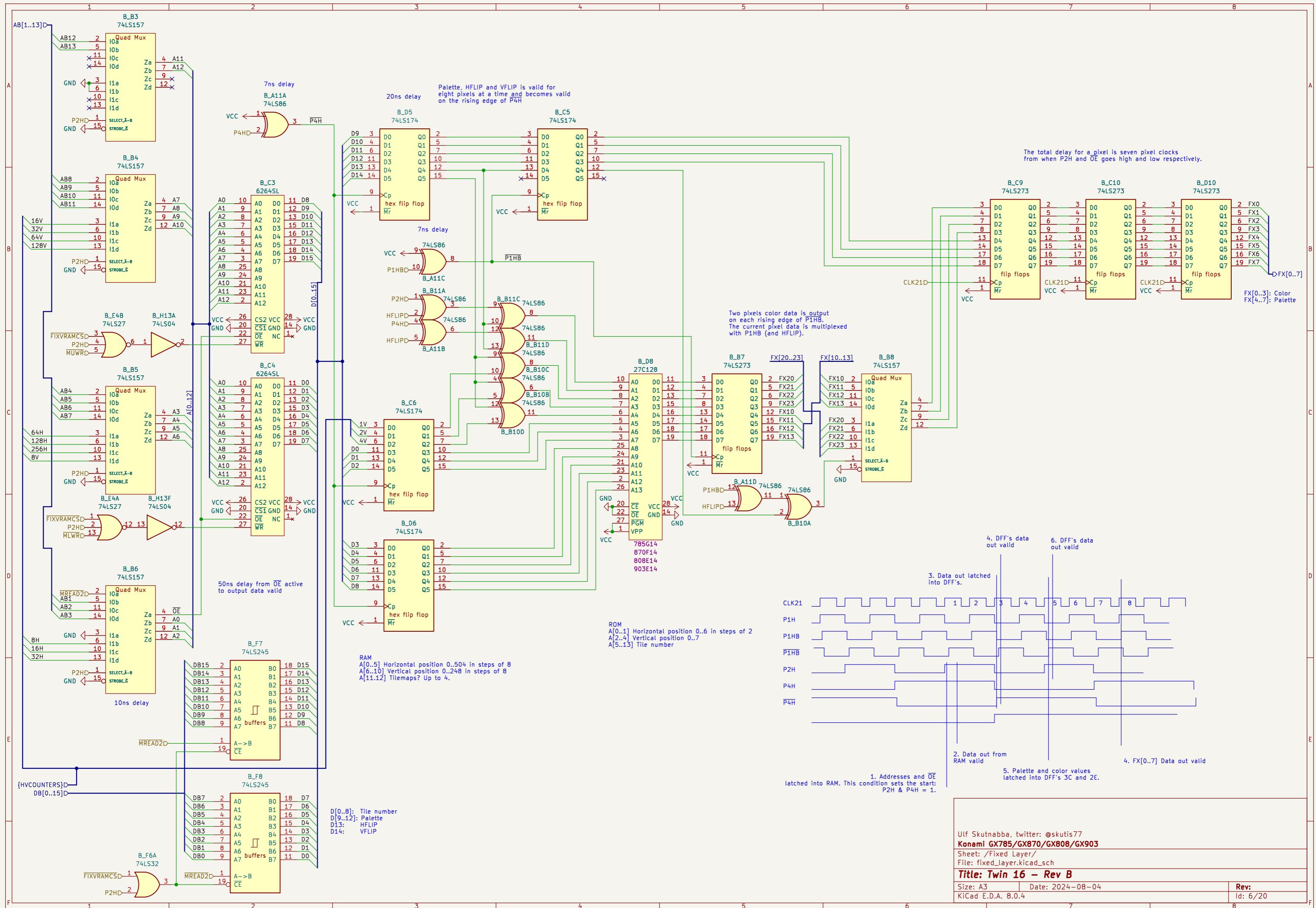
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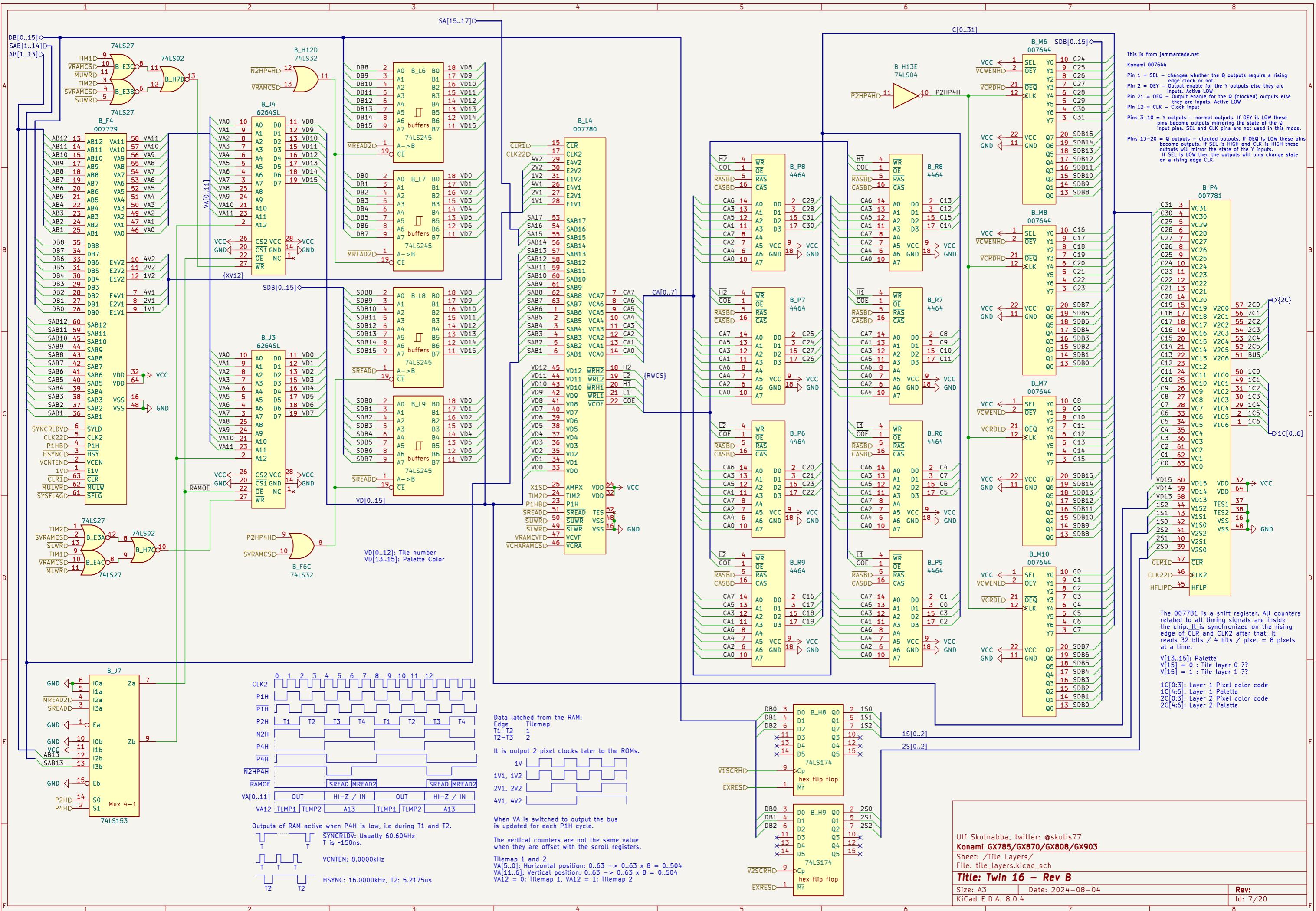
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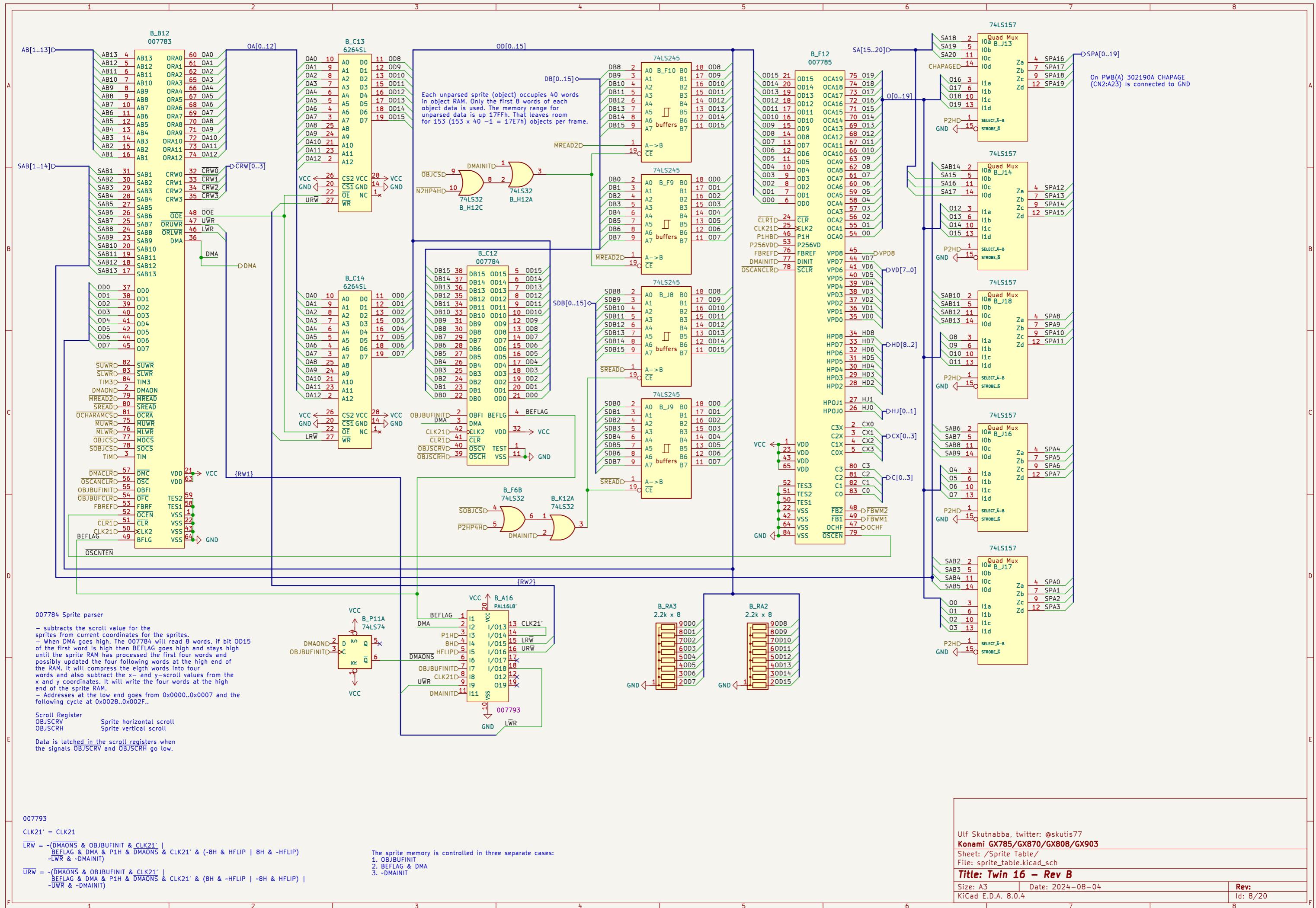
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Size: A3 Date: 2024-08-04
KiCad E.D.A. 8.0.4

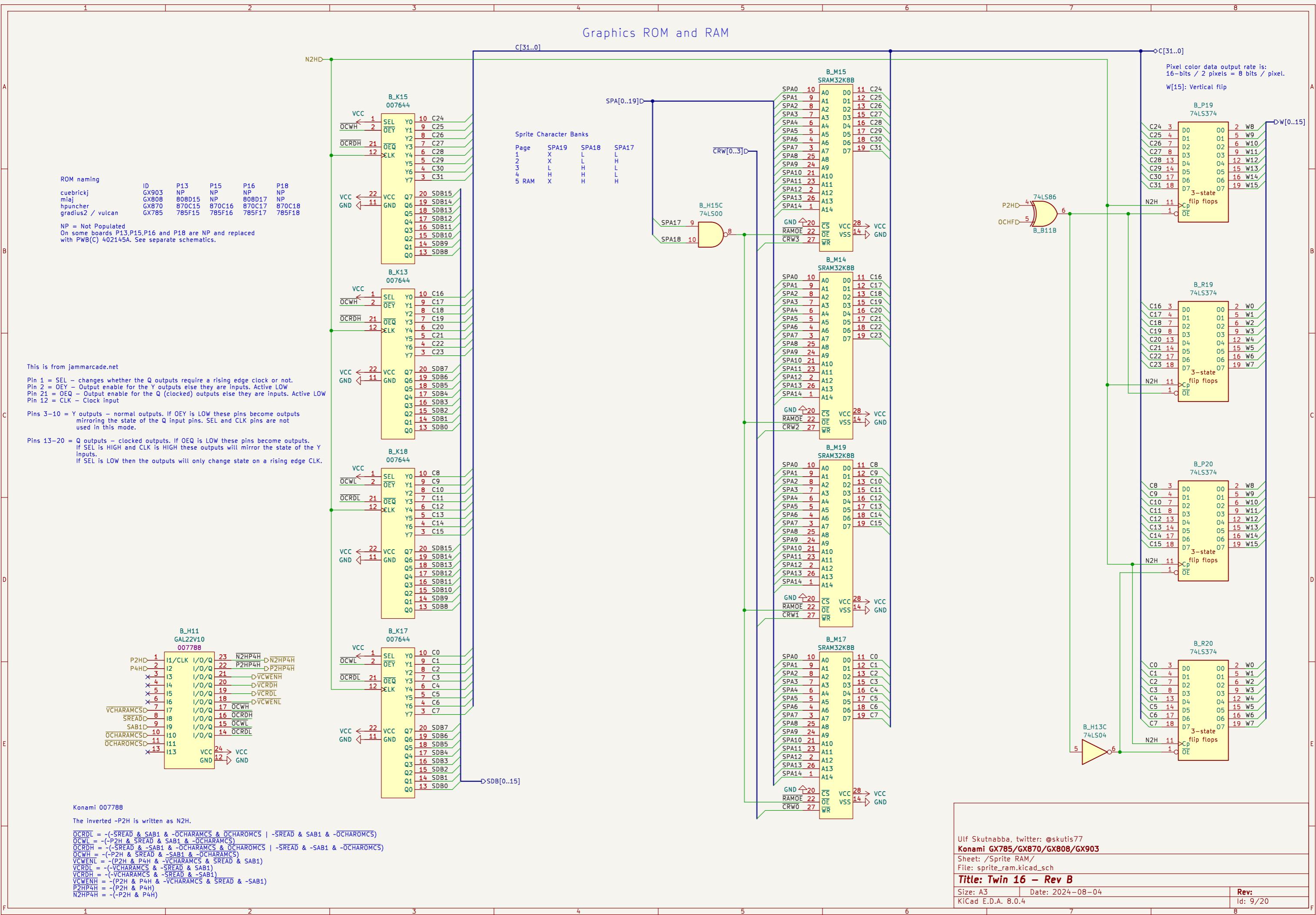
Rev: Id: 5/20

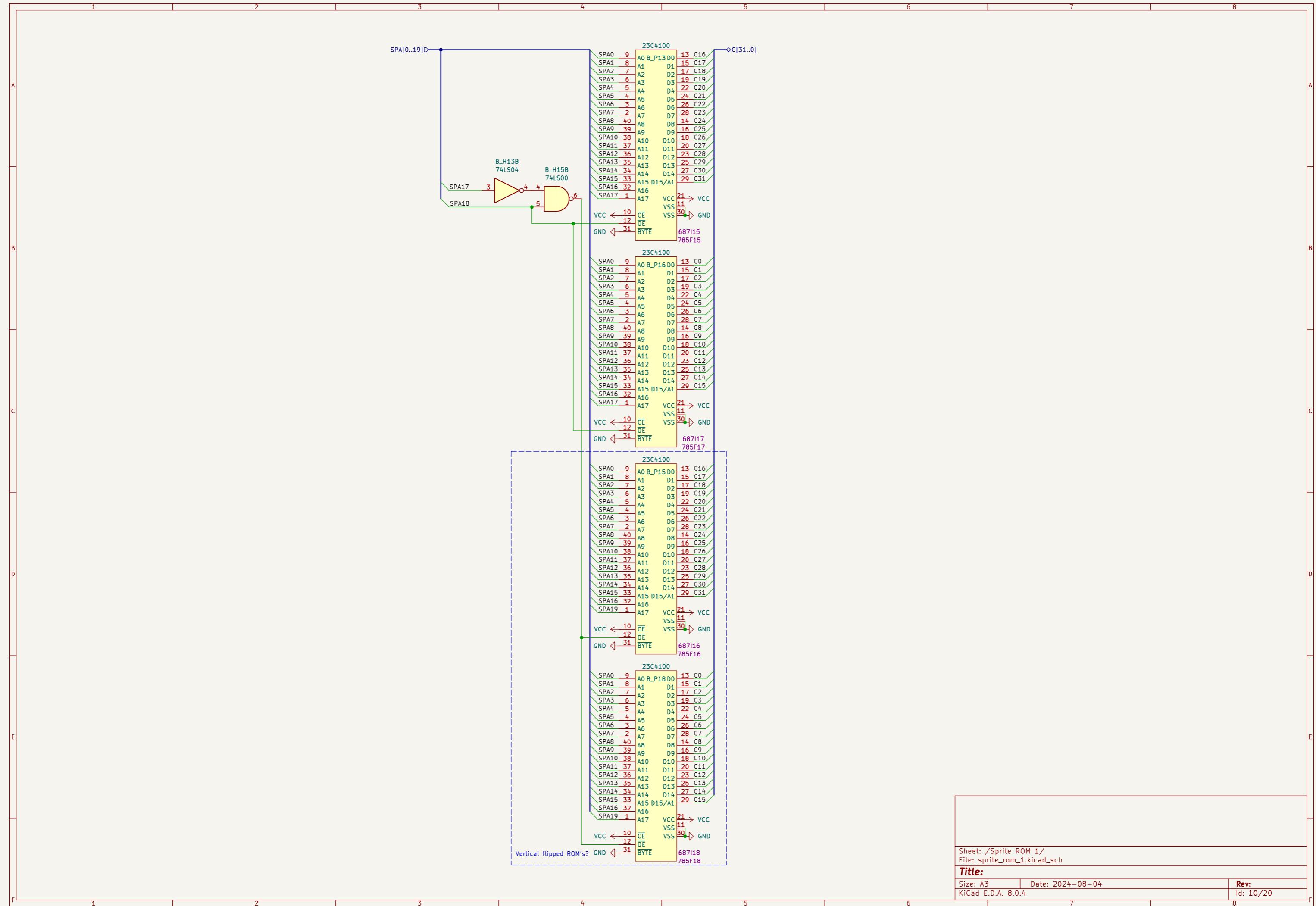






Graphics ROM and RAM



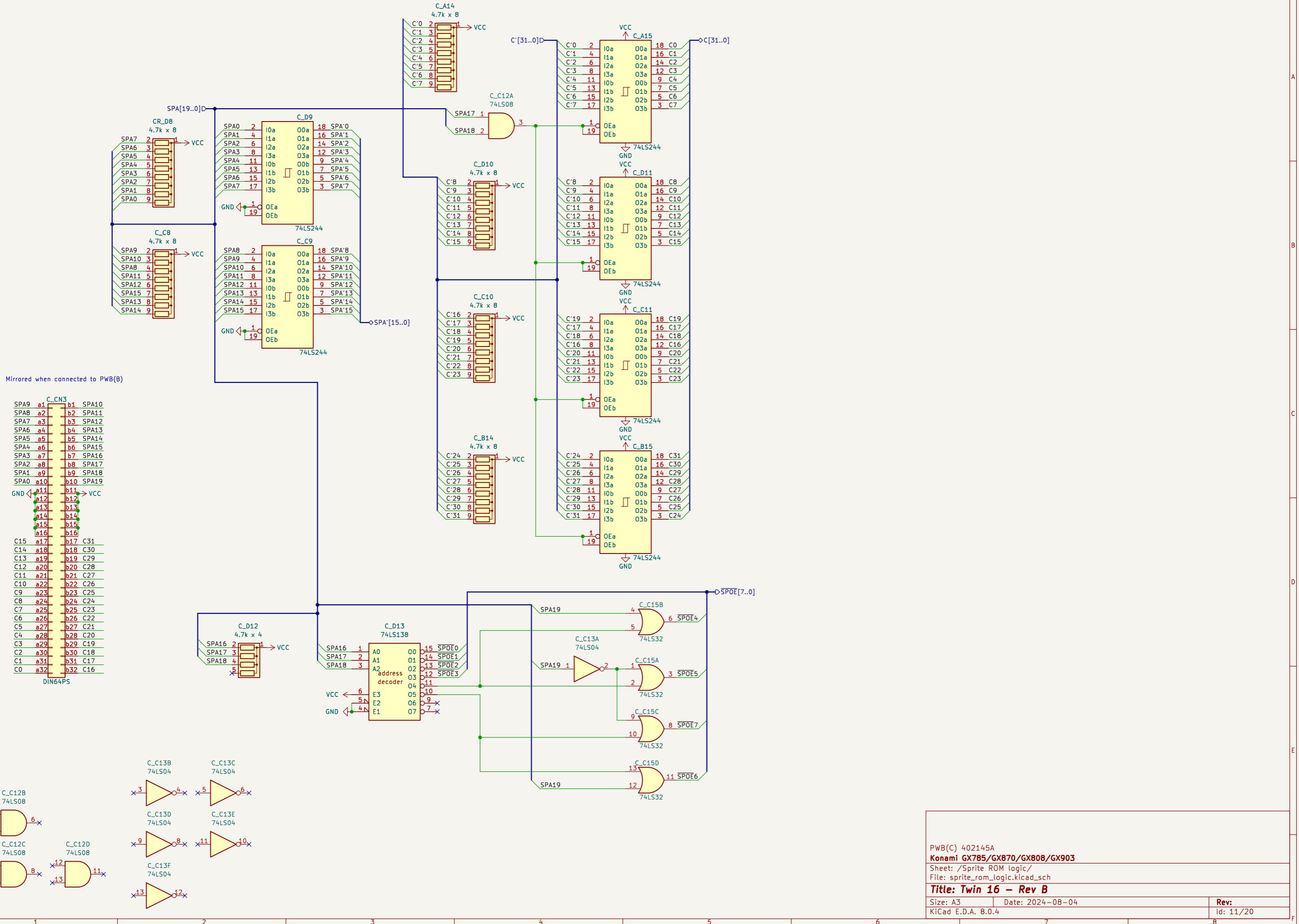


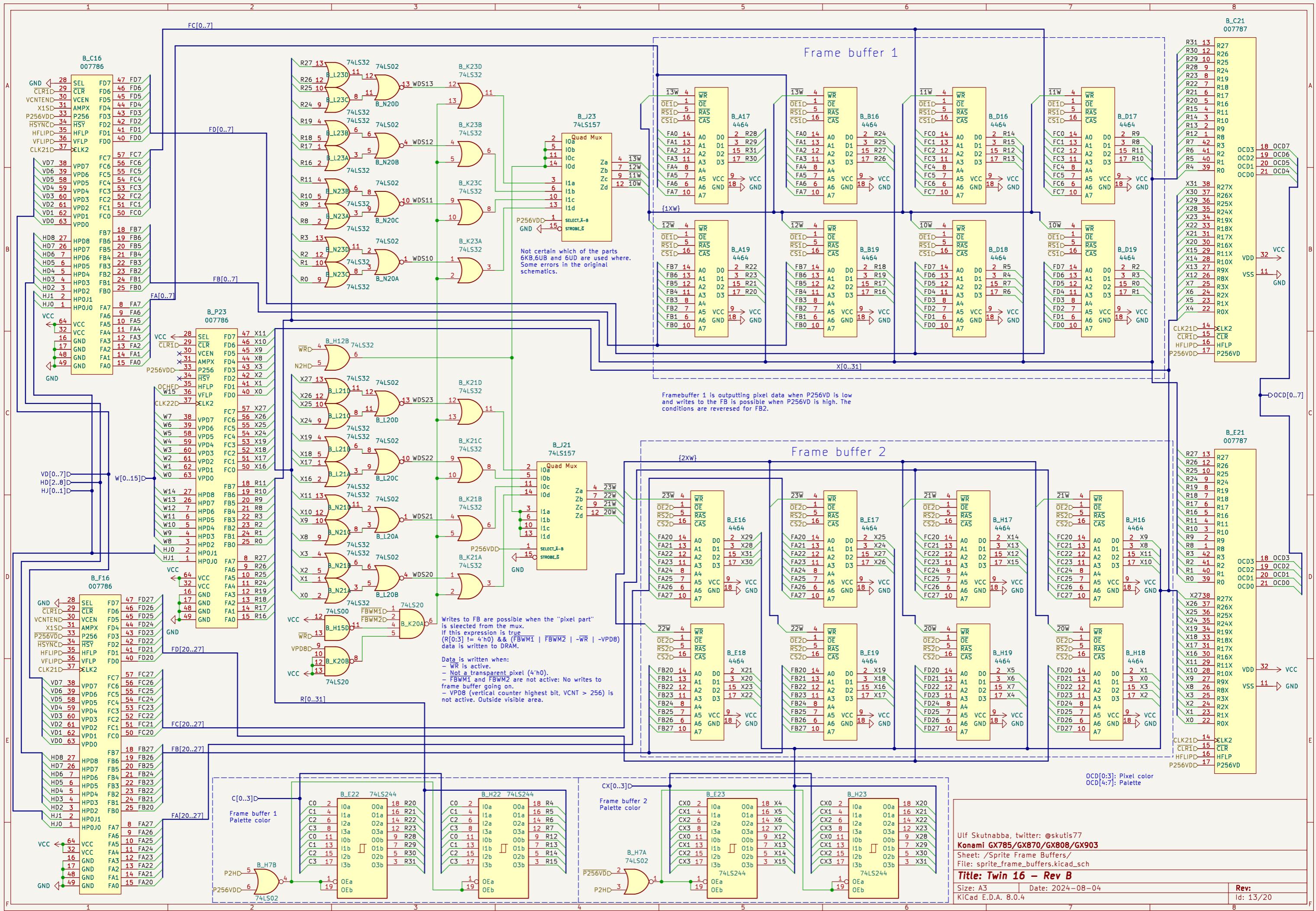
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File: sprite_rom_1.kicad_sch

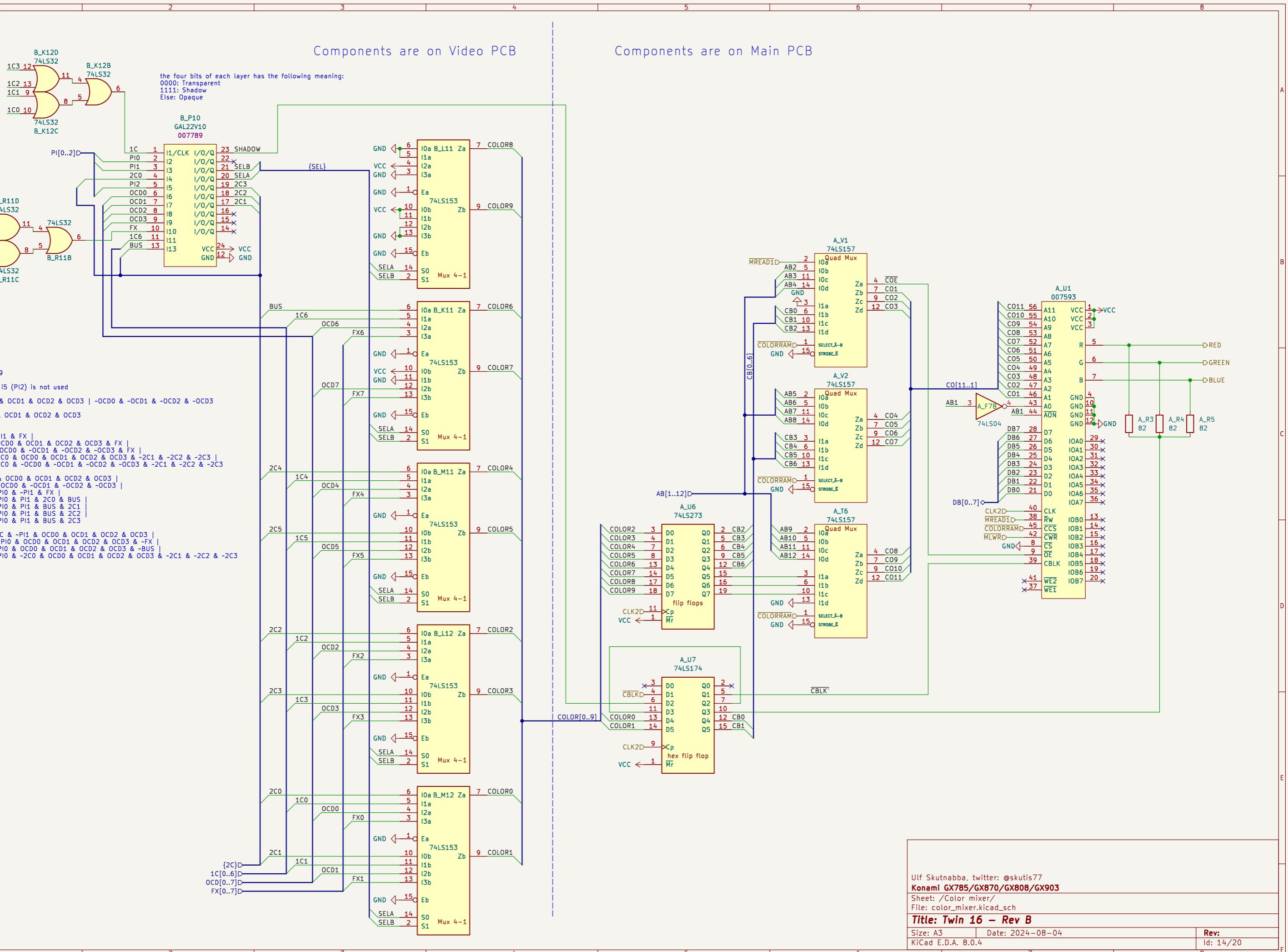
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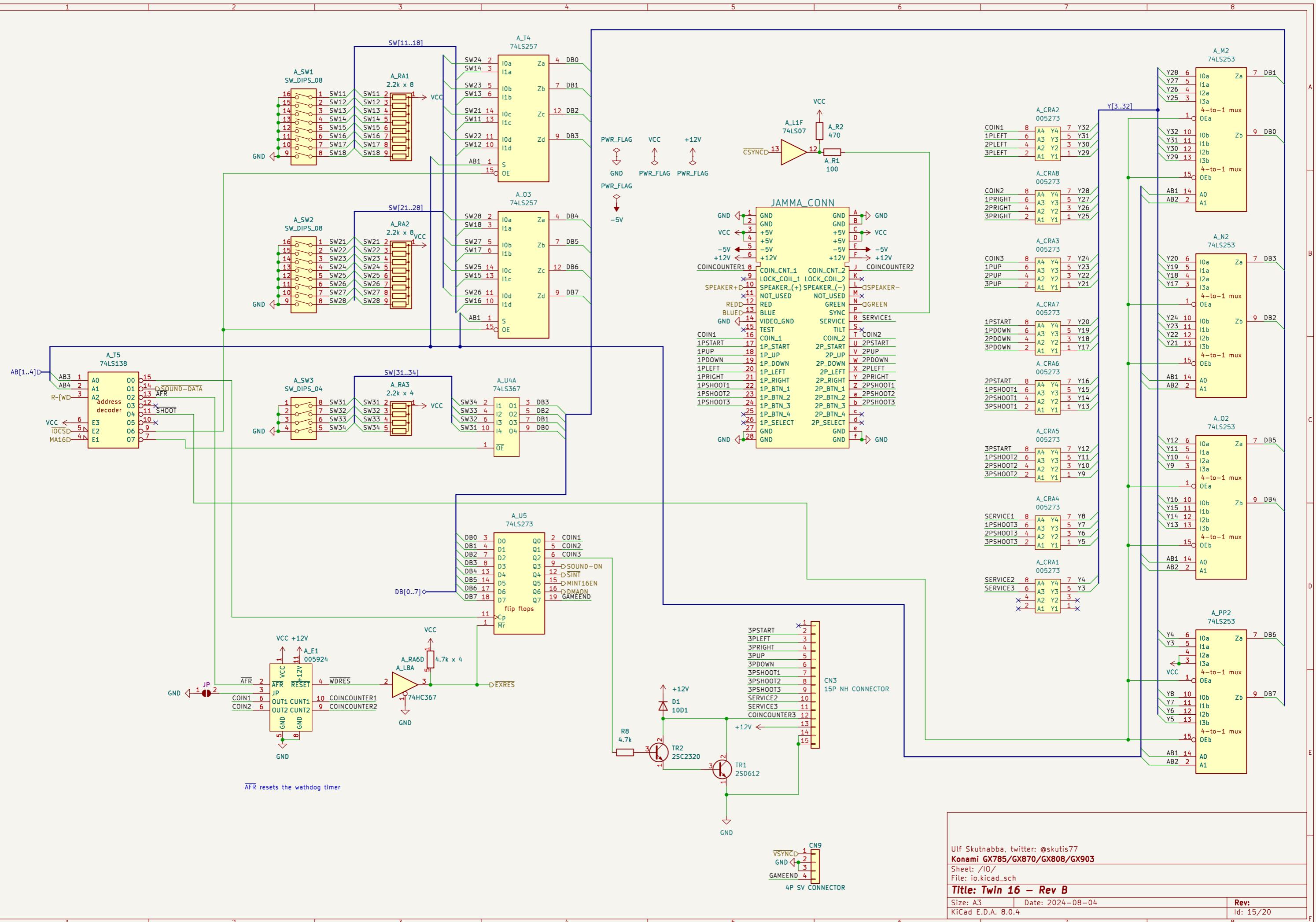
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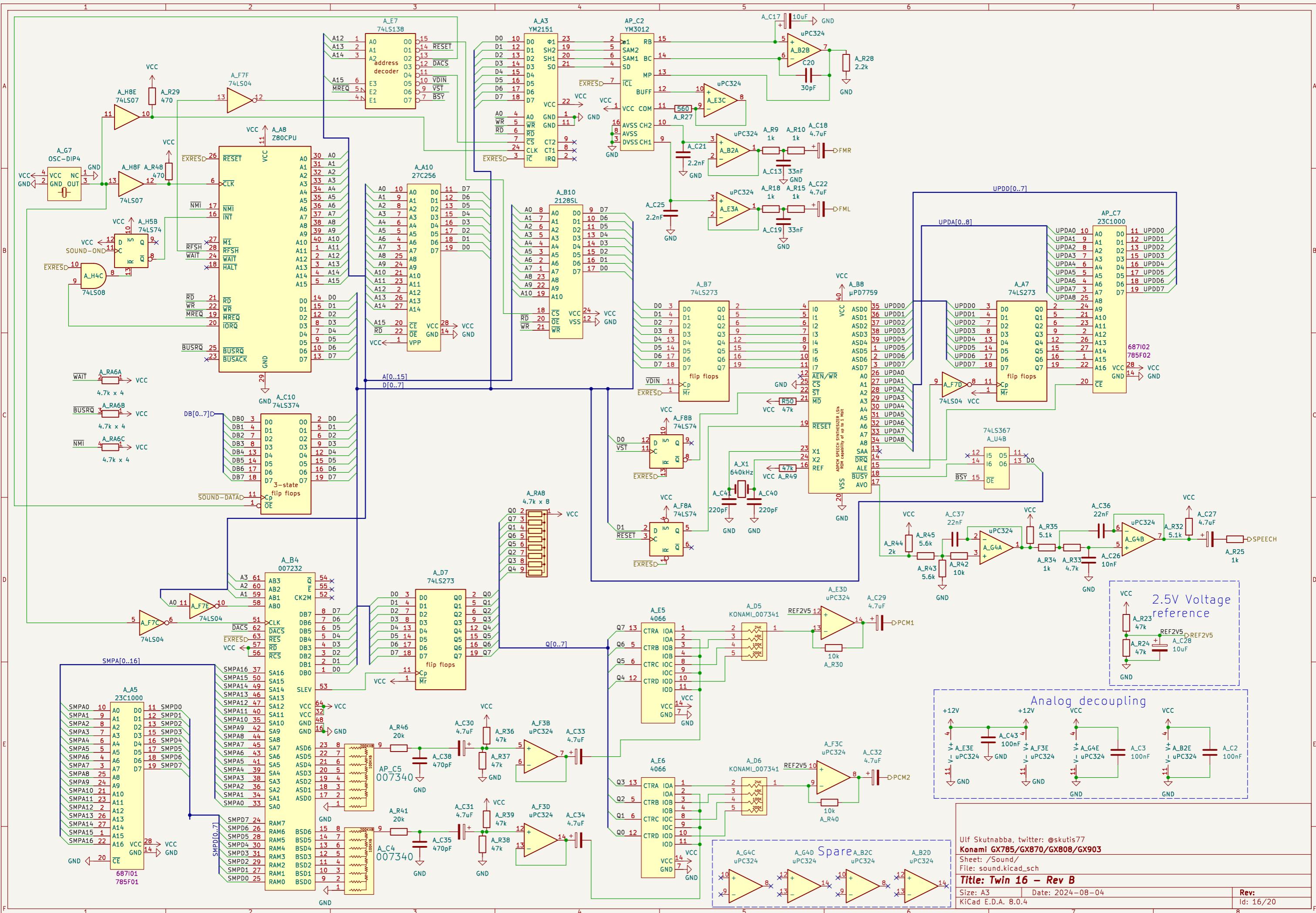
Rev:
Id: 10/20

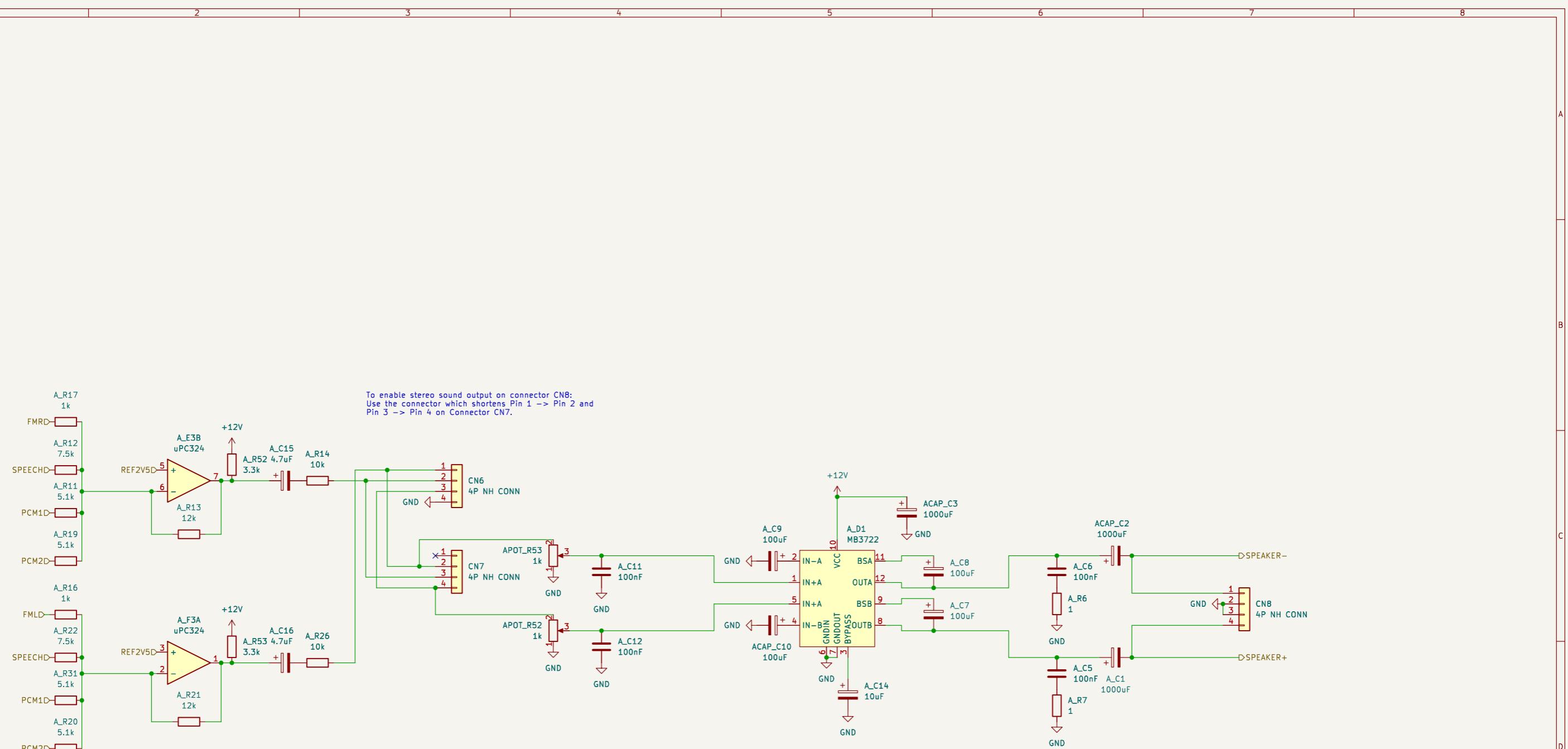












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Sheet: /Sound mixer/
File: sound_mixer.kicad_sch

Title: Twin 16 – Rev B

Size: A3 Date: 2024-08-04
KICad EDA 8.0.4

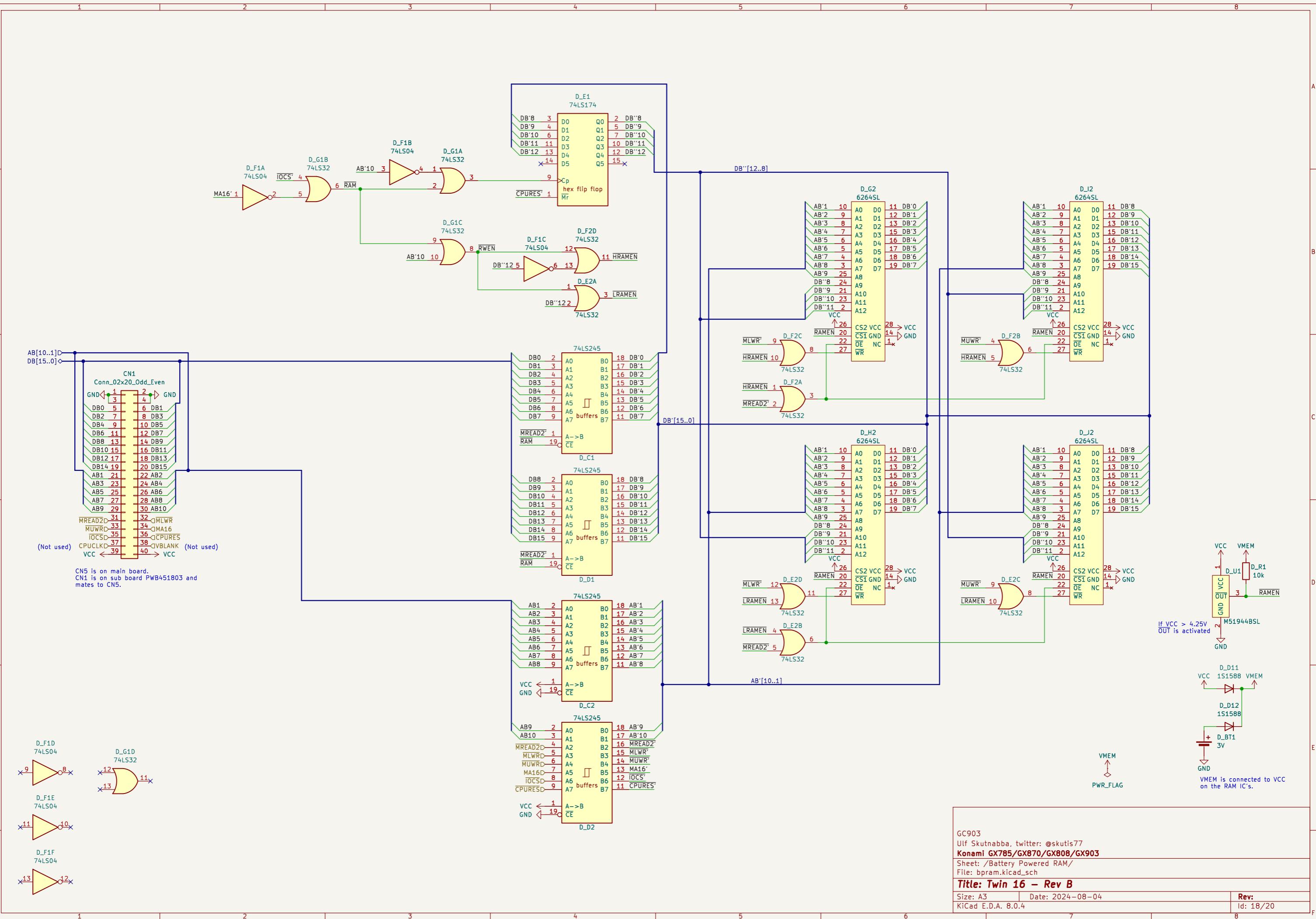
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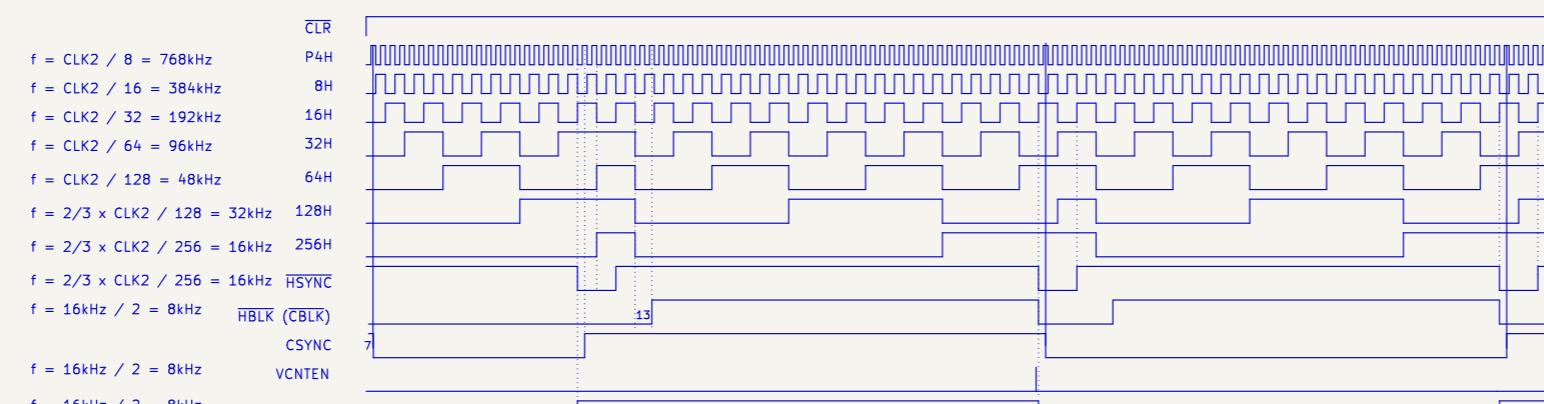
Rev:

Id: 17/2

3



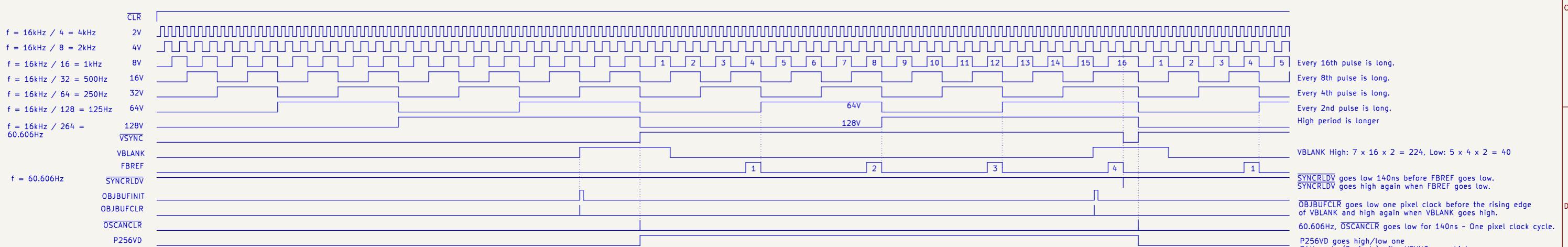
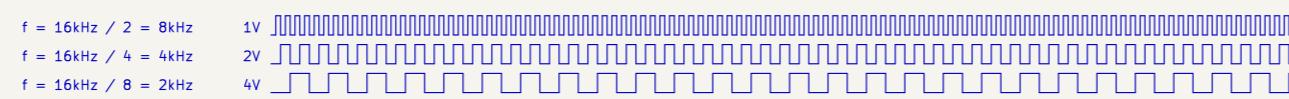
Horizontal signals



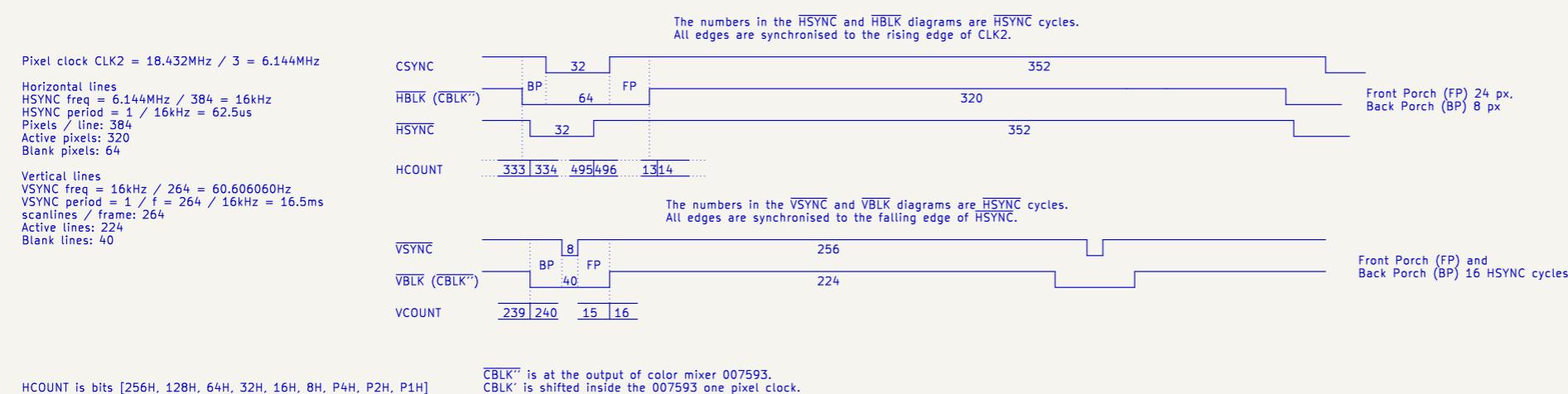
– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



Horizontal and vertical synch timing diagrams



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Sheet: /Timing diagrams/
File: timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

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Rev:
Id: 19/20

A

B

C

D

E

F

A

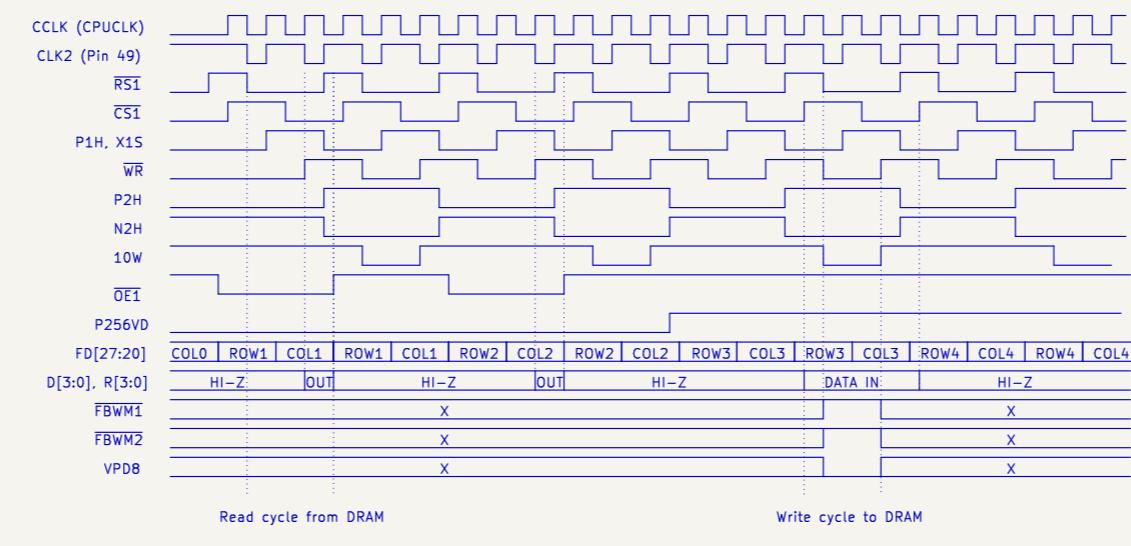
B

C

D

E

F



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Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

Size: A3 | Date: 2024-08-04
KiCad E.D.A. 8.0.4

Rev:
Id: 20/20