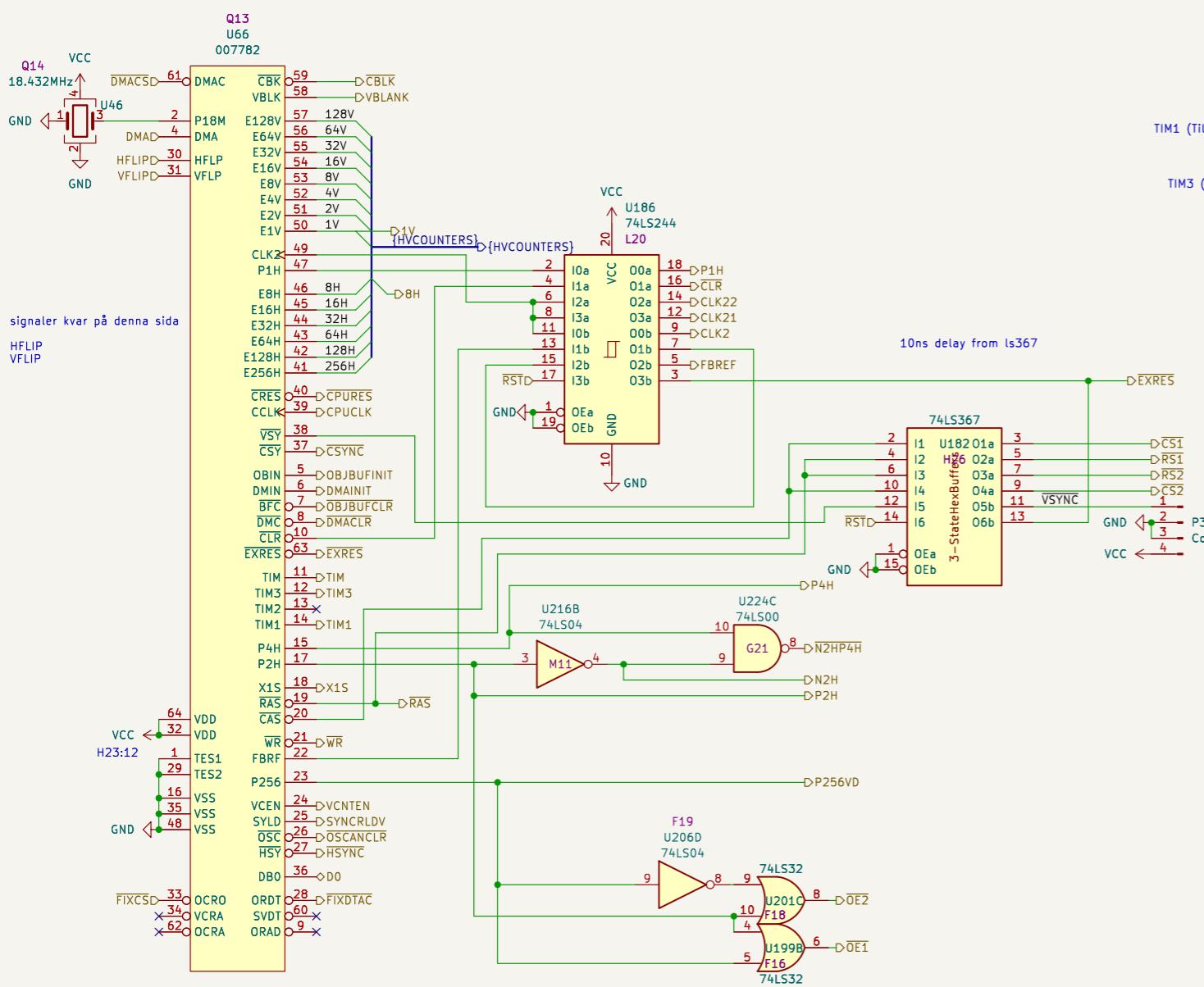
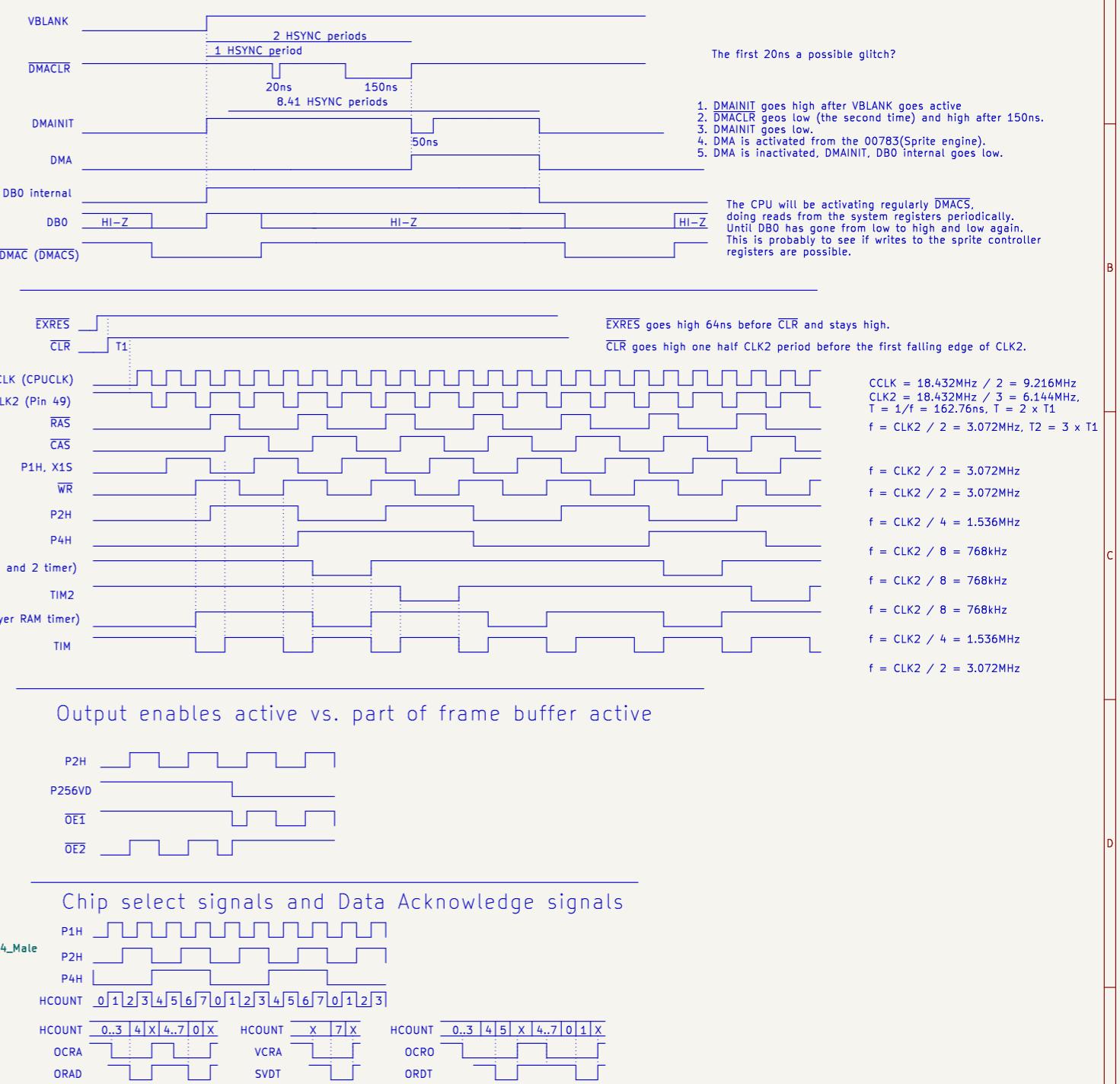


## DMA Synchronization



Pins 30 and 31 were swapped on the schematics.

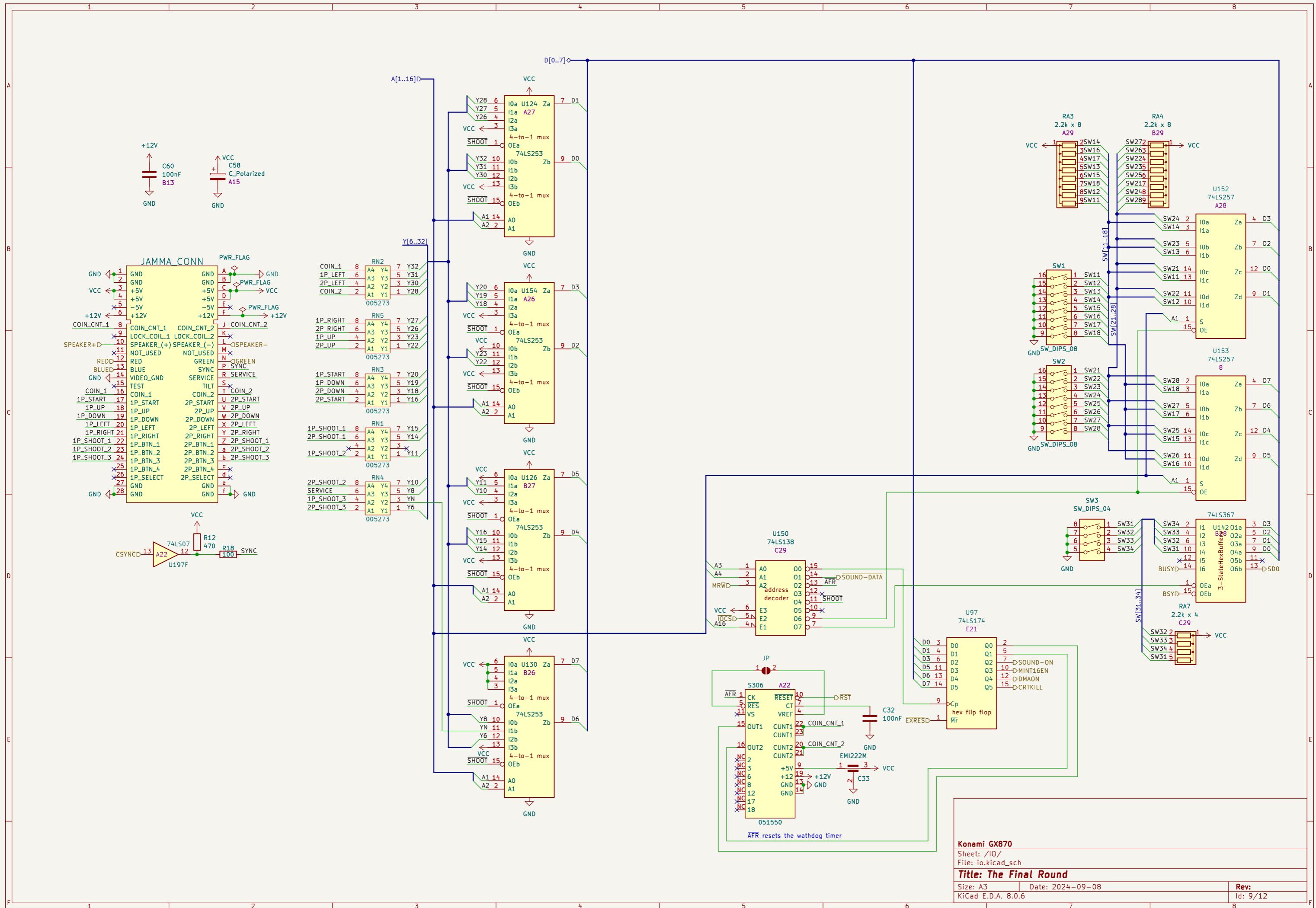


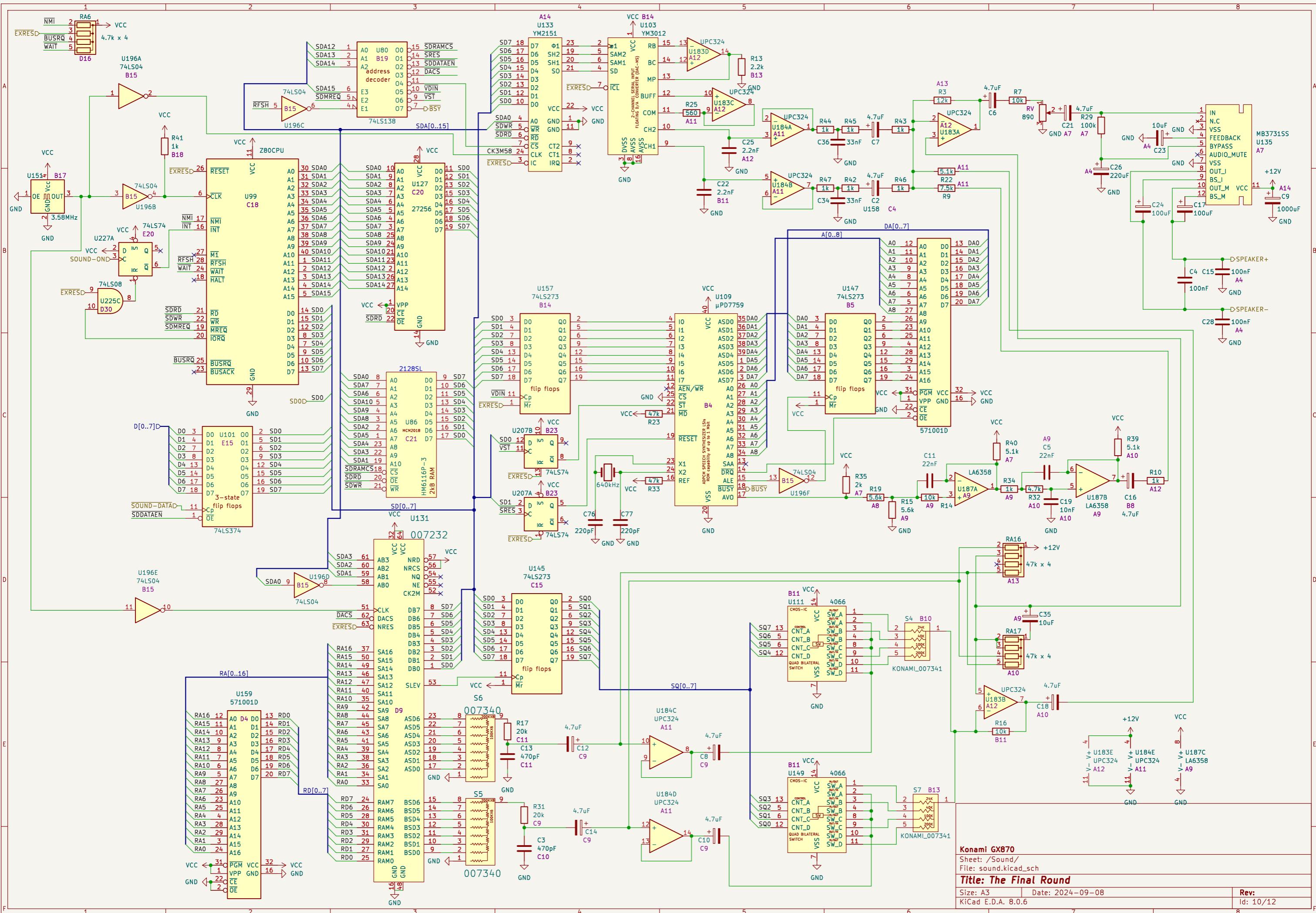
Timing  
**Konami GX870**  
Sheet: /Timing.  
File: timing.kicd

## Title: The Final Round

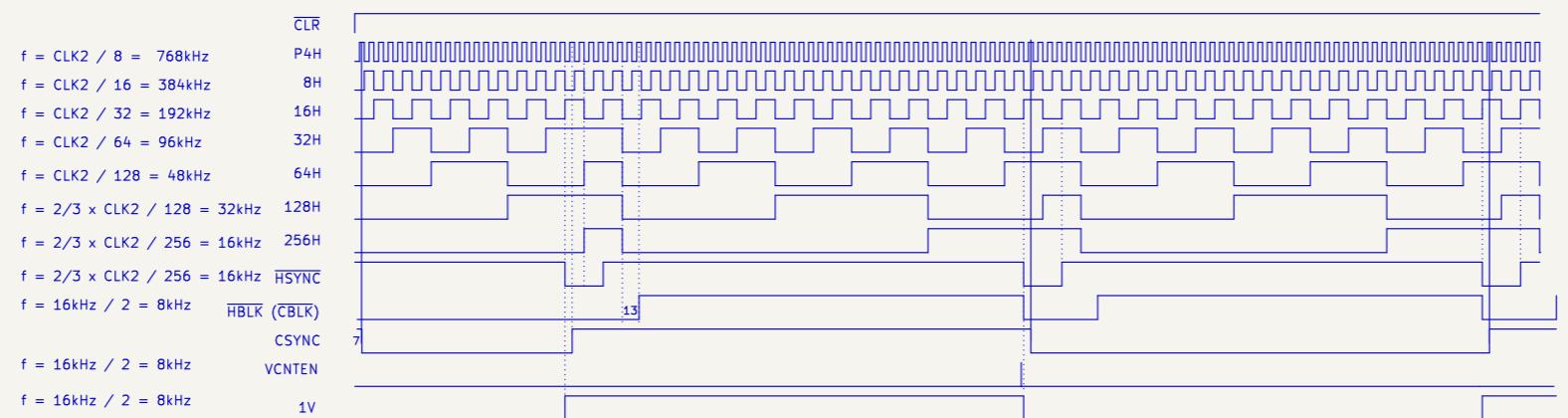
Size: A3 Date: 2024-09-08  
KiCad E.D.A. 8.0.6

**Rev:**  
Id: 8/12





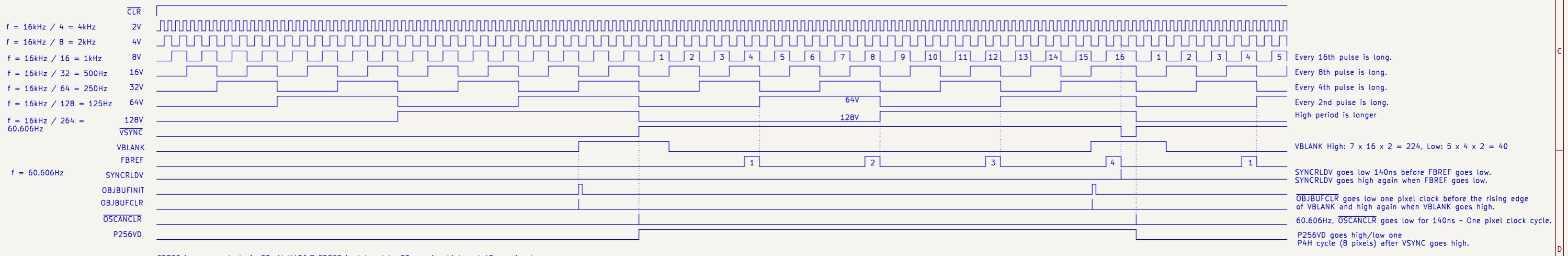
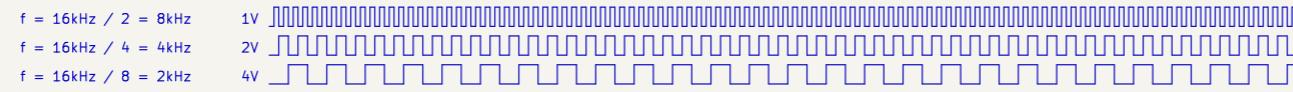
## Horizontal signals



- The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

- CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals



A

B

C

D

E

F

A

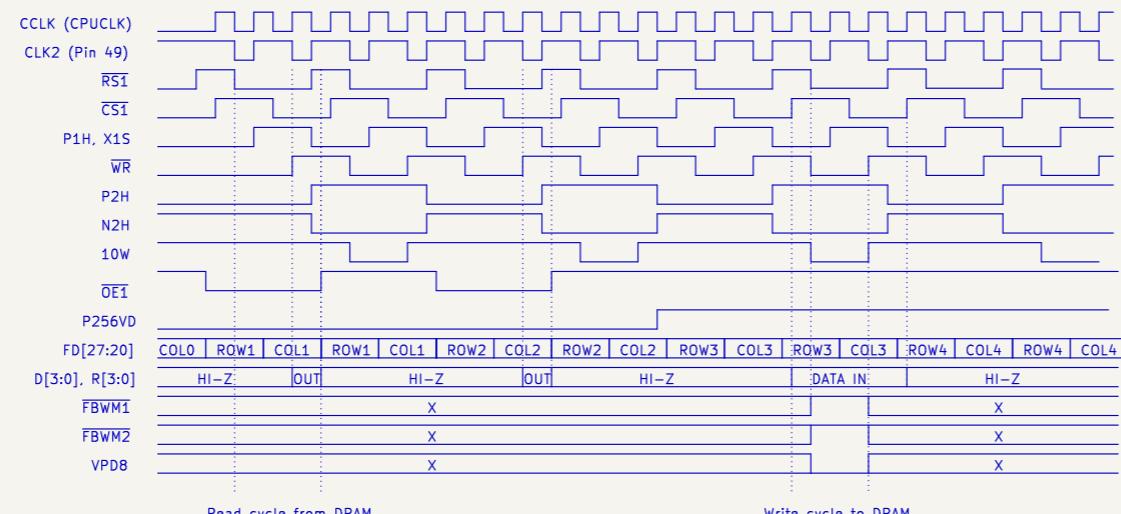
B

C

D

E

F

**Konami GX870**

Sheet: /Sprite timing diagrams/  
File: sprite\_timing\_diagrams.kicad\_sch

**Title: The Final Round**

Size: A3 | Date: 2024-09-08  
KiCad E.D.A. 8.0.6

Rev:  
Id: 12/12