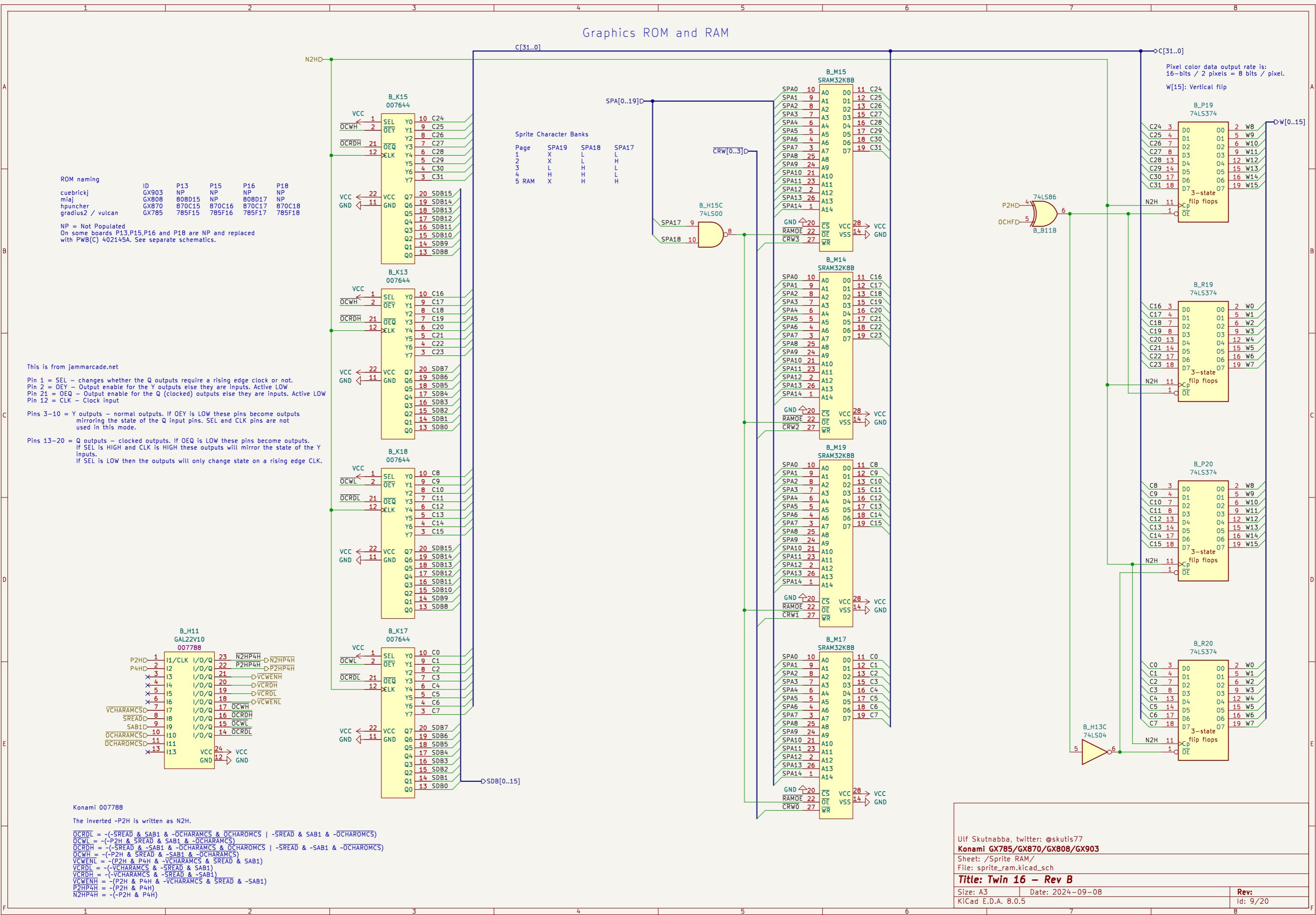
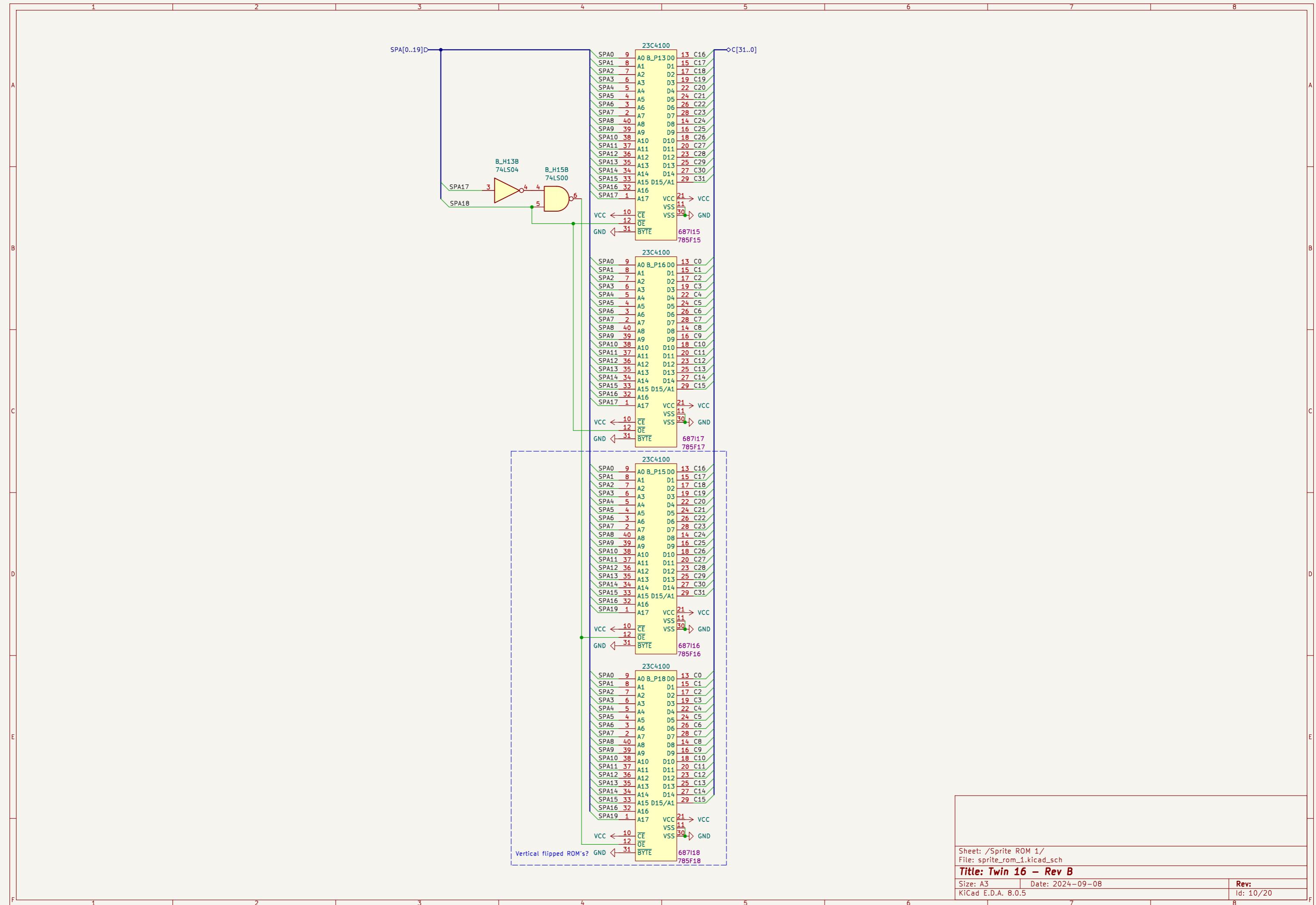
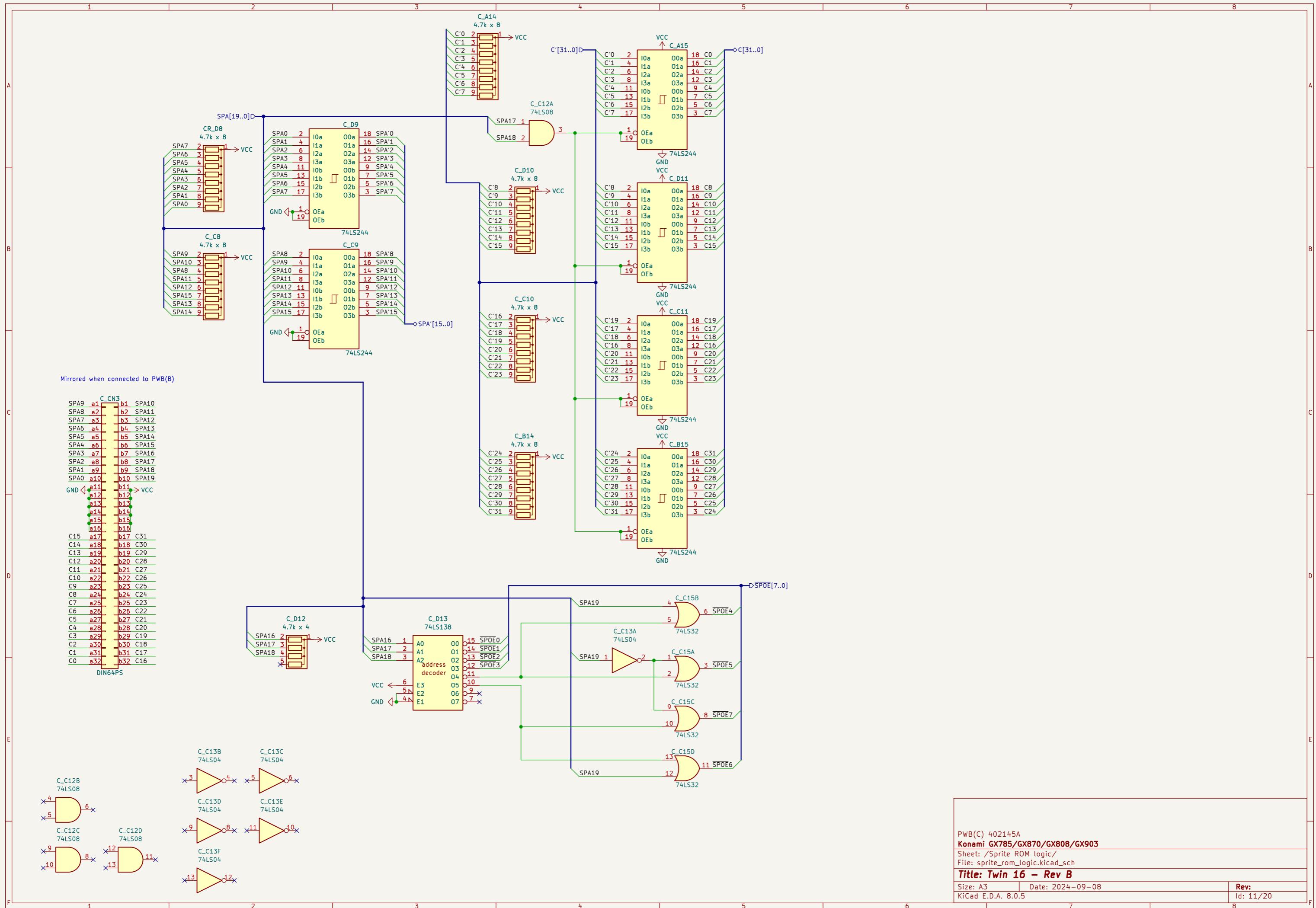
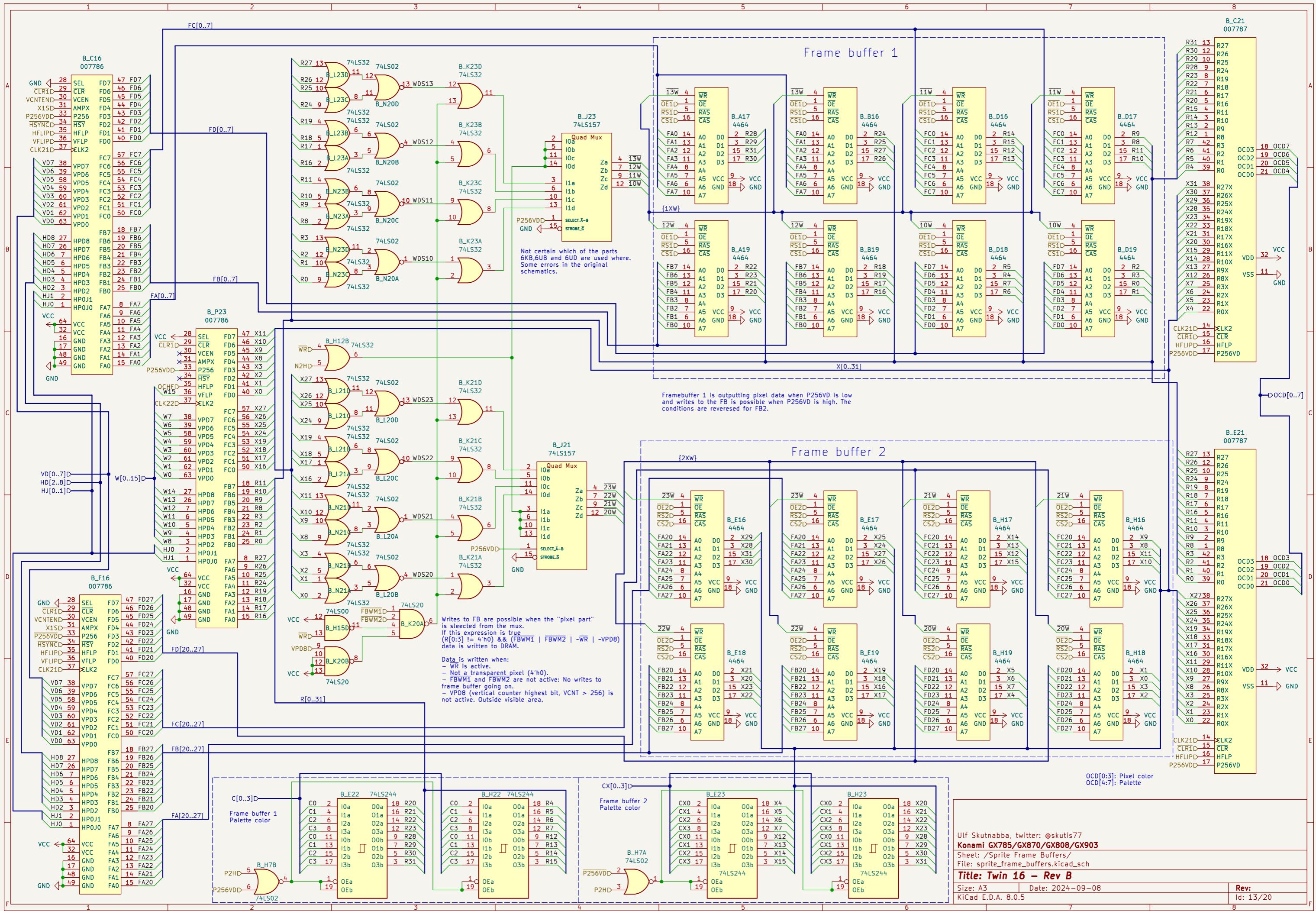


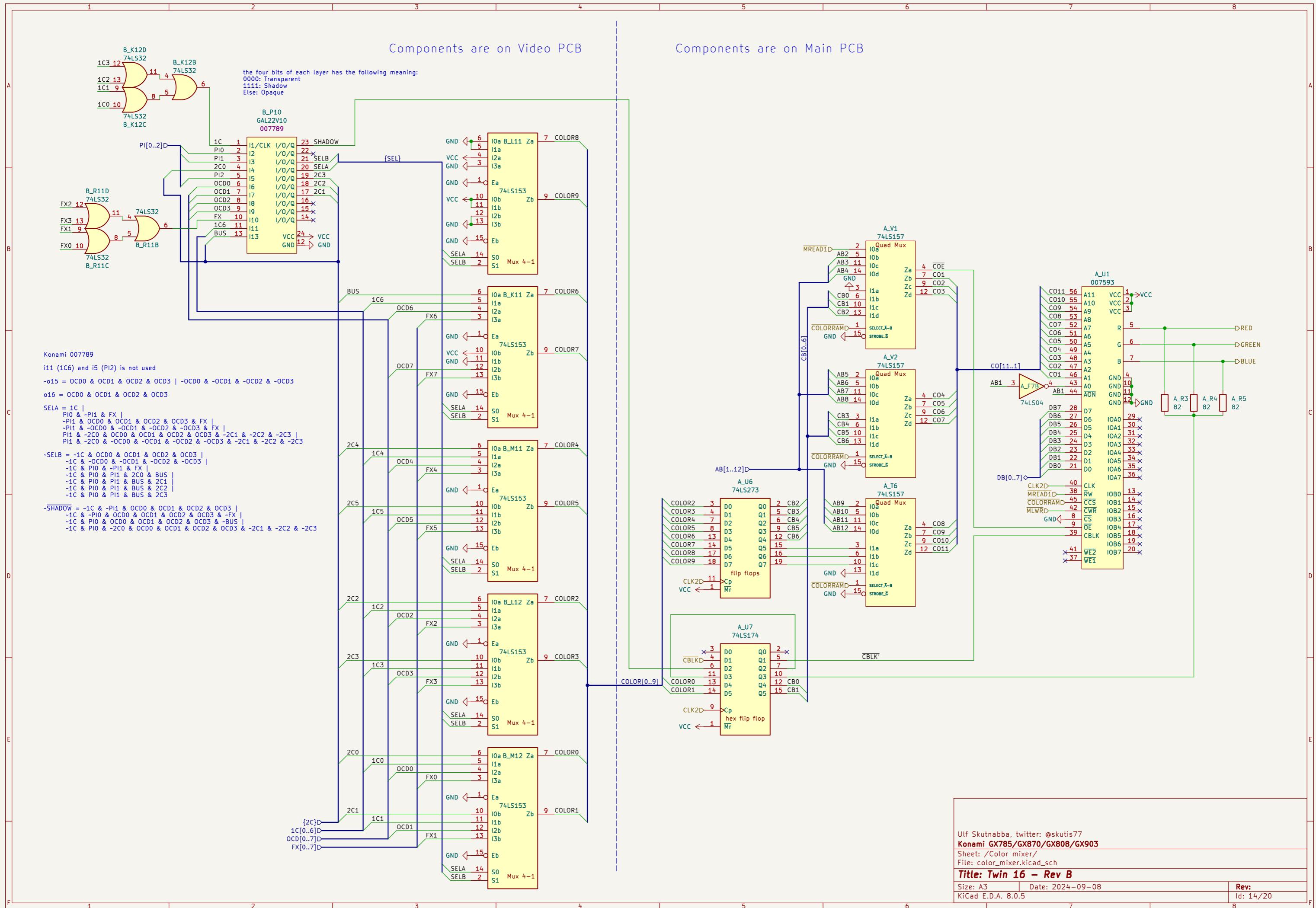
Graphics ROM and RAM

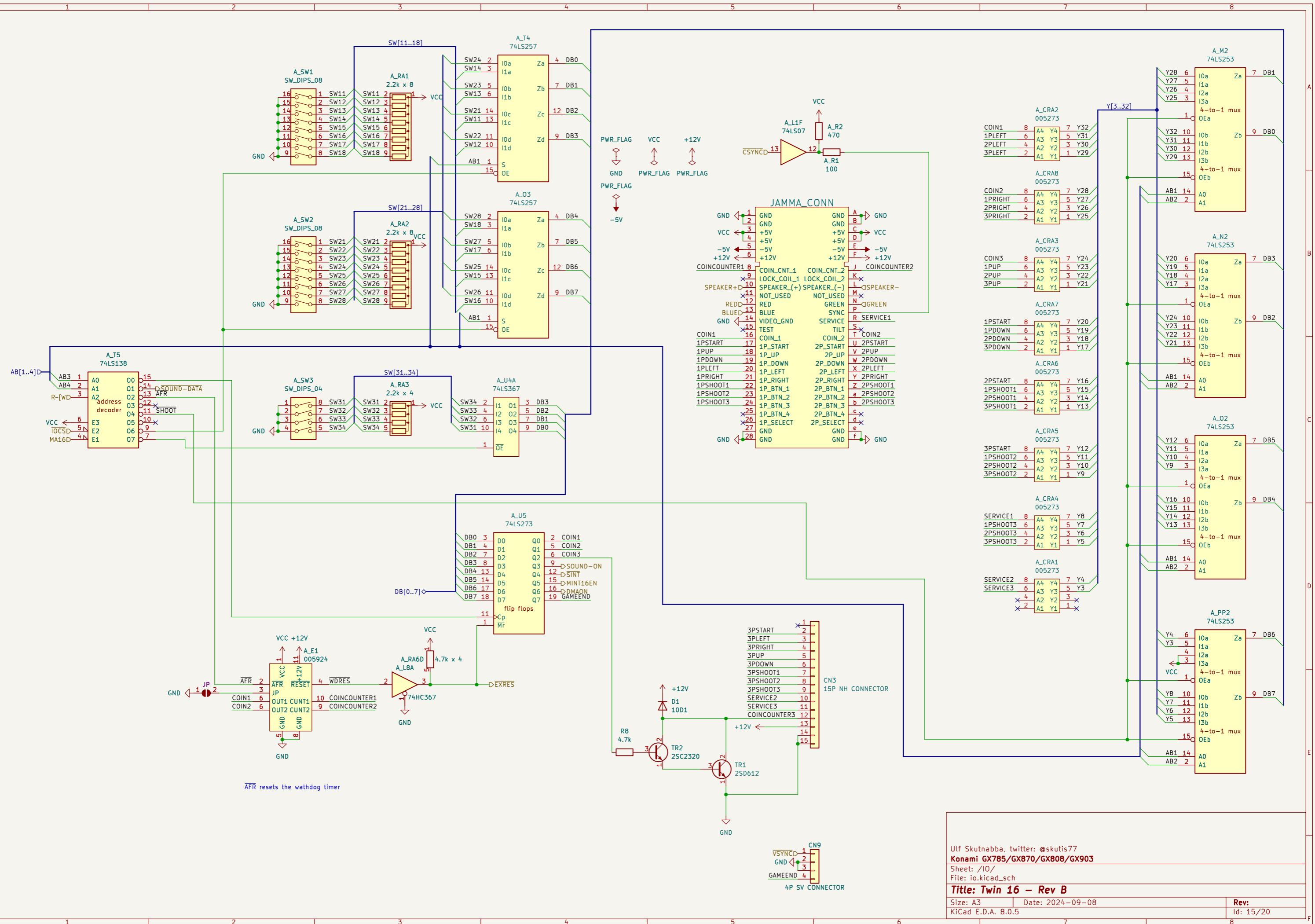


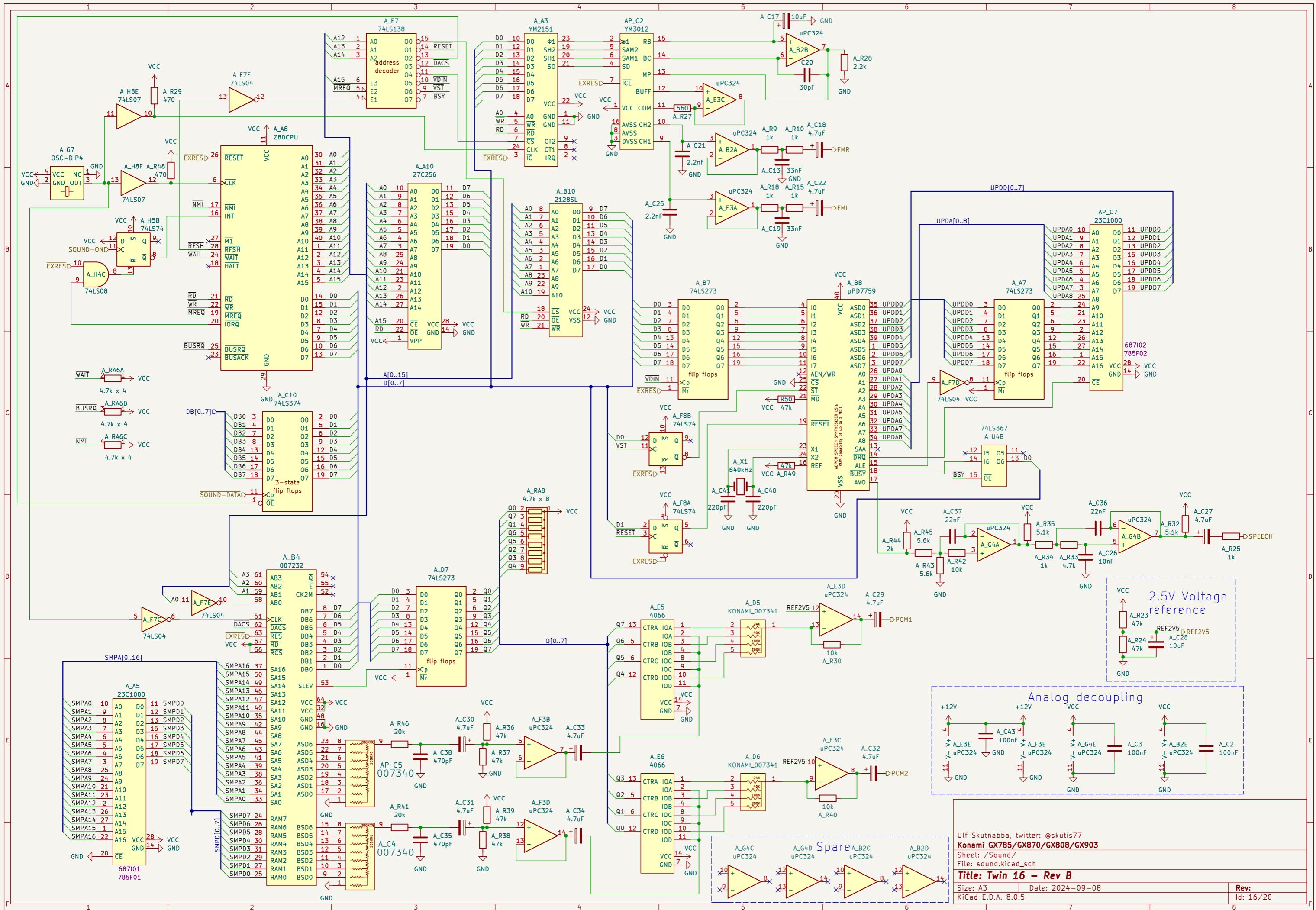




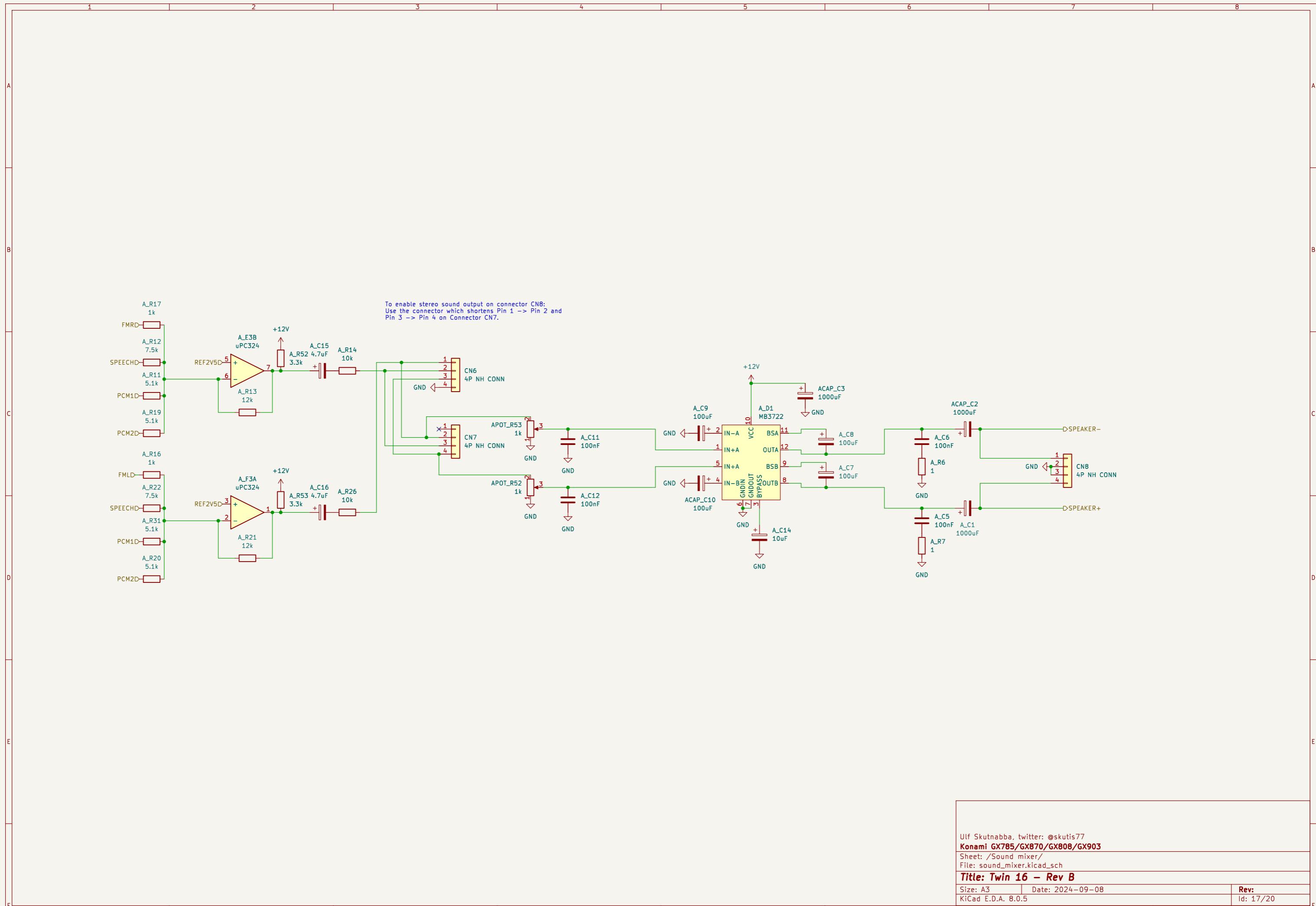








1 2 3 4 5 6 7 8



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Sheet: /Sound mixer/

File: sound_mixer.kicad_sch

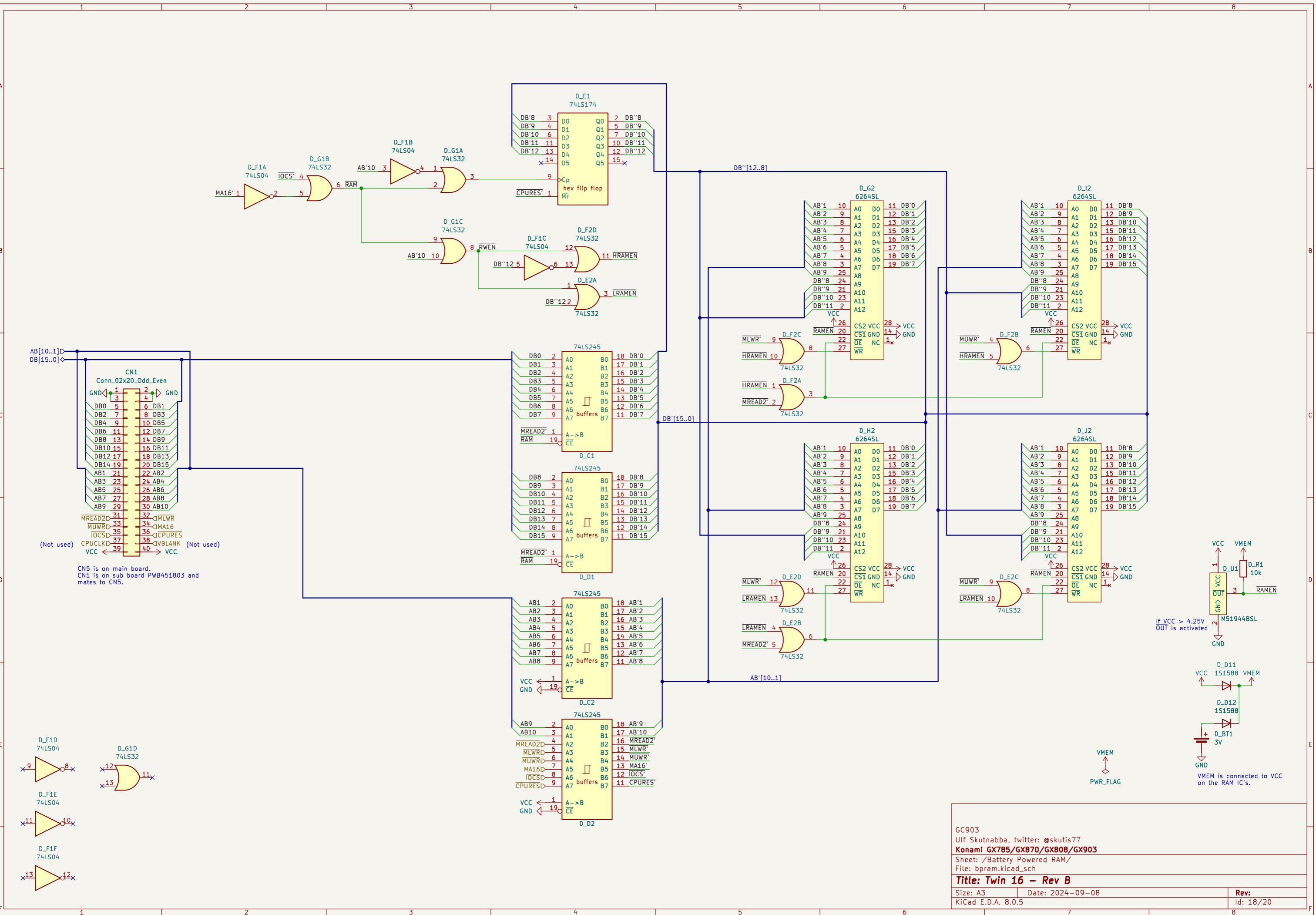
Title: Twin 16 – Rev B

Size: A3 Date: 2024-09-08

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Rev:

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GC903
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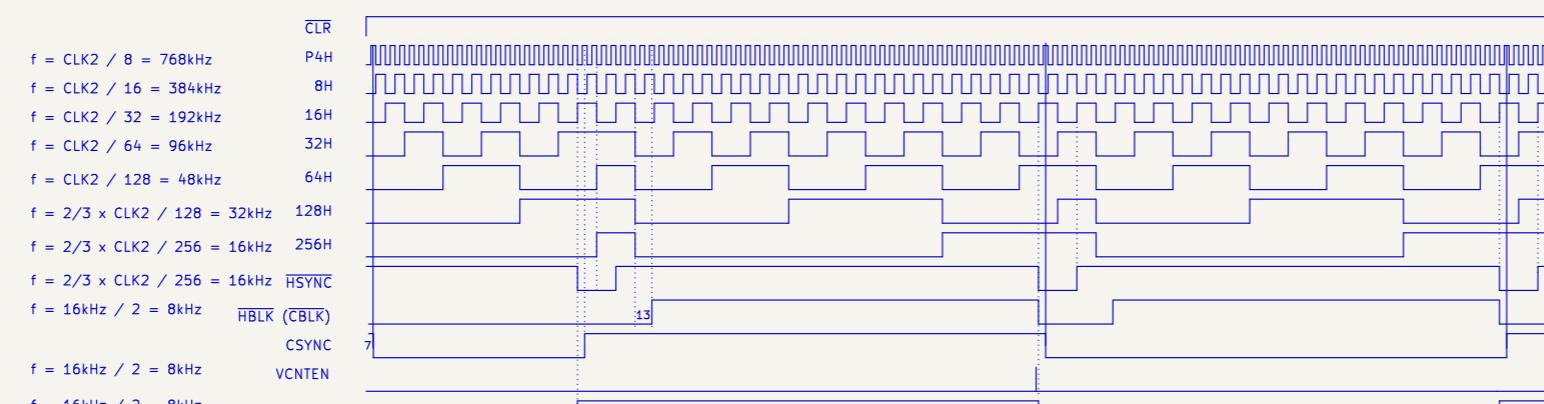
Sheet: /Battery Powered RAM/
File: bpram.kicad_sch

Title: Twin 16 – Rev B

Size: A3 Date: 2024-09-08
KiCad E.D.A. 8.0.5

Rev:
Id: 18/20

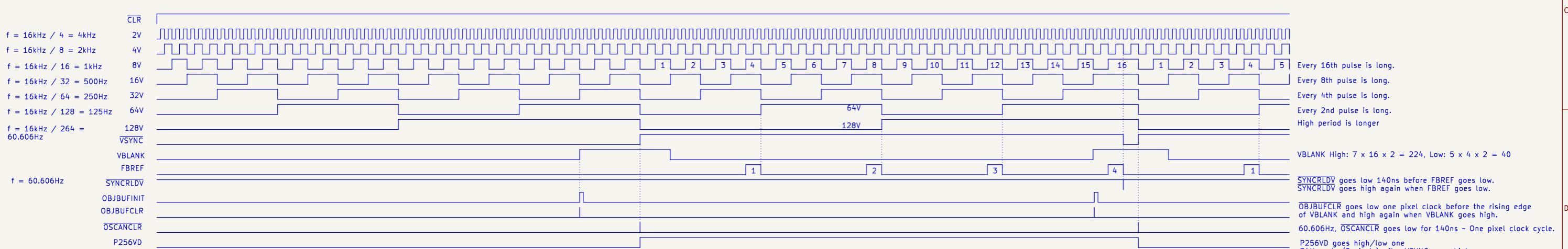
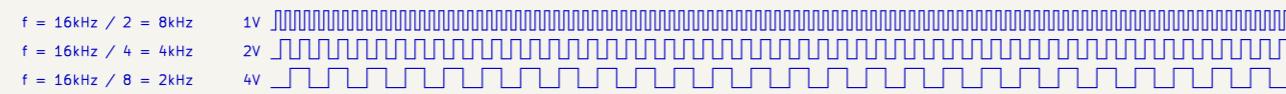
Horizontal signals



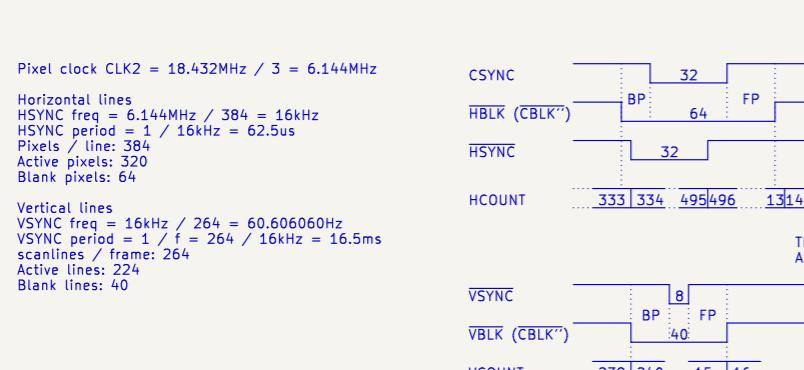
– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

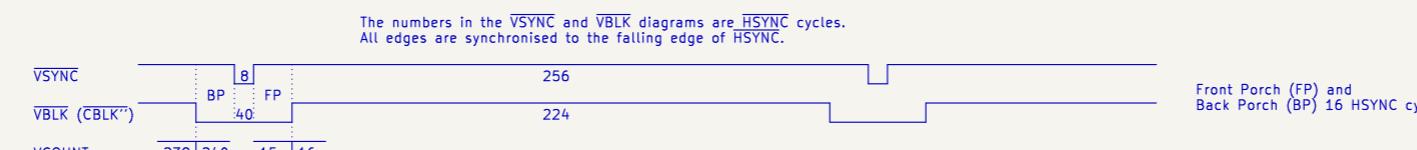
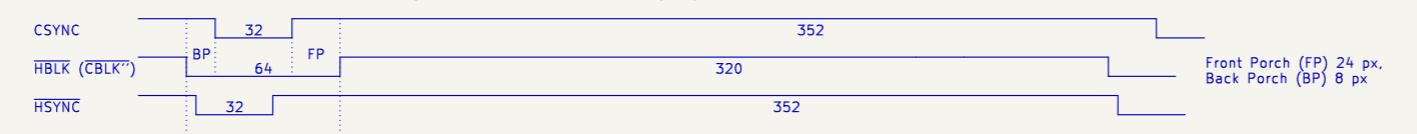
Vertical signals



Horizontal and vertical synch timing diagrams



The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.
All edges are synchronised to the rising edge of CLK2.



HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK'' is at the output of color mixer 007593.
CBLK' is shifted inside the 007593 one pixel clock.

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Sheet: /Timing diagrams/
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A

B

C

D

E

F

A

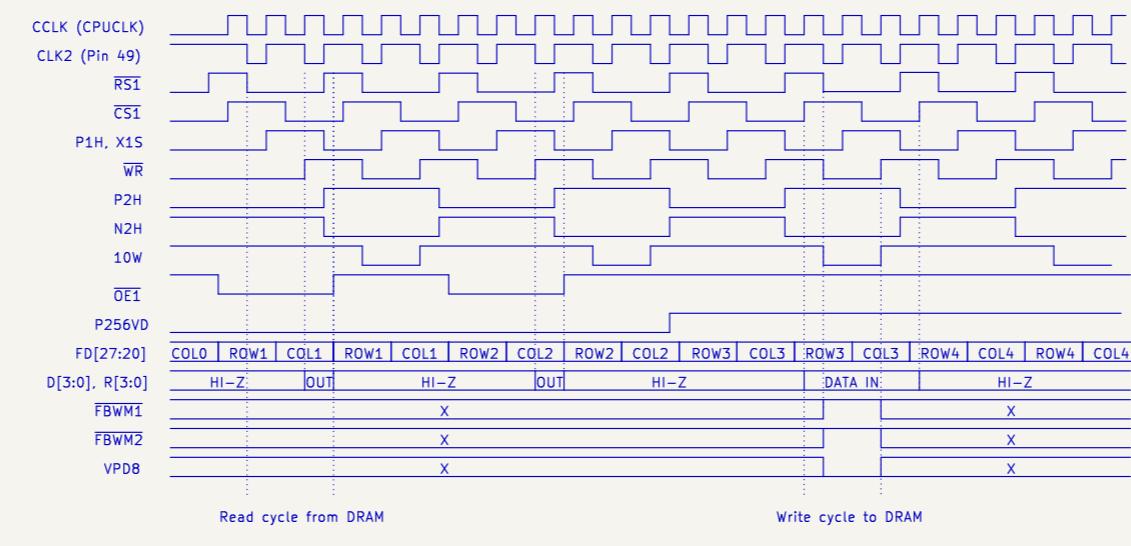
B

C

D

E

F



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Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

Size: A3 | Date: 2024-09-08
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Rev:
Id: 20/20