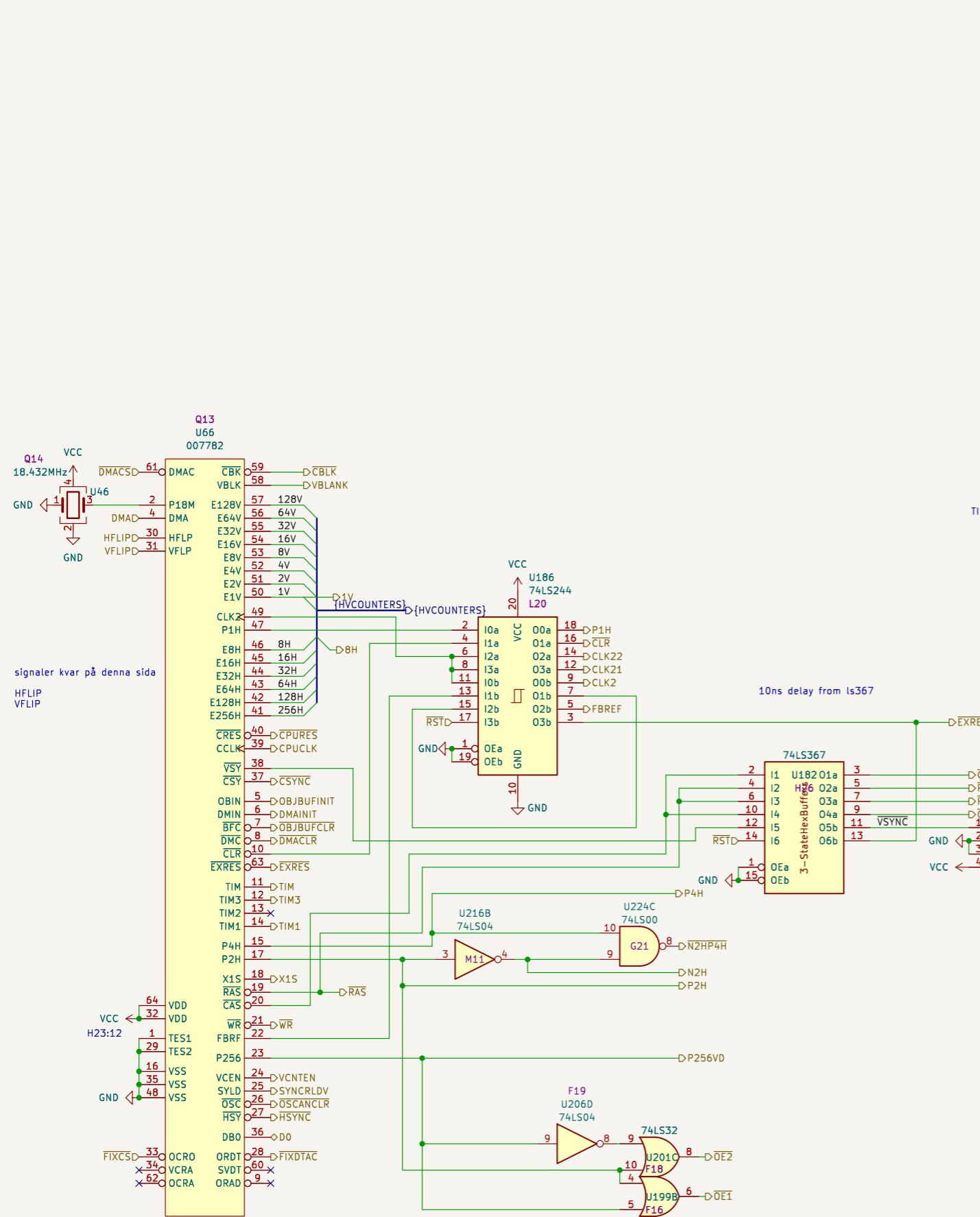
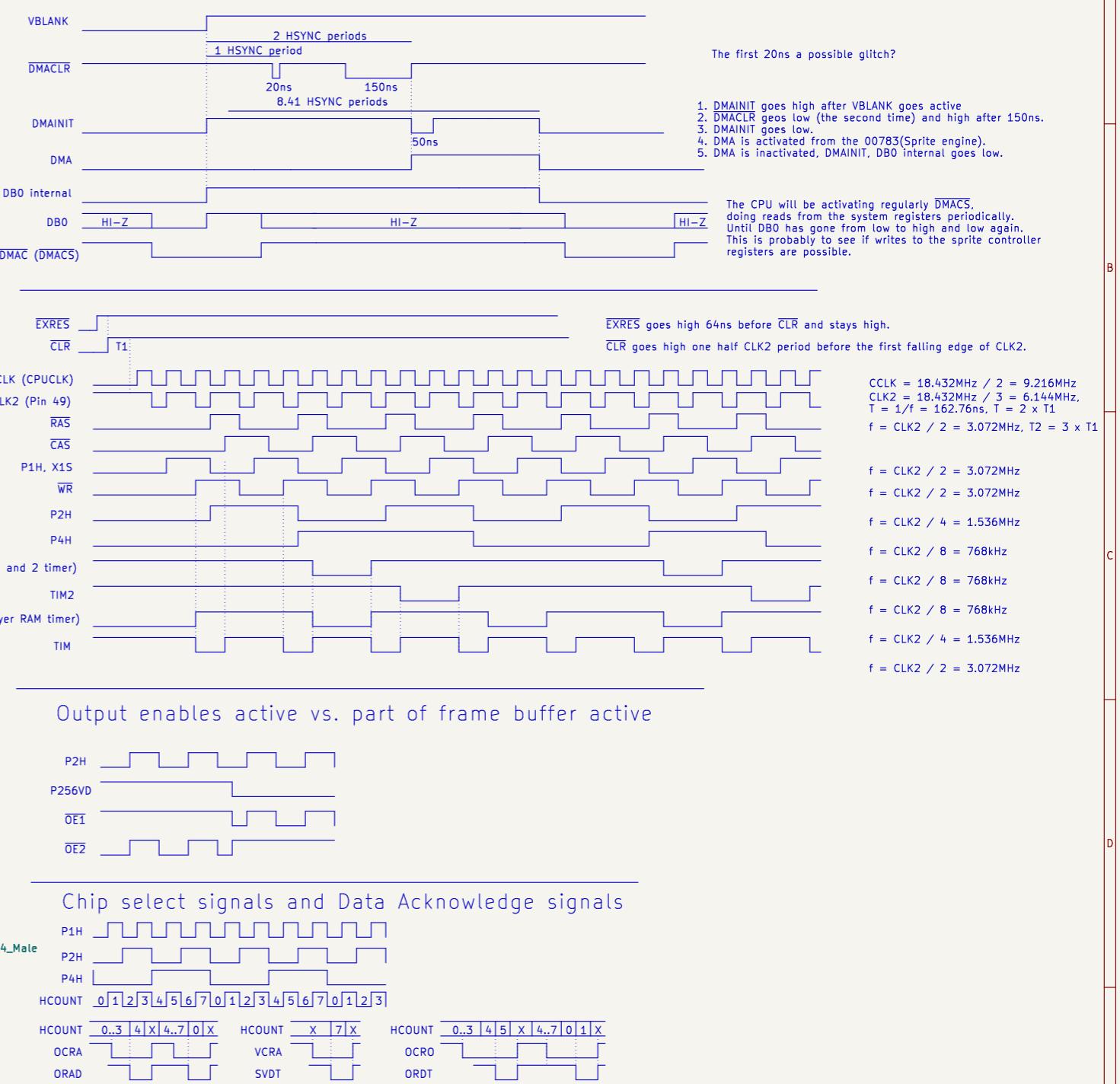


DMA Synchronization



Pins 30 and 31 were swapped on the schematics.



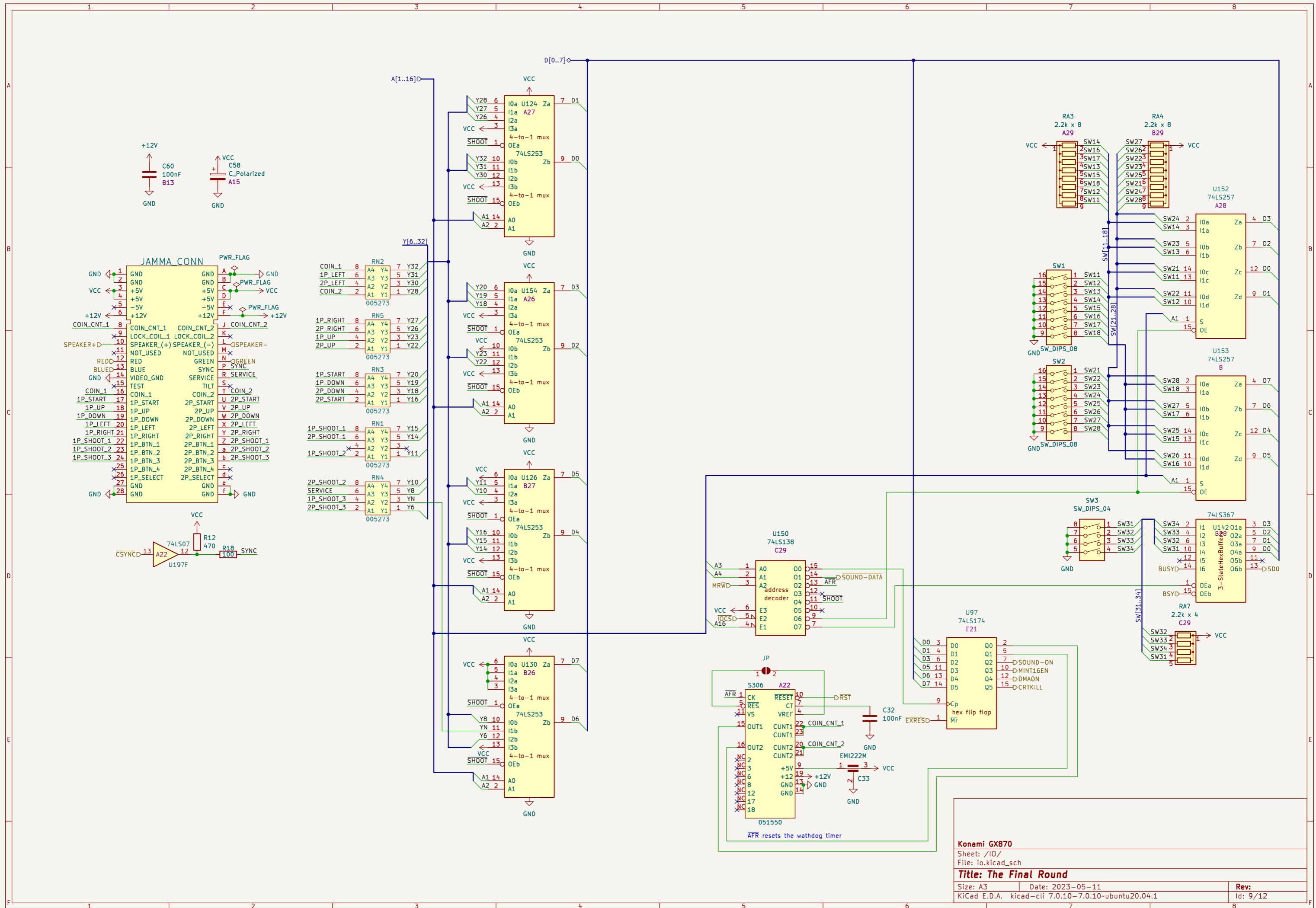
Timing
Konami GX870

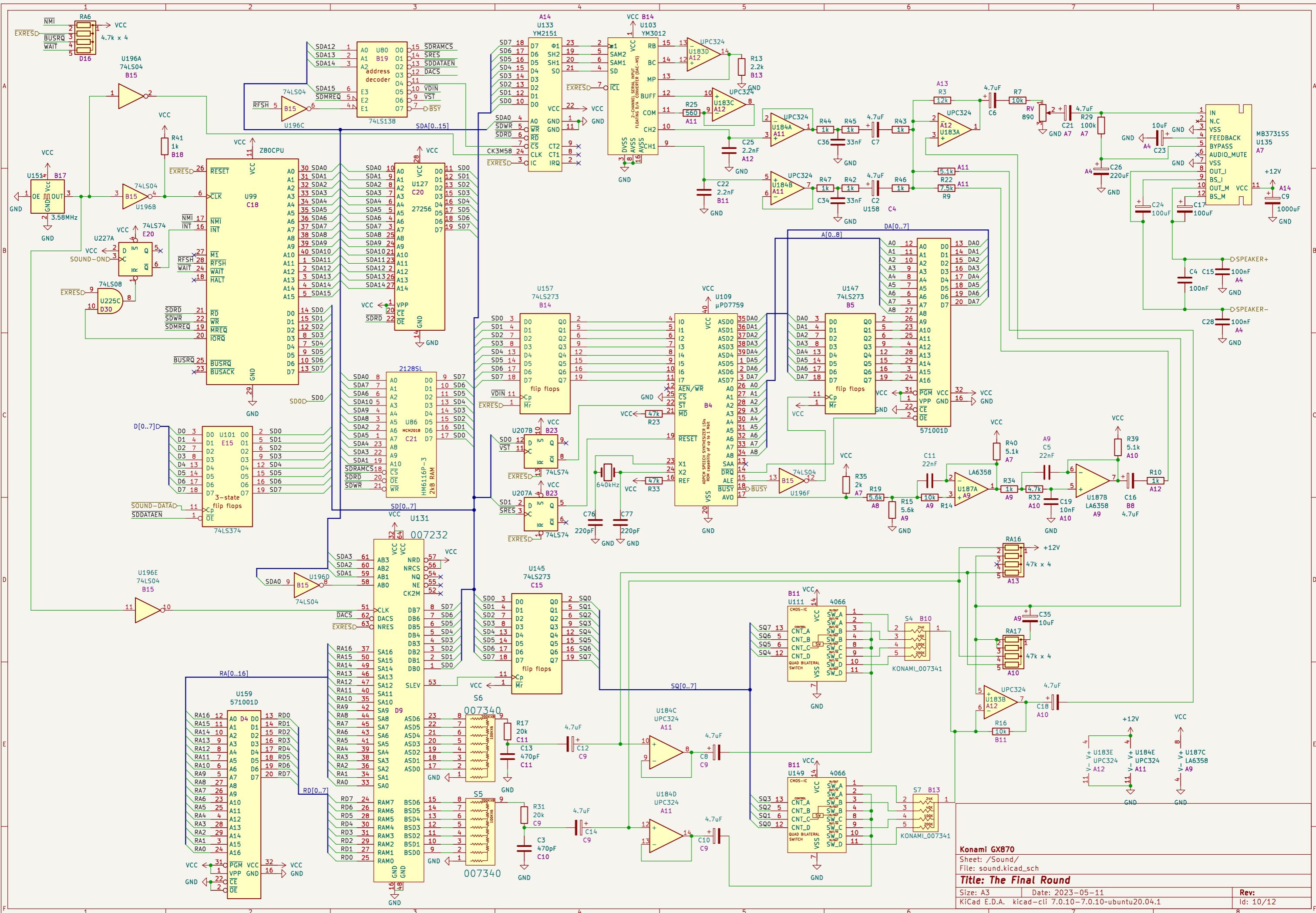
Title: The Final Round

Size: A3 Date: 2

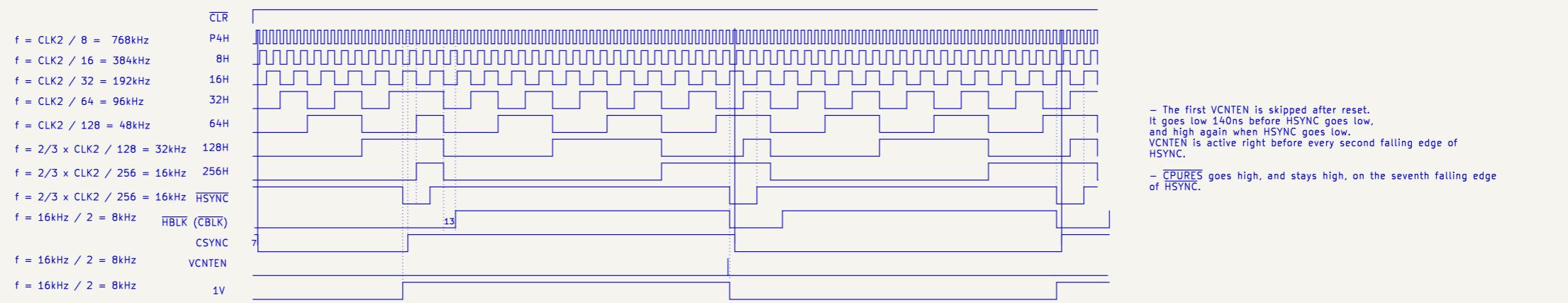
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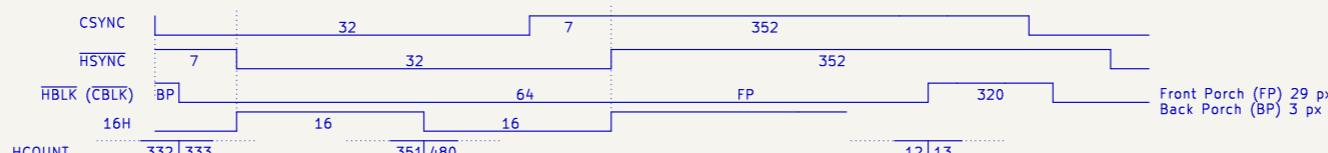
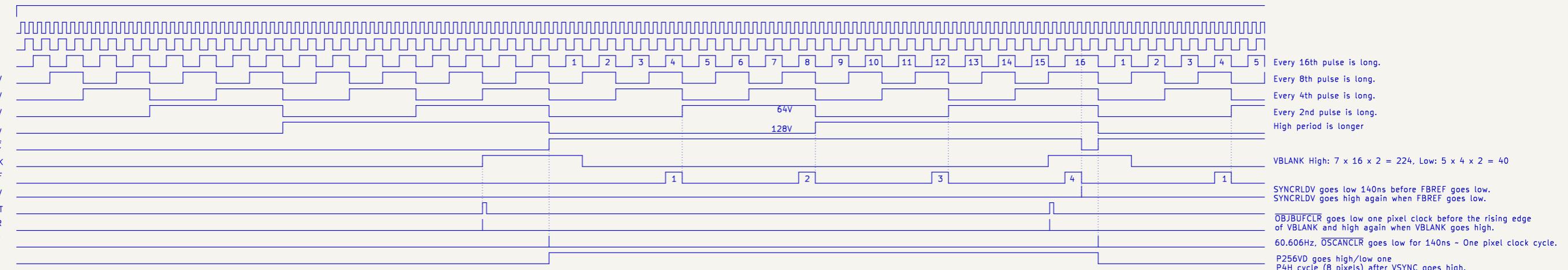
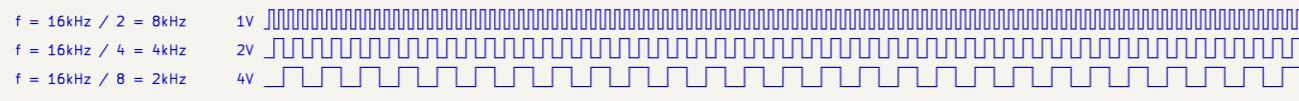
Horizontal signals



- The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

- CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



The horizontal blanking part is shown of the composite blanking signals.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]

HSYNC = $6.144\text{MHz} / 384 = 16\text{kHz}$

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Sheet: /Timing diagrams/
File: timing_diagrams.kicad_sch

Title: The Final Round

Size: A3	Date: 2023-05-11	Rev:
KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1	Id: 11/12	8

A

B

C

D

E

F

A

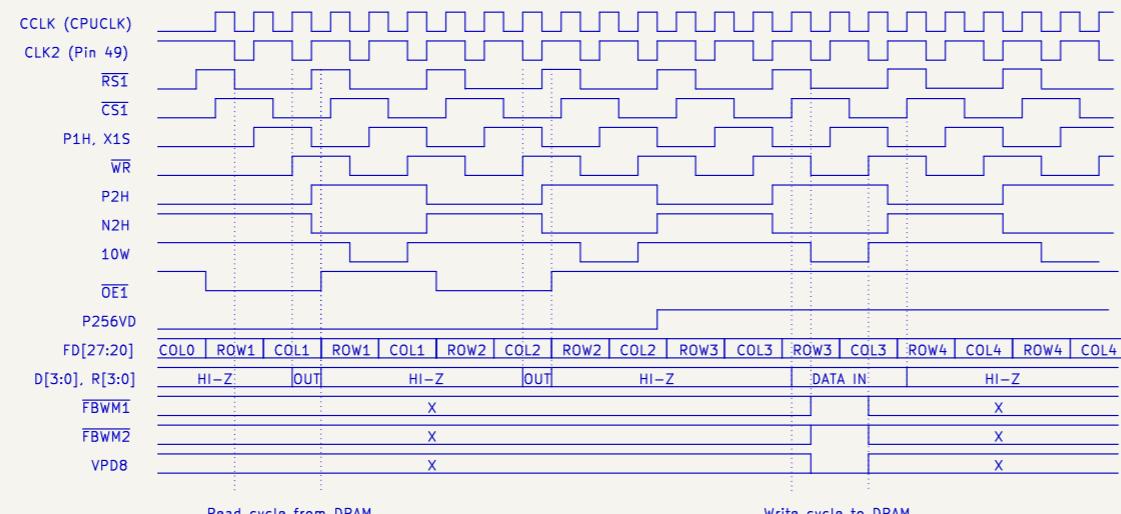
B

C

D

E

F

**Konami GX870**

Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: The Final Round

Size: A3	Date: 2023-05-11
KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1	Rev: Id: 12/12