

JOTEGI

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File: extermin.kicad_sch

Size: A3 Date: 29/08/2022

1 2 3 4 5 6 7 8

A

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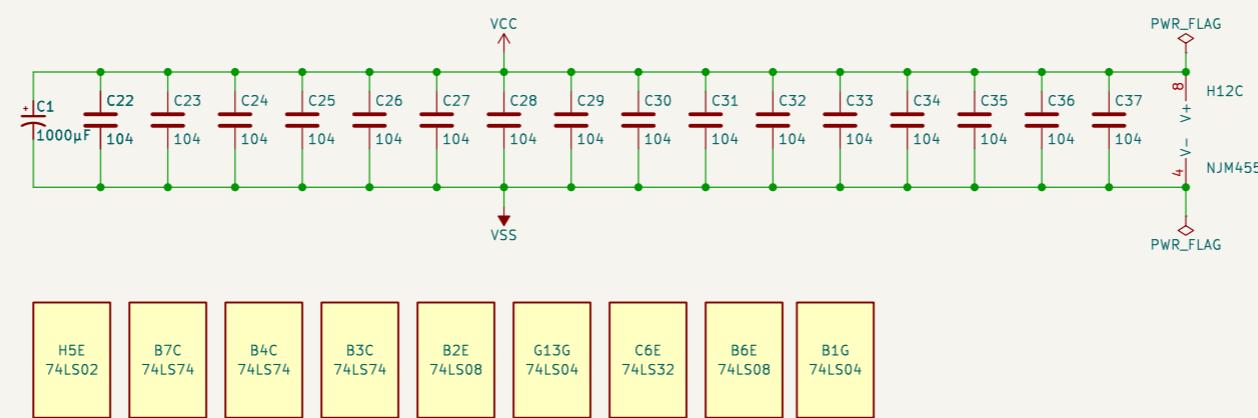
JOTEGO

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File: capacitors.kicad_sch

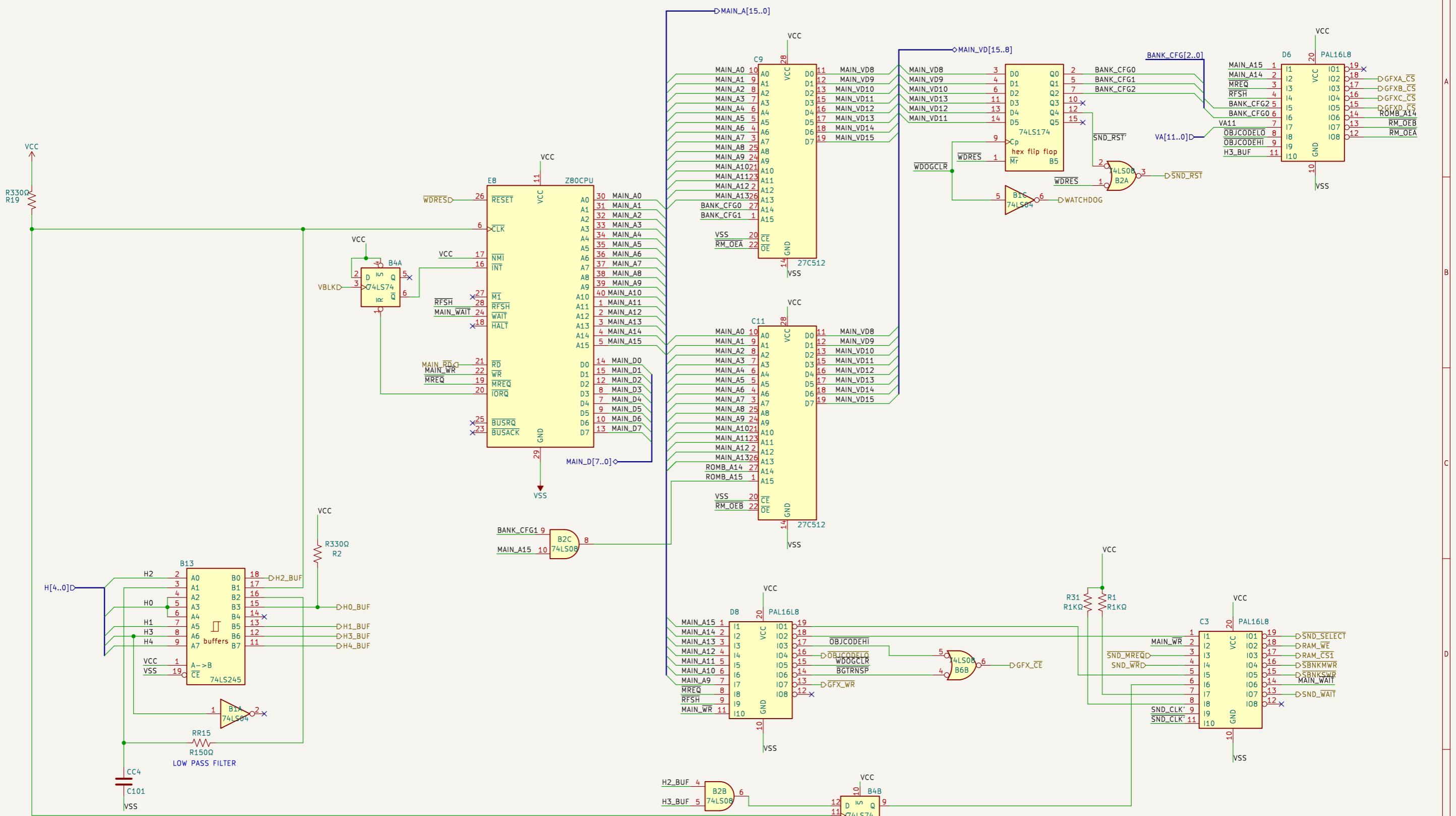
Title: EXTERMINATION

Size: A3 | Date: 29/08/2022
KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1

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1 2 3 4 5 6 7 8



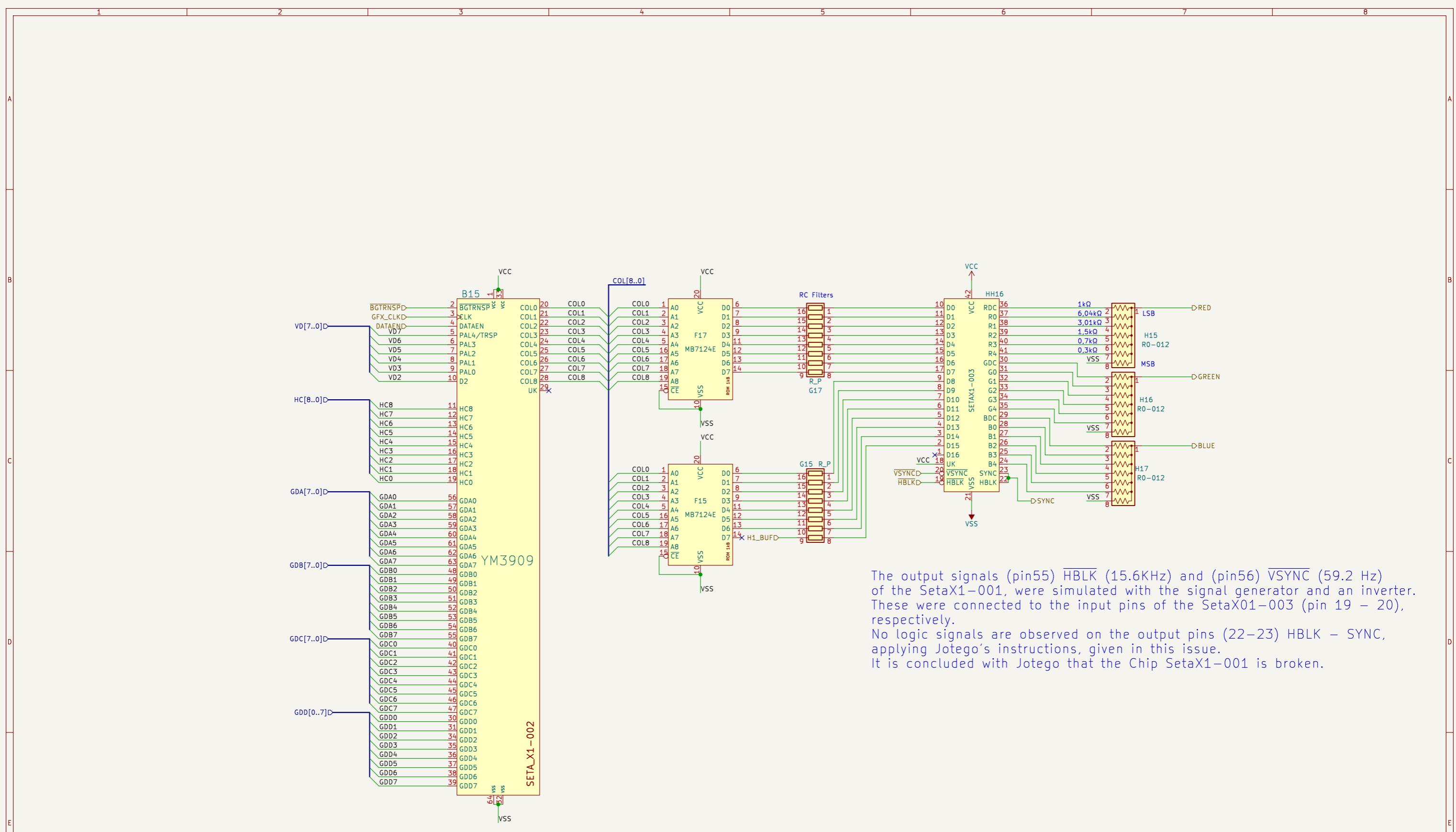
JOTEGO

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Title: EXTERMINATION

Size: A3	Date: 29/08/2022	Rev: José Tejada G.
KiCad E.D.A. kicad-cliv 7.0.10-7.0.10-ubuntu20.04.1		Id: 3/10





The output signals (pin 55) **HBLK** (15.6KHz) and (pin 56) **VSYNC** (59.2 Hz) of the **Setax1-001**, were simulated with the signal generator and an inverter. These were connected to the input pins of the **Setax01-003** (pin 19 – 20), respectively. No logic signals are observed on the output pins (22–23) **HBLK** – **SYNC**, applying Jotego's instructions, given in this issue. It is concluded with Jotego that the Chip **Setax1-001** is broken.

JOTEGO

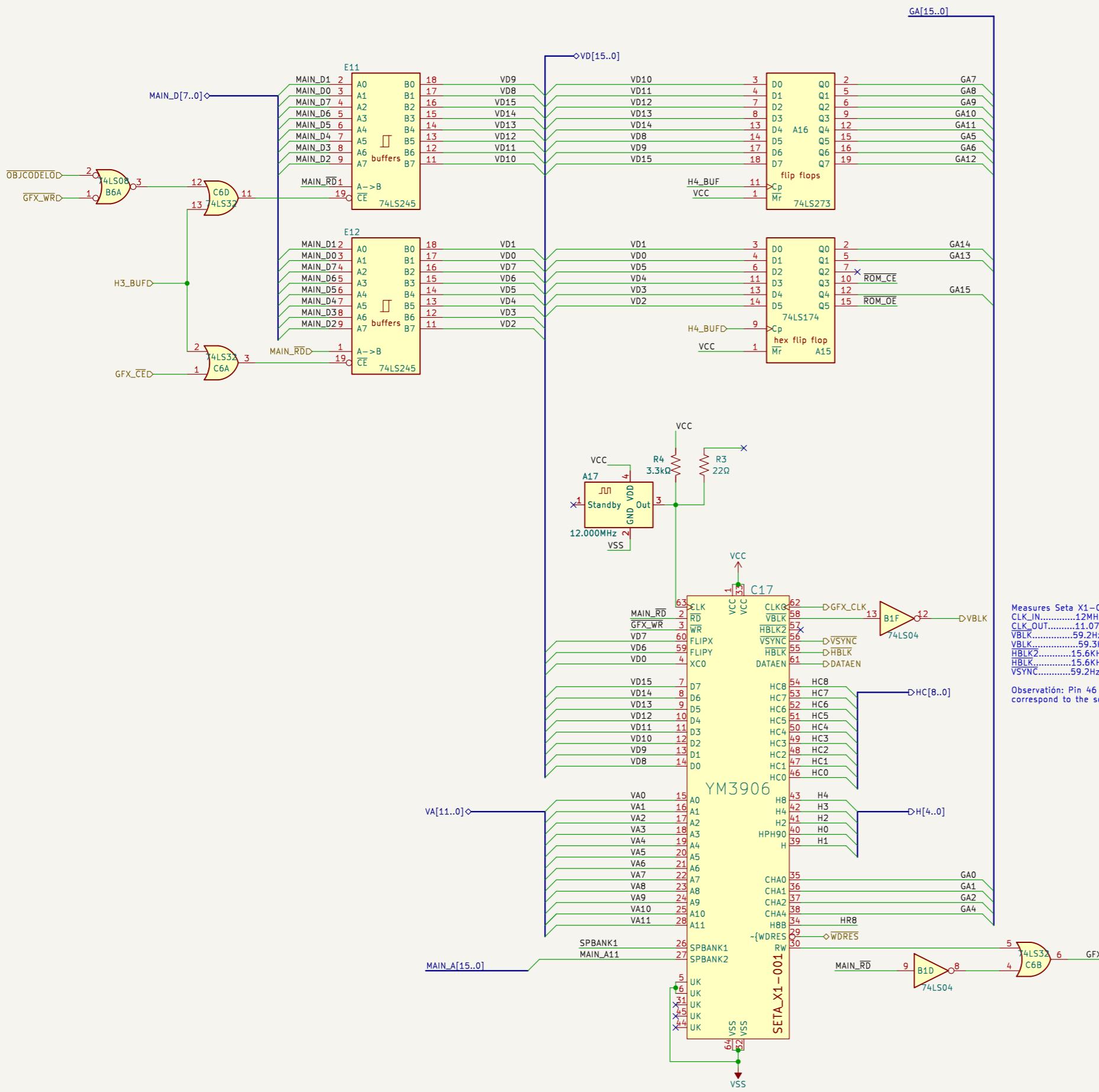
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Size: A3 | Date: 29/08/2022
KiCad E.D.A. kicad-cl 7.0.10-7.0.10-ubuntu20.04.1



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JOTEGO

Sheet: /gfx/
File: gfx.kicad_sch

Title: EXTERMINATION

Size: A3 Date: 29/08/2022
KiCad E.D.A. kicad-cli 7.0.10-7.0.10~ubuntu20.04.1



1 2 3 4 5 6 7 8

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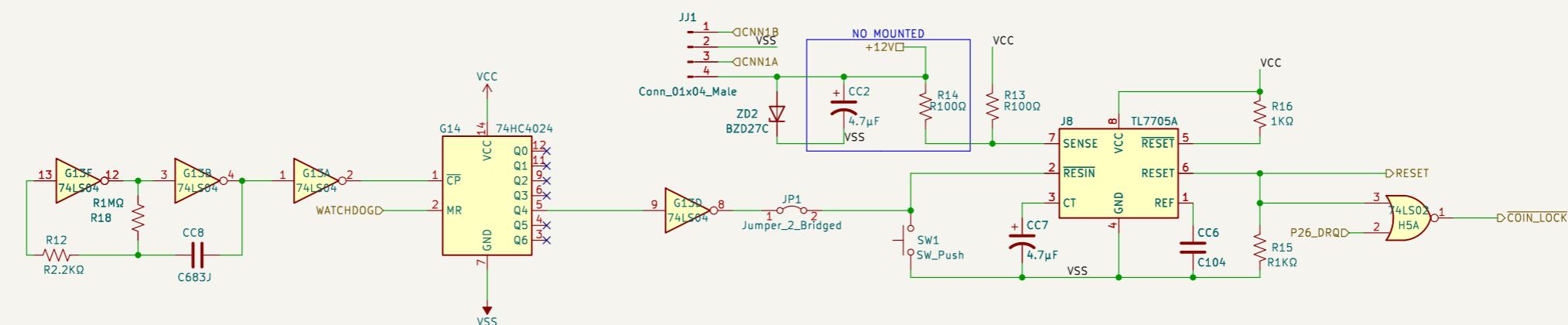
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JOTEGO

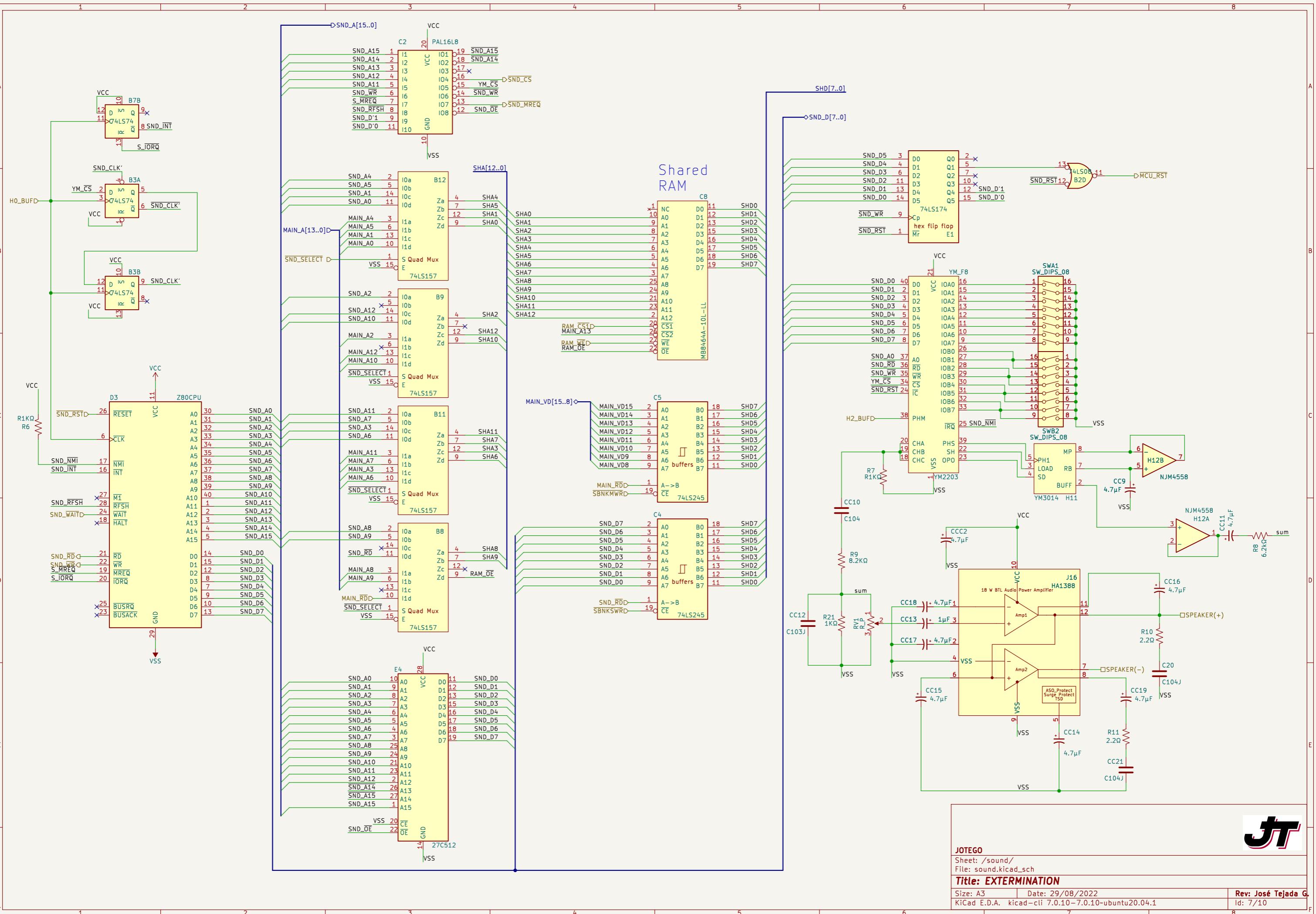
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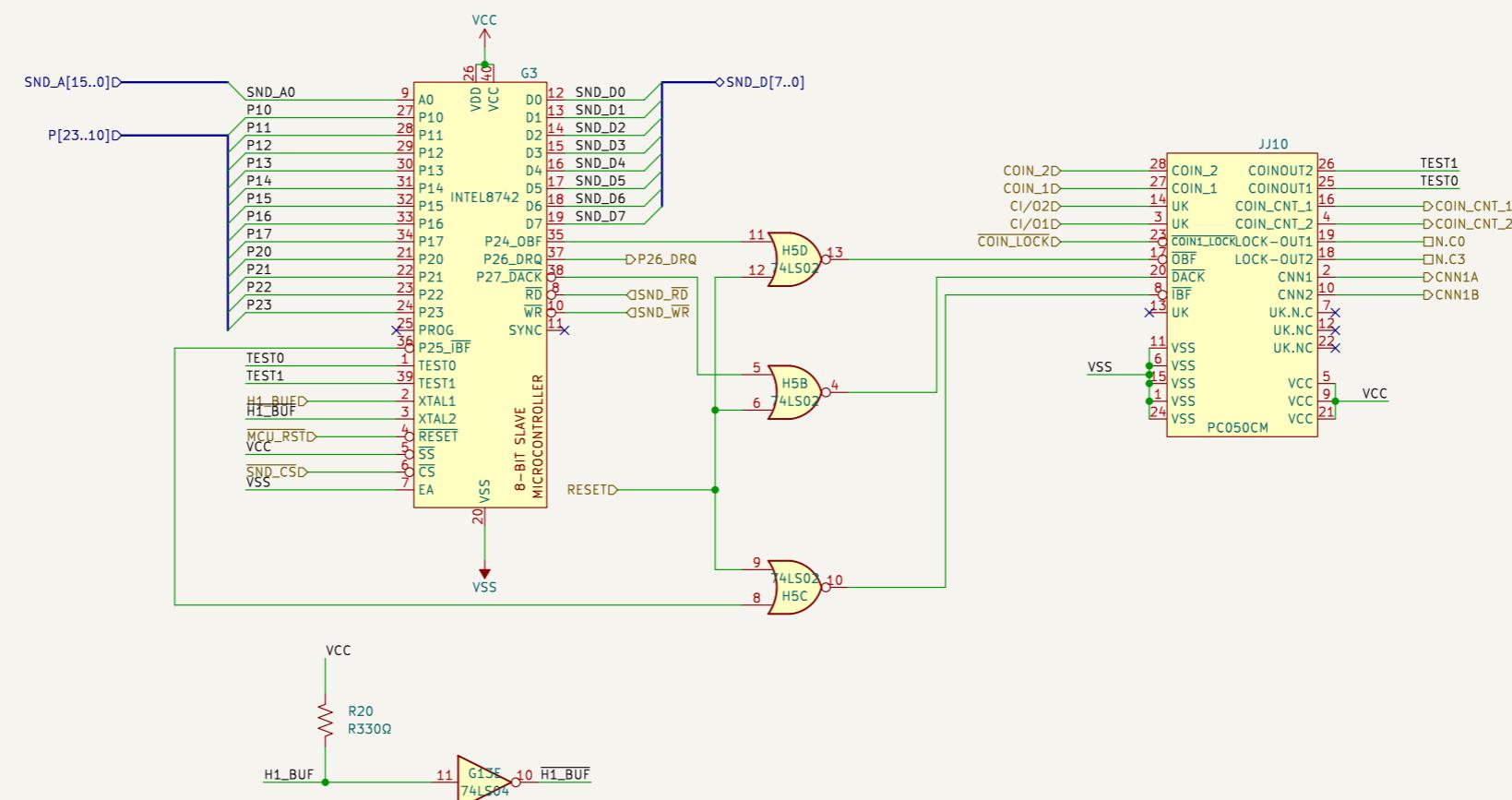
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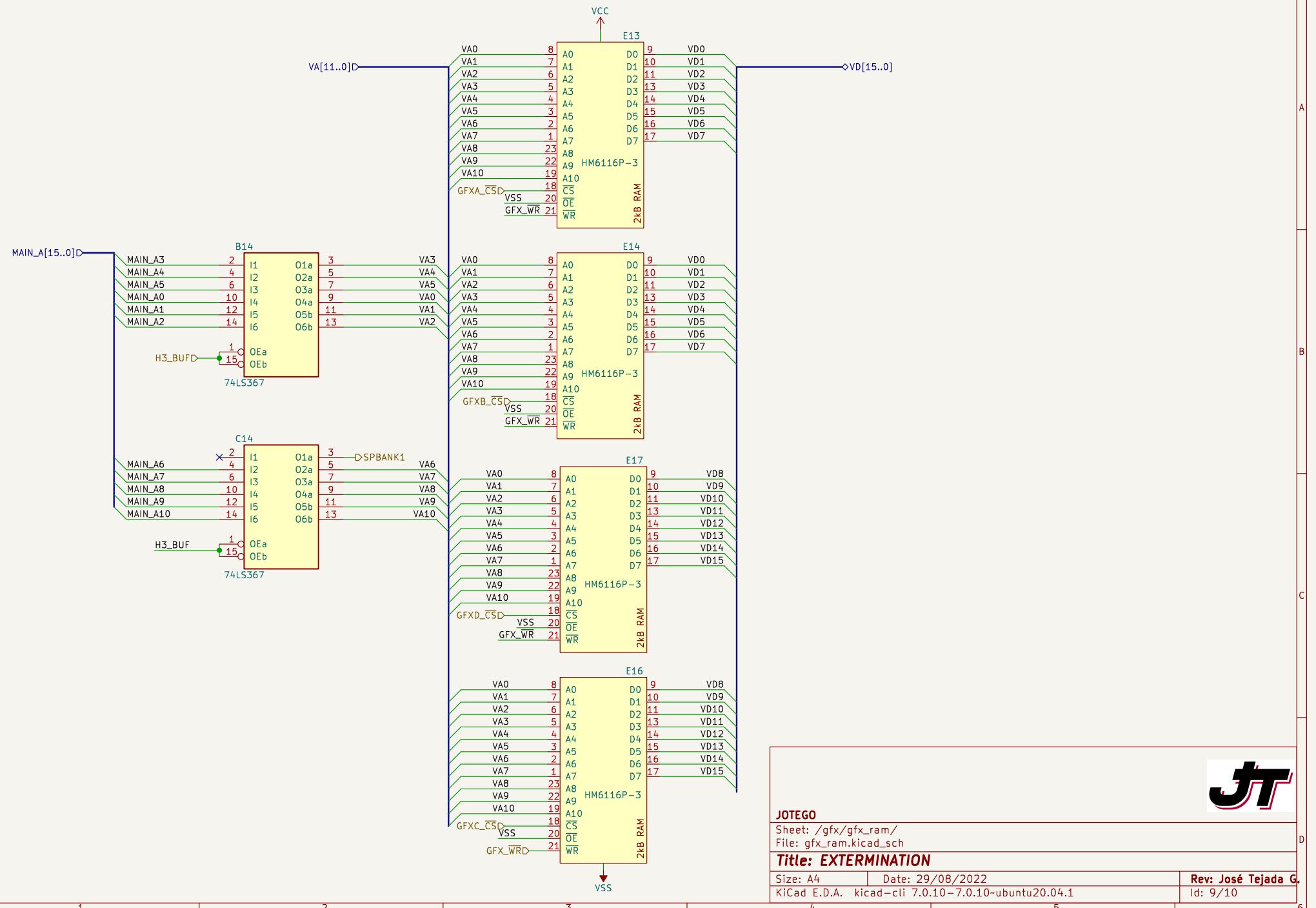
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KiCad E.D.A. kicad-cli 7.0.10-7.0.10-ubuntu20.04.1

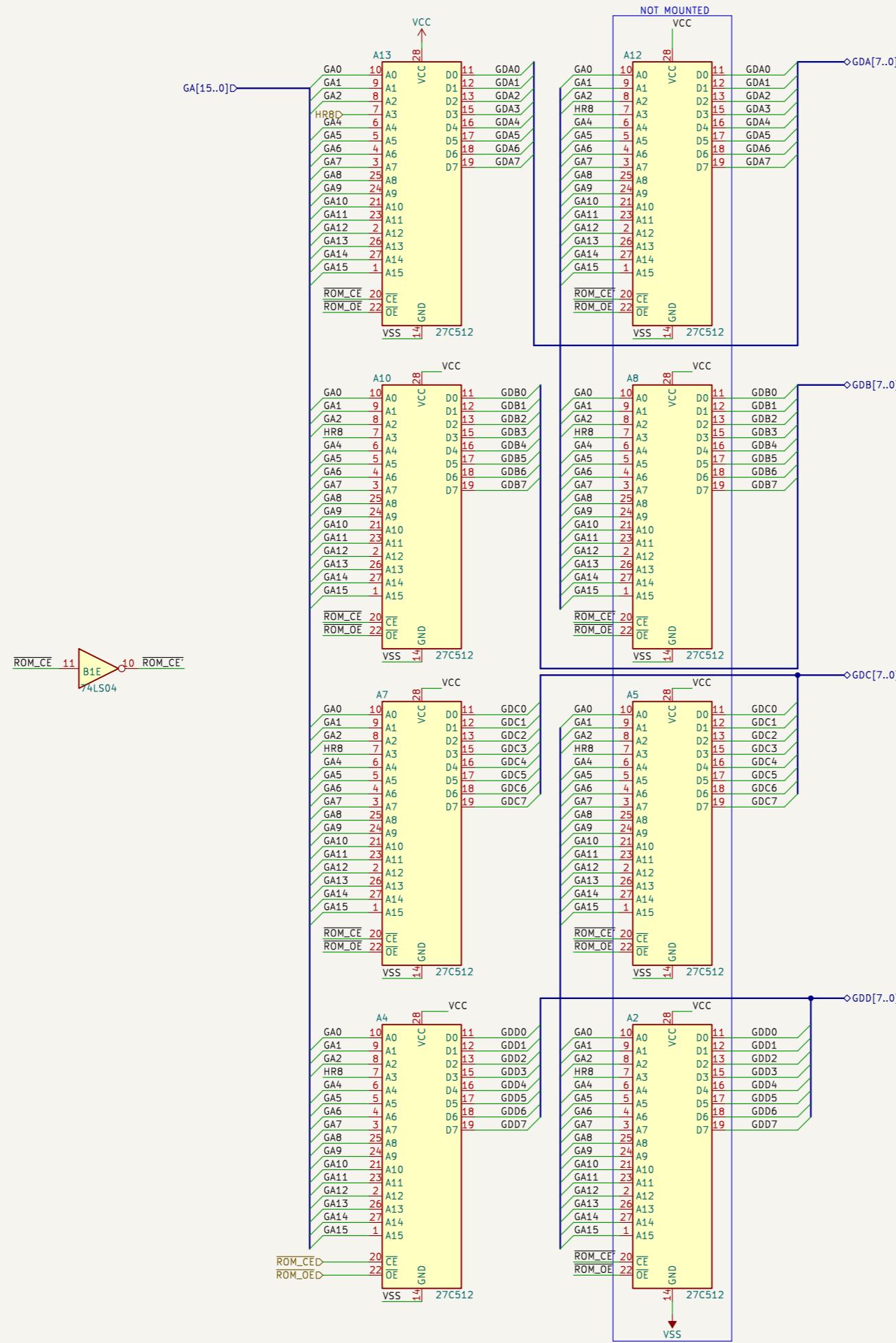


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Sheet: /gfx/gfx_rom/
File: gfx_rom.kicad_sch

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Size: A3 Date: 29/08/2022 Rev: José Tejada G.
 KiCad E.D.A. kicad-clt 7.0.10-7.0.10-ubuntu20.04.1 Id: 10/10