

Address mapping for memory select signals

Output	Start	End
MSEL0	\$0000	\$7FFF
MSEL1A/B	\$8000	\$BFFF
MSEL2	\$C000	\$C7FF
MSEL3	\$C800	\$CFFF
MSEL4	\$D000	\$DFFF
MSEL5	\$E000	\$FFFF

The Schematics have been analyzed from
a die picture by Furrtek.
The chip is identified as:

624108U
AAAA 2C32
FUJITSU
C 1987

It is a C-530UHB , MB624108 device
from the UHB-CMOS series.
- 840 Basic Cells
- 12 Columns, 74 Rows (70 of them are usable)

LSB is input B.

Ulf Skutnabba, twitter: @skutis77

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Title: **Capcom DL-020F-108U**

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