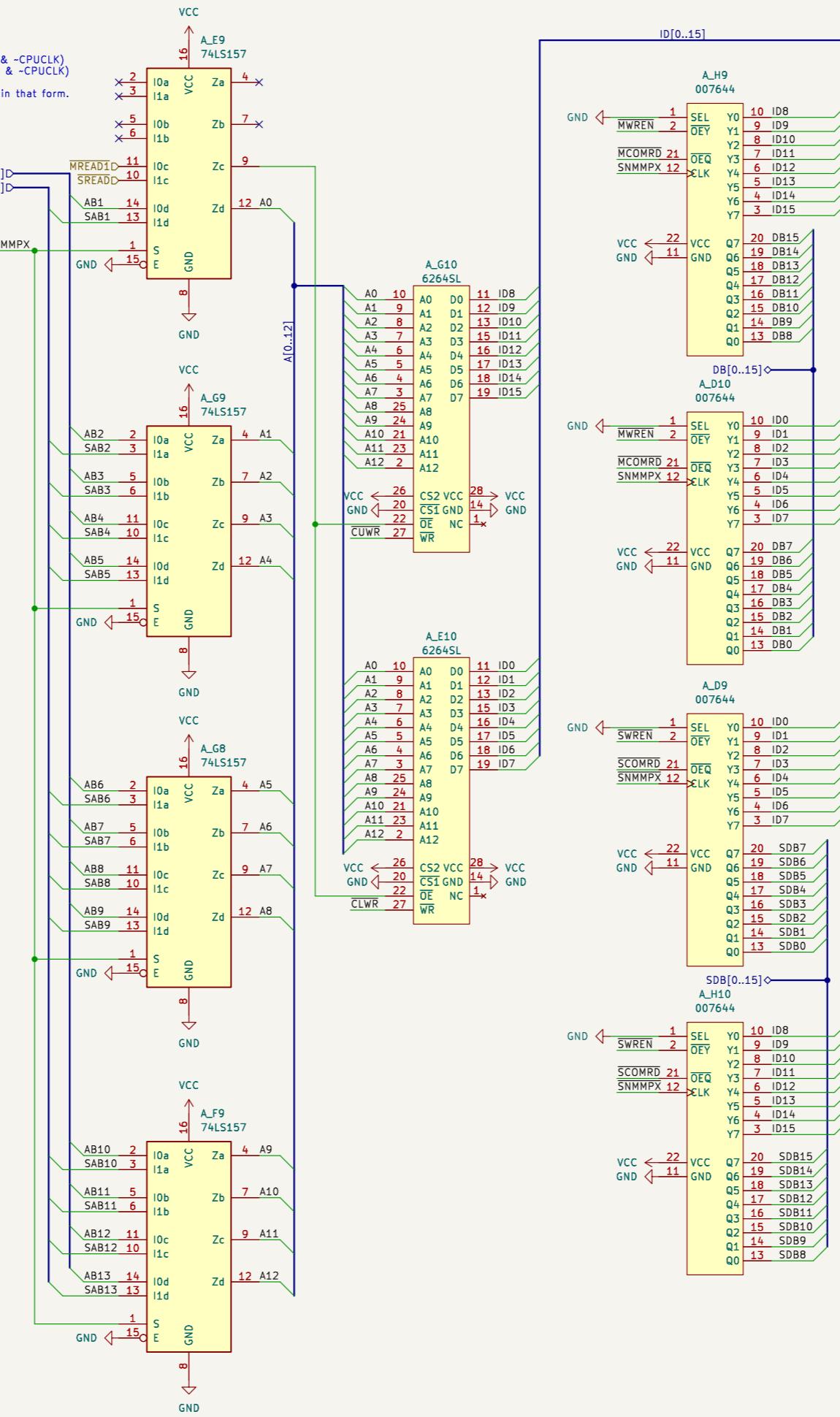
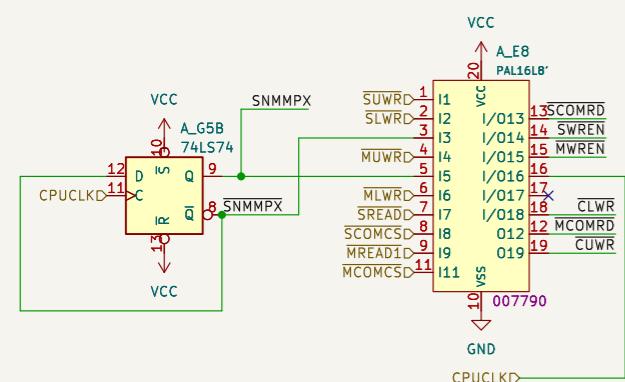


Konami 007790

$MCOMRD = \neg(MREAD1 \& \neg MCOMCS) = MREAD1 \mid MCOMCS$
 $SCOMRD = \neg(SREAD \& \neg SCOMCS)$
 $SWREN = \neg(SNMMPX \& SREAD \& \neg SCOMCS)$
 $MWREN = \neg(SNMMPX \& MREAD1 \& \neg MCOMCS)$
 $CLWR = \neg(CLWR \& \neg SNMMPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg SNMMPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$
 $CUWR = \neg(CUWR \& \neg SNMMPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg MUWR \& \neg SNMMPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$

A All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16L8 device it is kept in that form. The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



This is from jammarcade.net

Pin 1 = SEL – changes whether the Q outputs require a rising edge clock or not.
Pin 2 = OEQ – Output enable for the Y outputs else they are inputs. Active LOW
Pin 21 = OEQ – Output enable for the Q (clocked) outputs else they are inputs. Active LOW
Pin 12 = CLK – Clock input
Pins 3–10 = Y outputs – normal outputs. If OEQ is LOW these pins become outputs
mirroring the state of the Q input pins. SEL and CLK pins are not used in this mode.
Pins 13–20 = Q outputs – clocked outputs. If OEQ is LOW these pins become outputs.
If SEL is HIGH and CLK is HIGH these outputs will mirror the state of the Y inputs.
If SEL is LOW then the outputs will only change state on a rising edge CLK.

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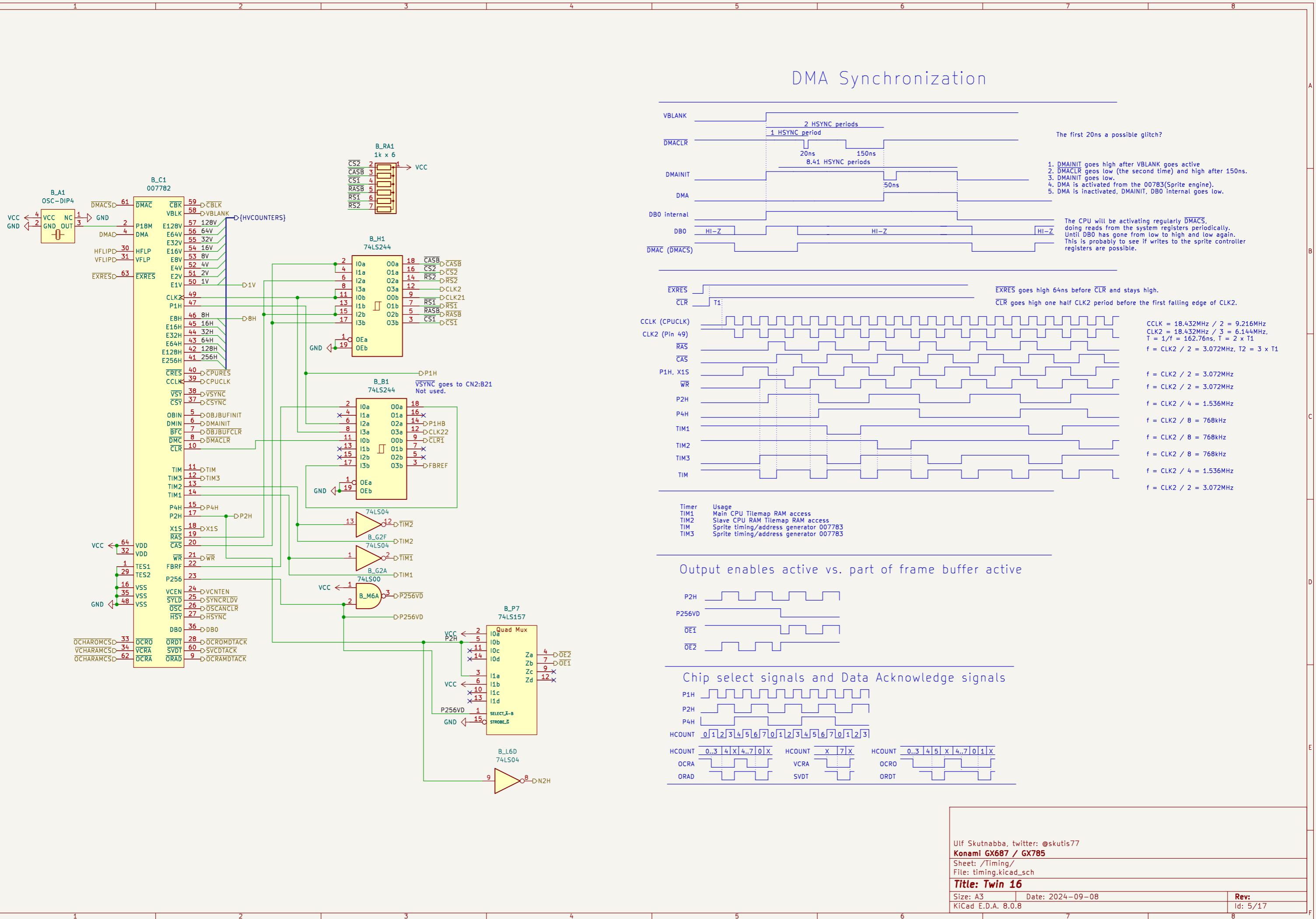
Konami GX687 / GX785

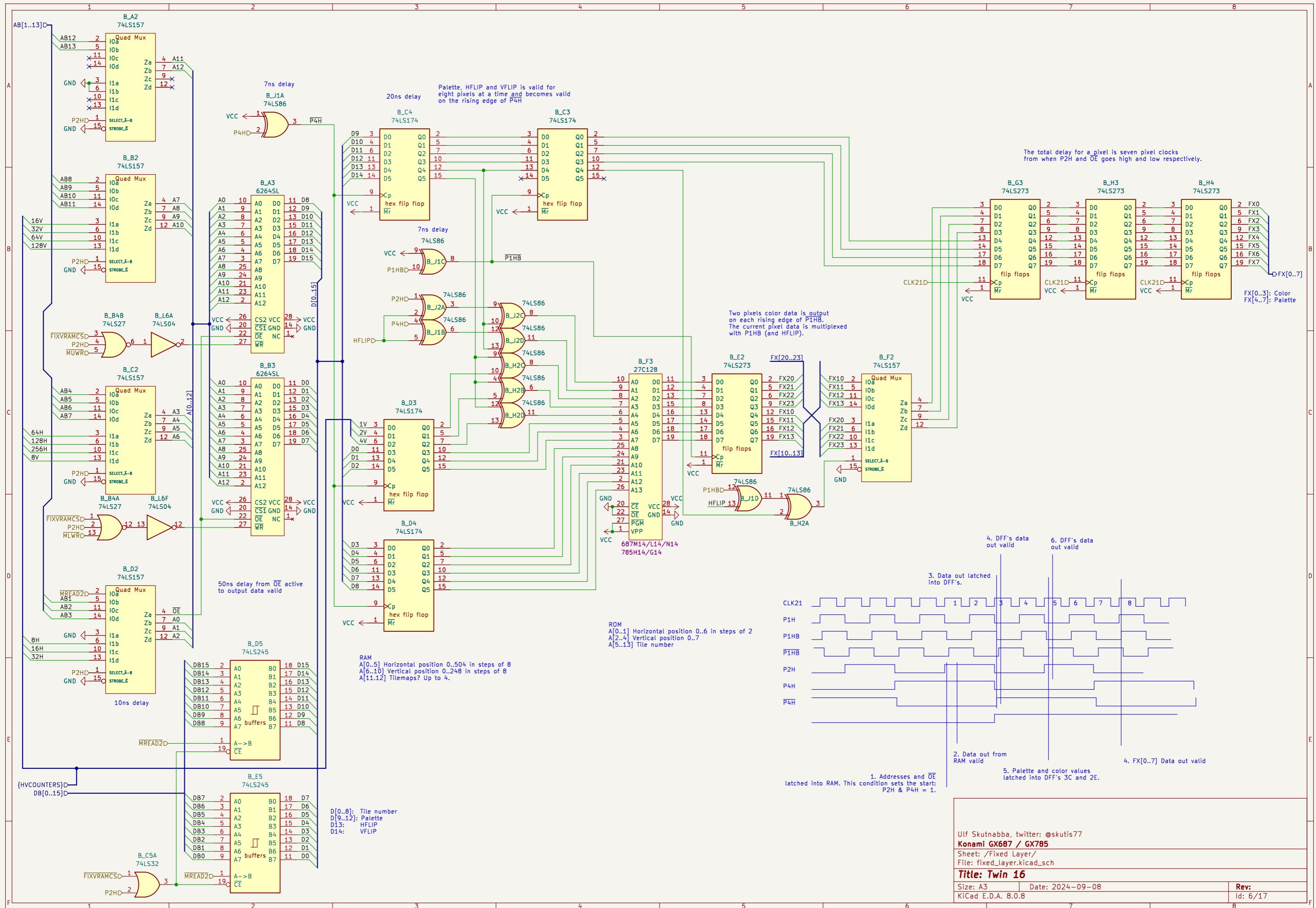
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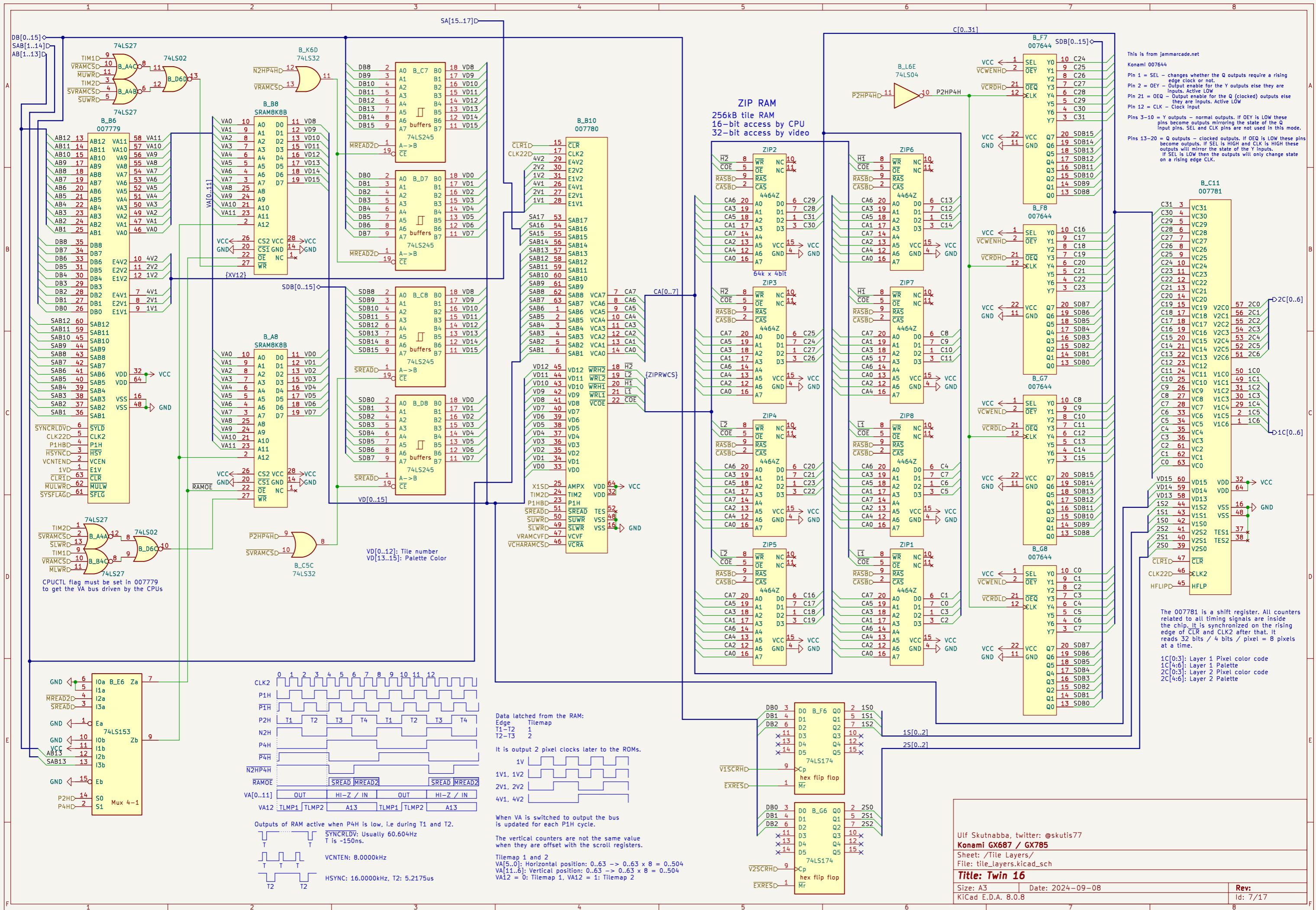
Konami GX687 / GX785

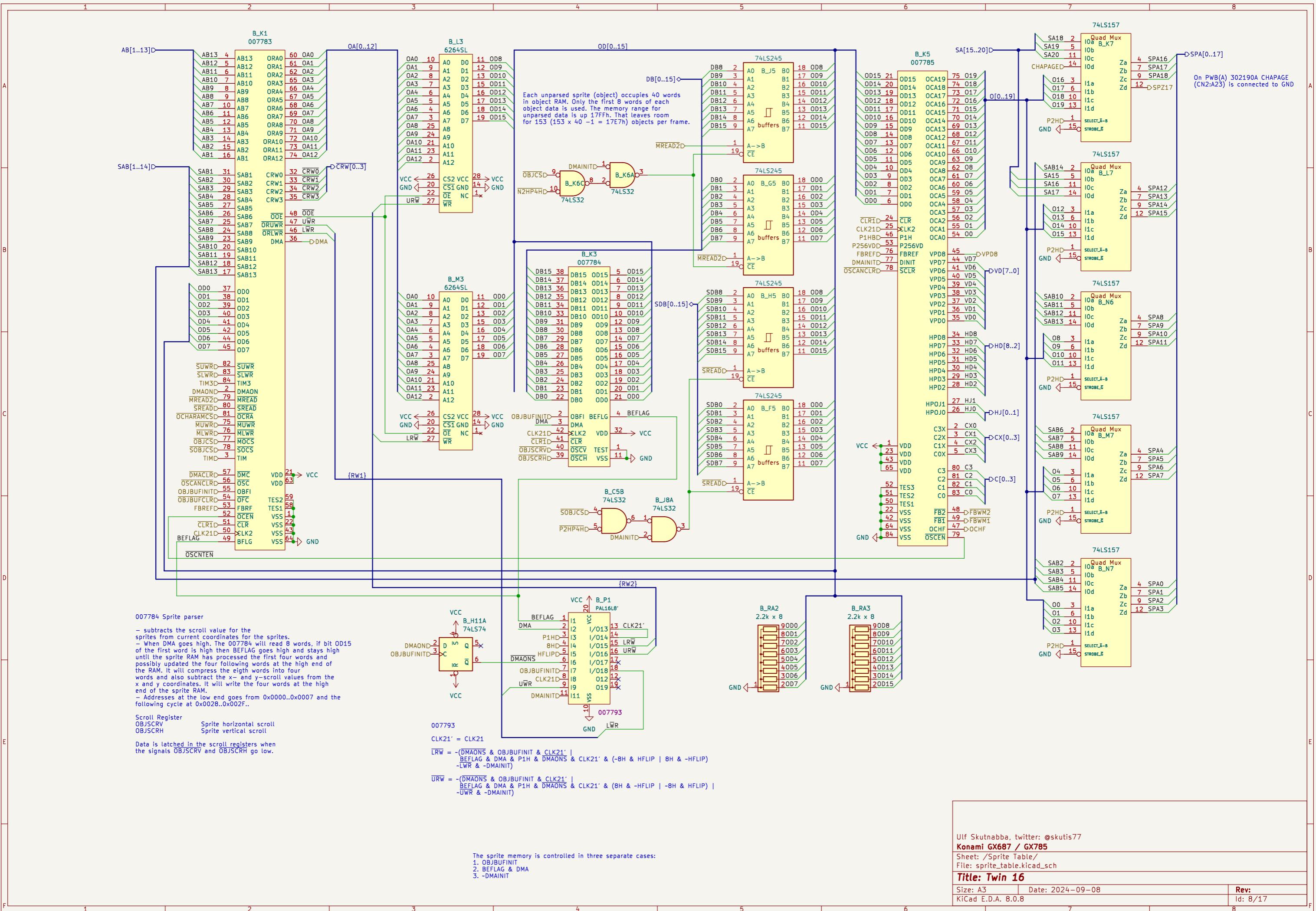
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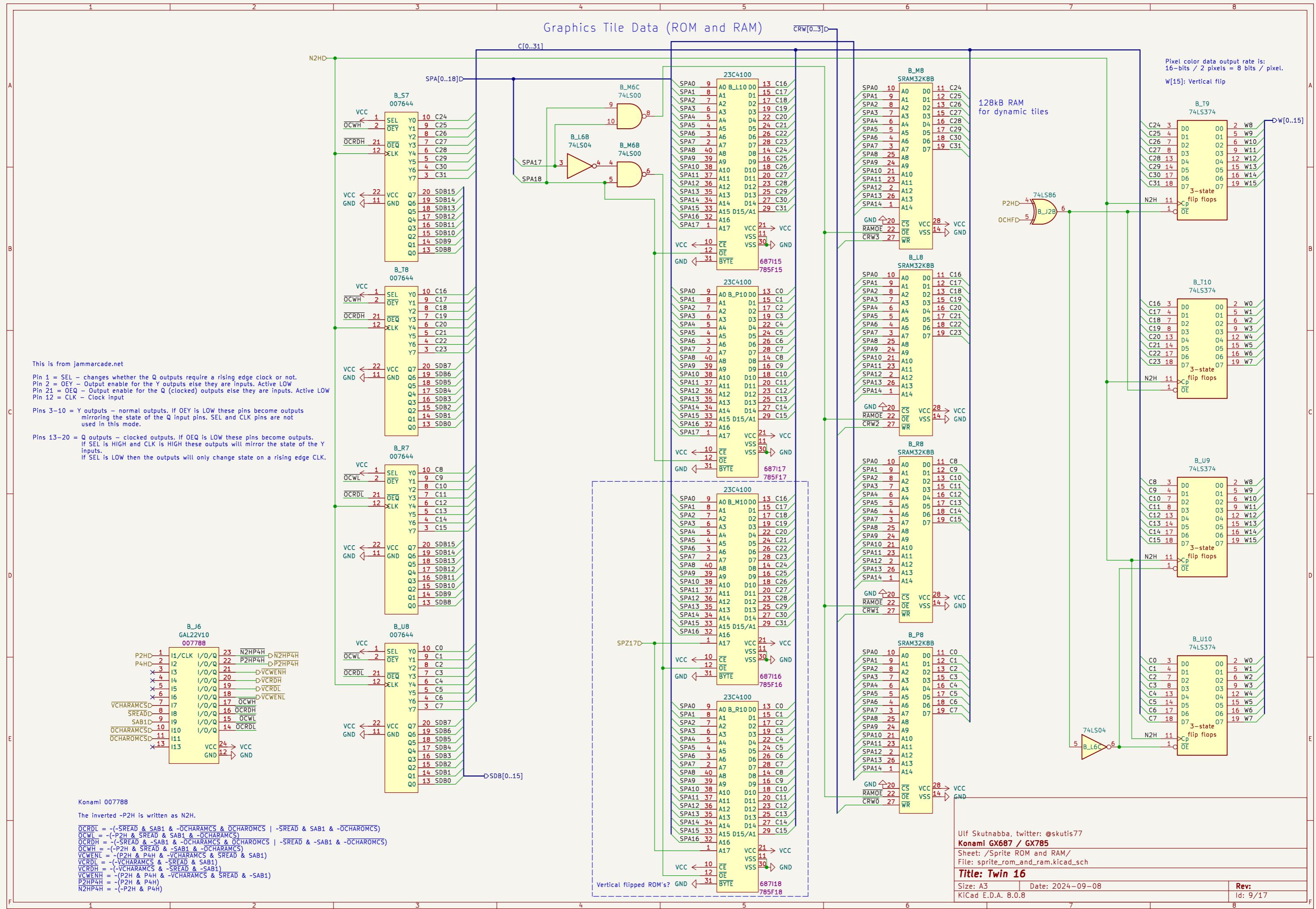
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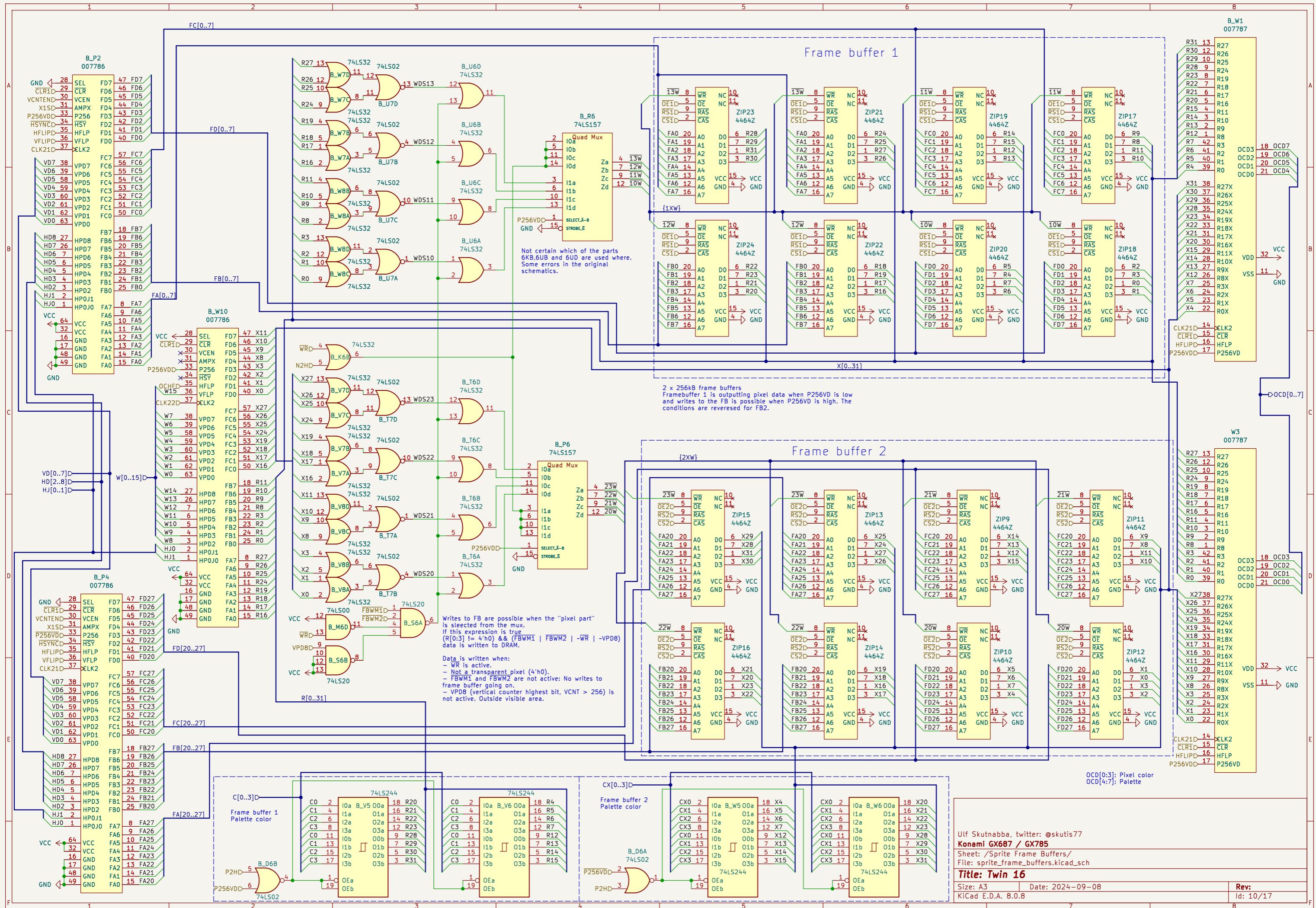
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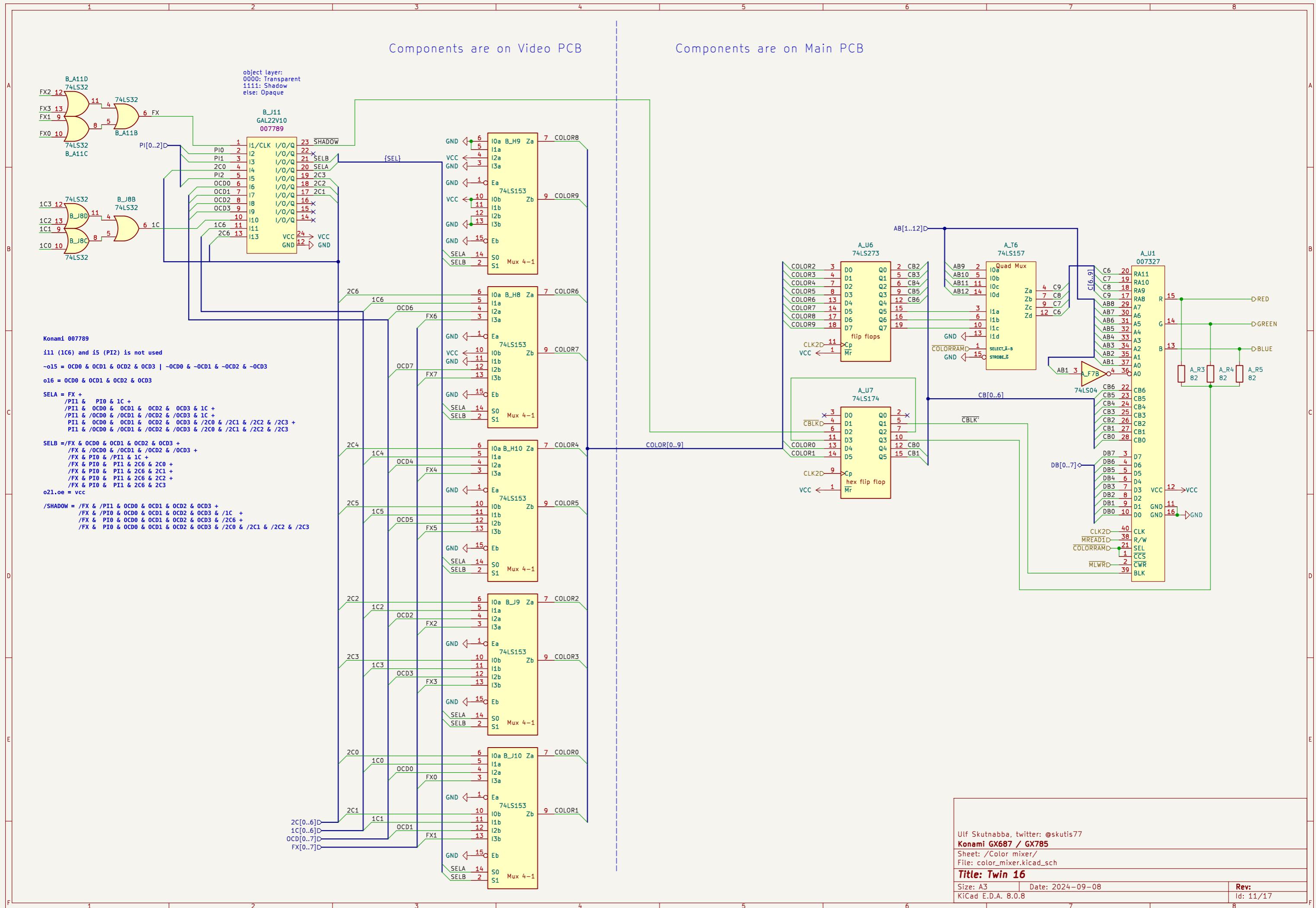
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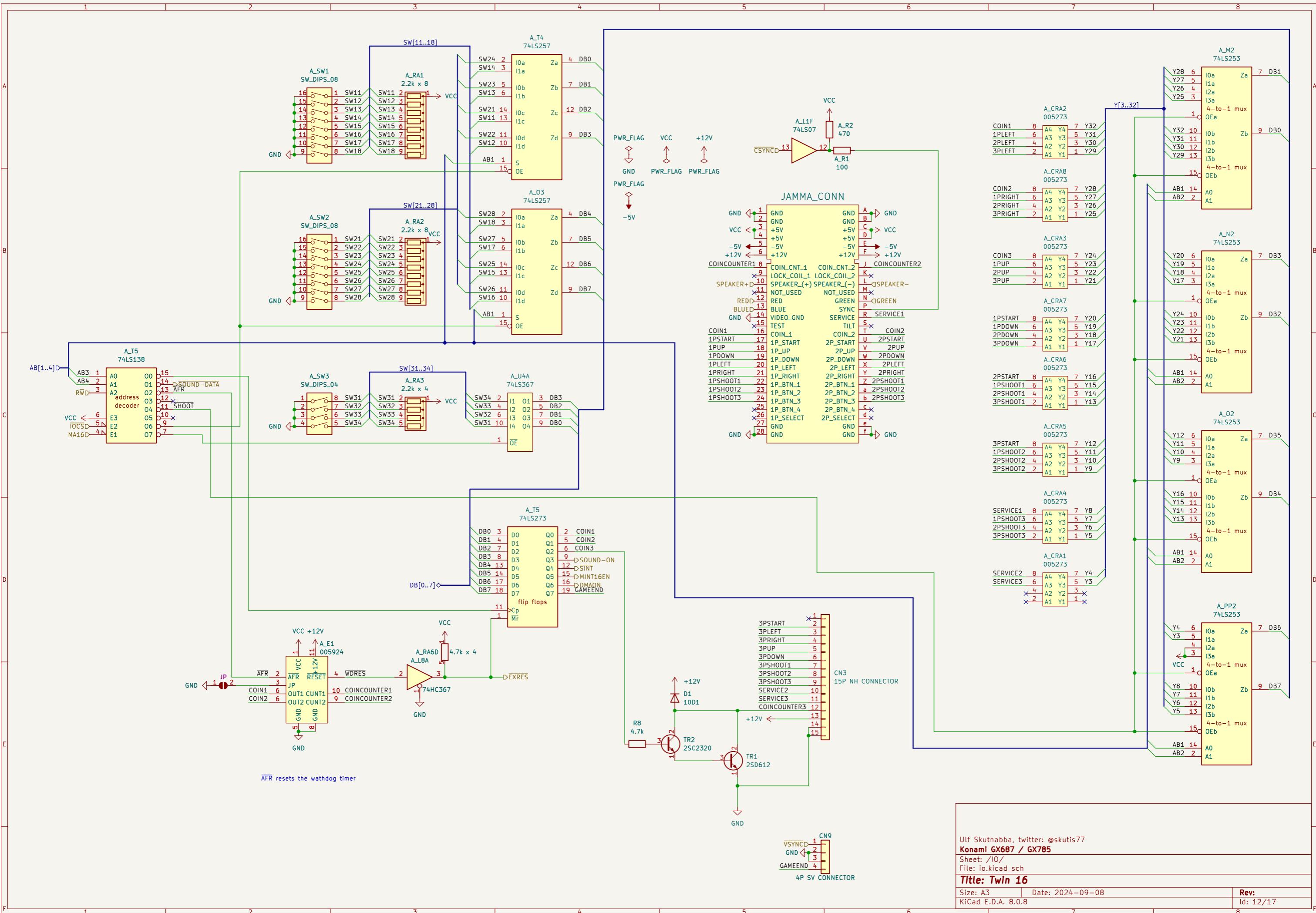


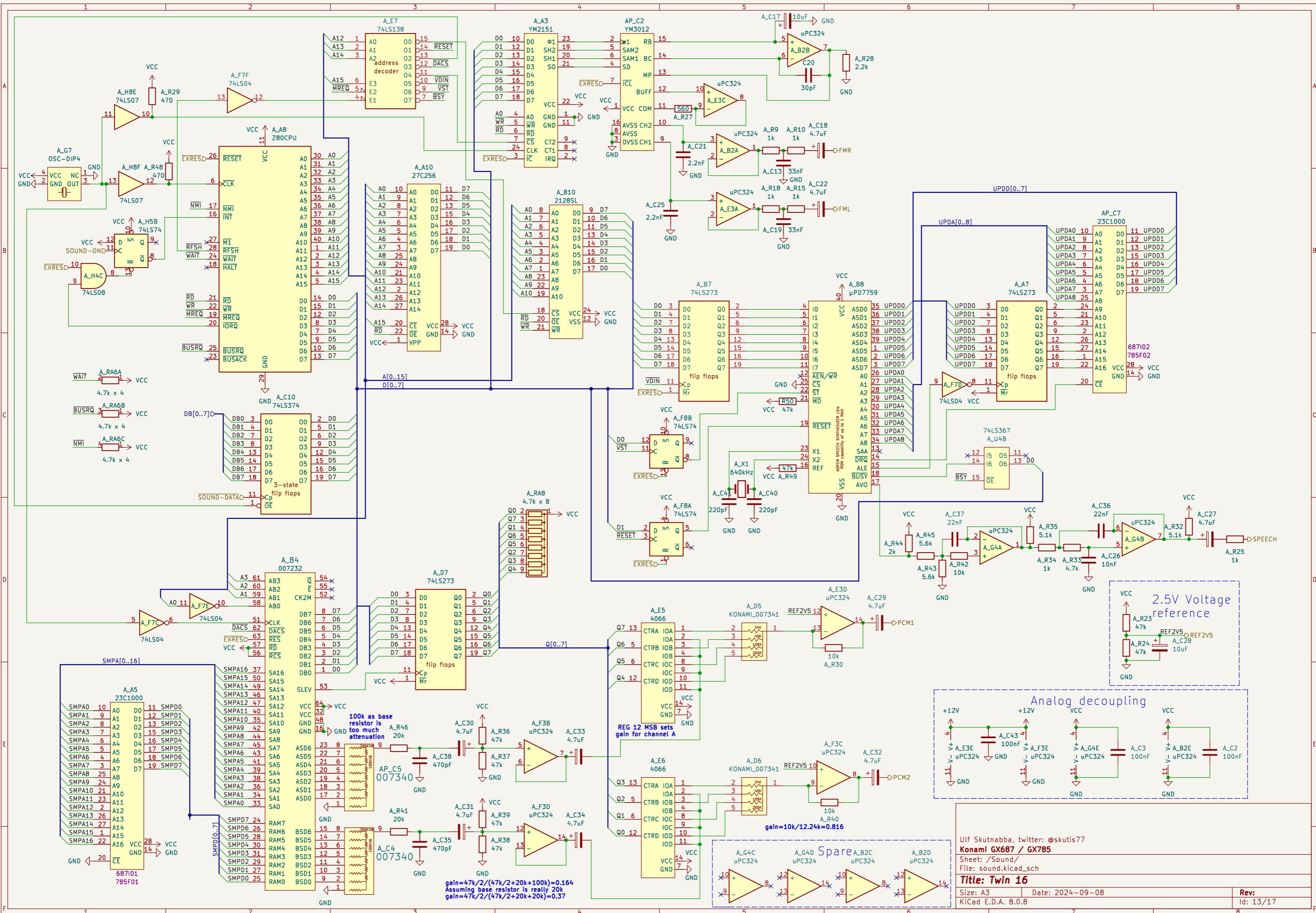




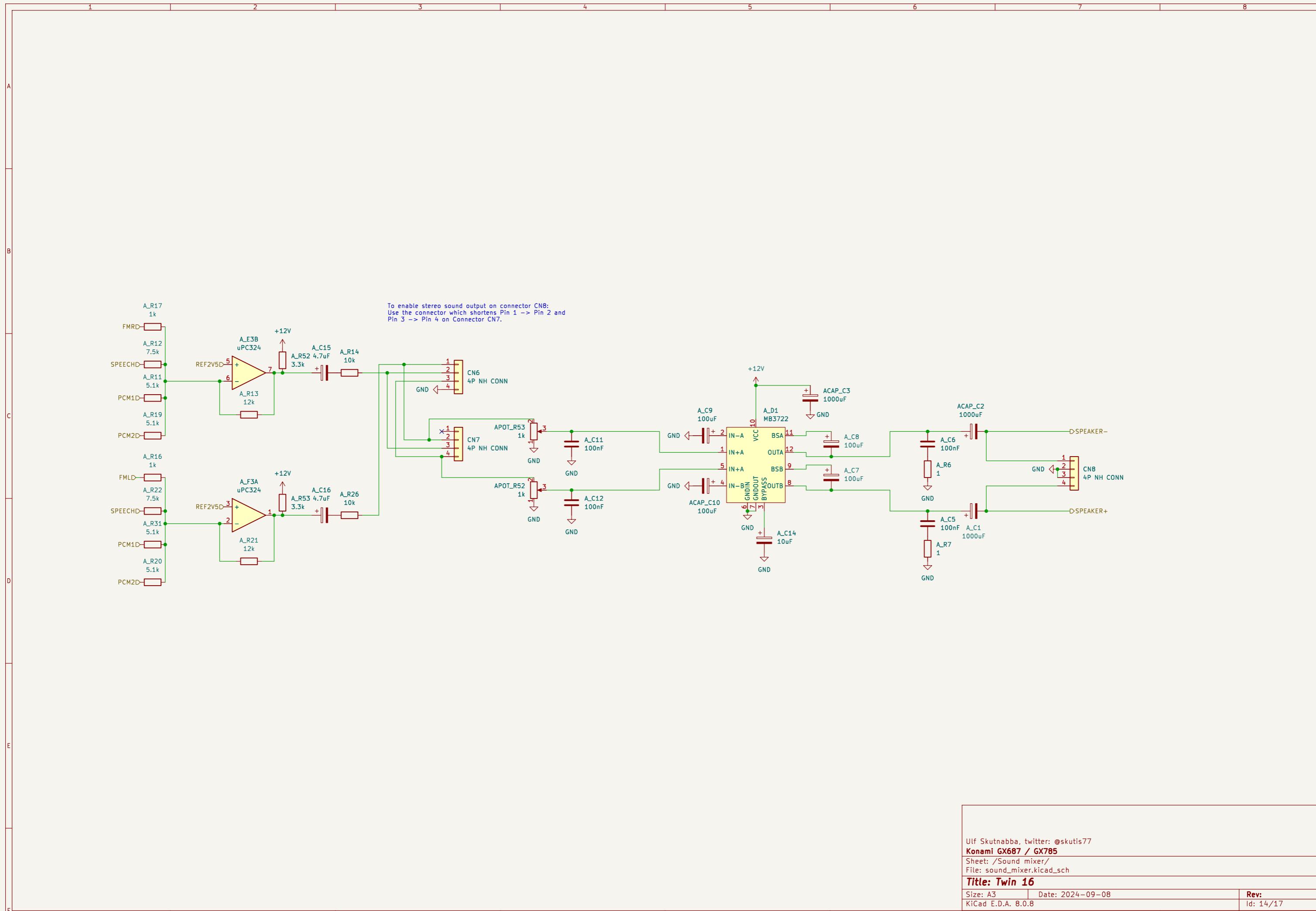




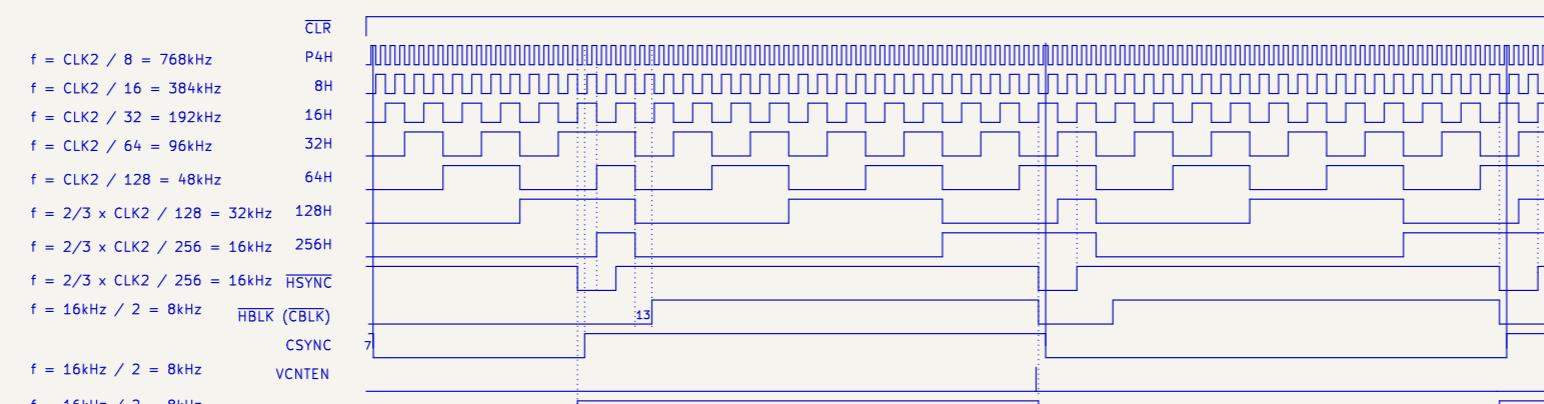




1 2 3 4 5 6 7 8



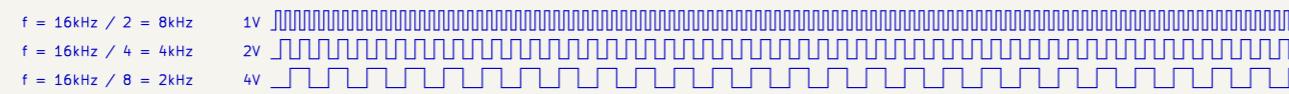
Horizontal signals



– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



Every 16th pulse is long.
Every 8th pulse is long.
Every 4th pulse is long.
Every 2nd pulse is long.
High period is longer

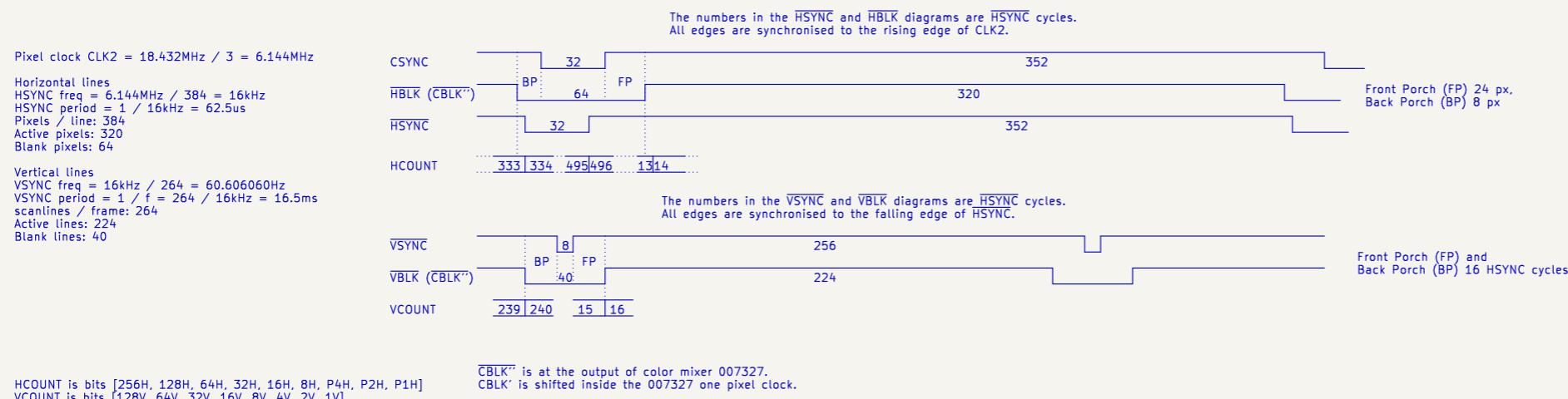
VBLANK High: 7 x 16 x 2 = 224, Low: 5 x 4 x 2 = 40
SYNCRLDV goes low 140ns before FBREF goes low.
SYNCRLDV goes high again when FBREF goes low.

OBJBUFCLR goes low one pixel clock before the rising edge
of VBLANK and high again when VBLANK goes high.

60.606Hz, OSCANCLR goes low for 140ns ~ One pixel clock cycle.
P256VD goes high/low one
P4H cycle (8 pixels) after VSYNC goes high.

FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.

Horizontal and vertical synch timing diagrams



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Sheet: /Timing diagrams/
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A

B

C

D

E

F

A

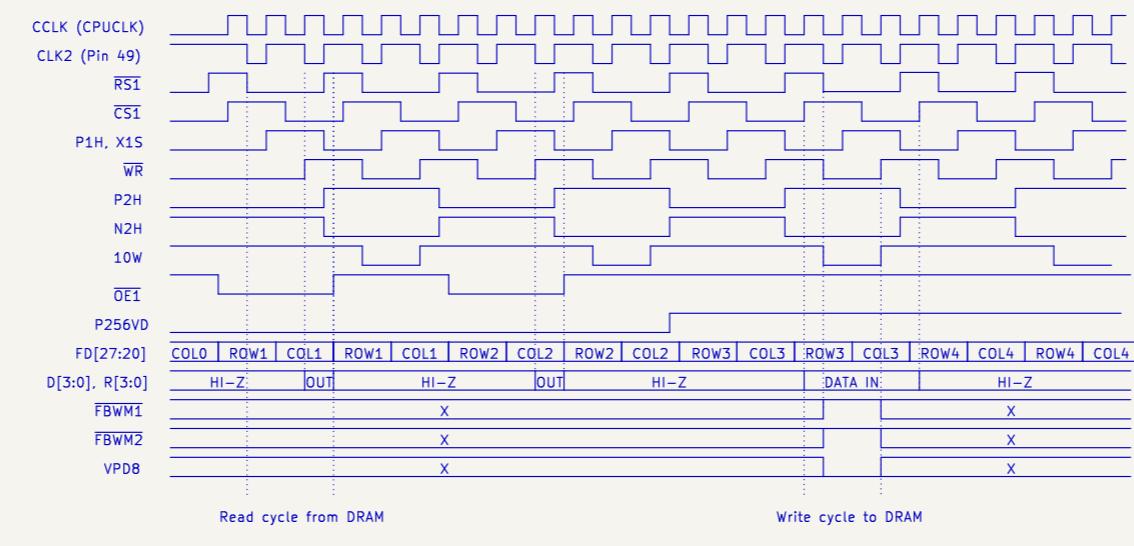
B

C

D

E

F



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