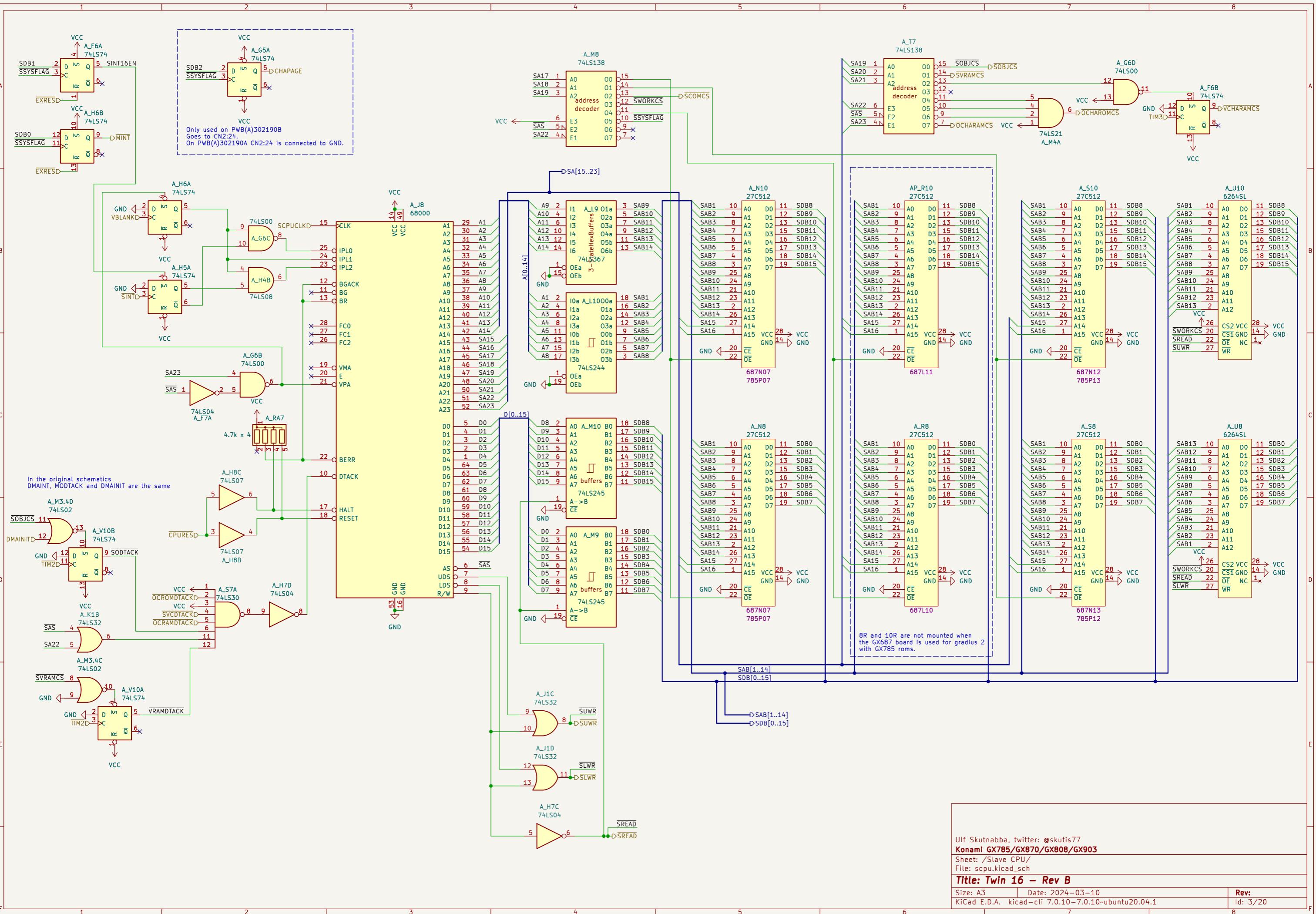


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Sheet: /Main CPU/
File: mcpu.kicad_sch

Title: Twin 16 – Rev B

Size: A3 | Date: 2024-03-10
KiCad E.D.A. kicad-cl 7.0.10-7.0.10-ubuntu20.04.1

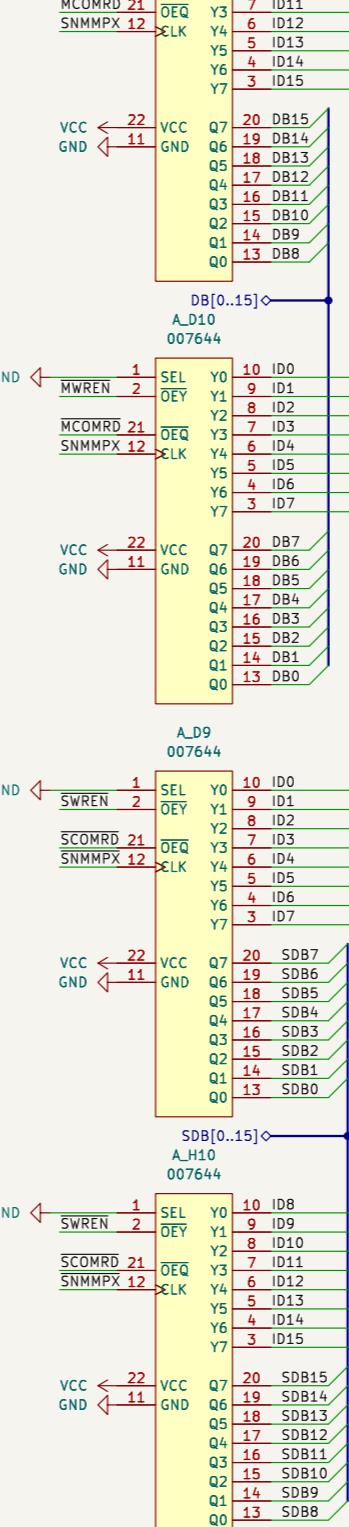
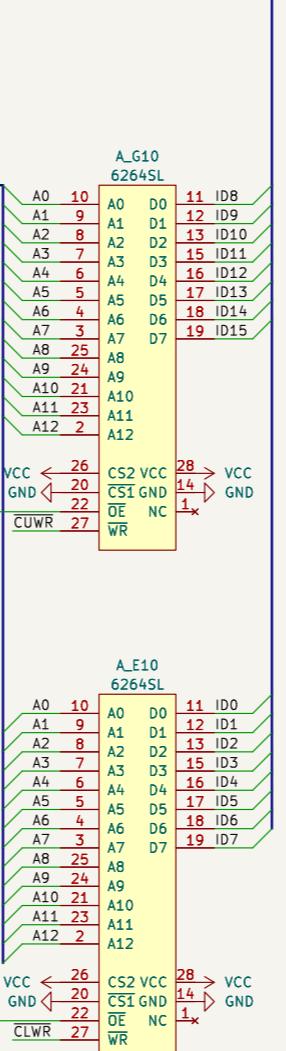
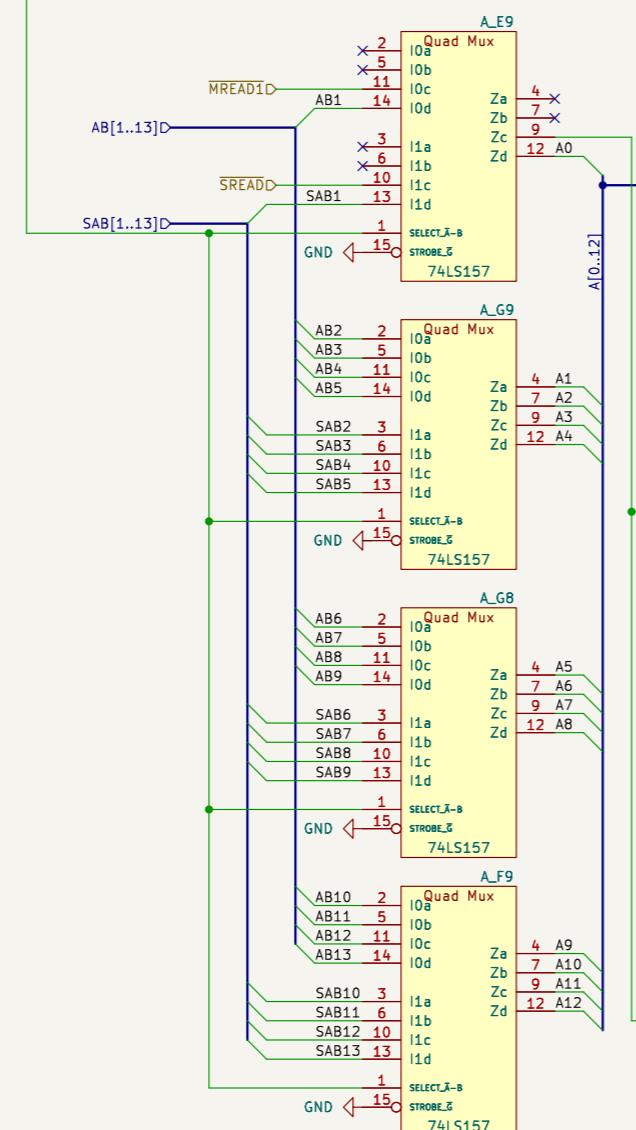
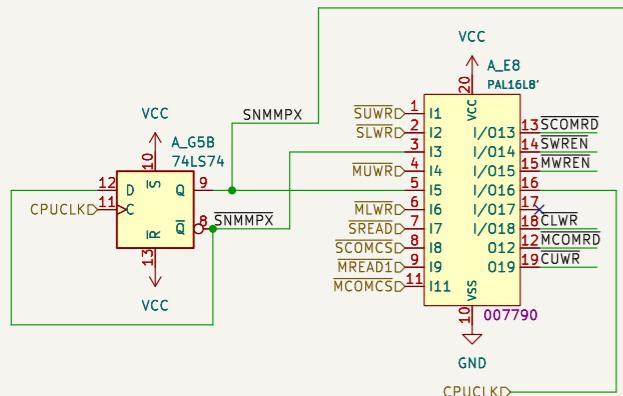
Rev: 2/20



Konami 007790

$MCOMRD = \neg(MREAD1 \& \neg MCOMCS) = MREAD1 \mid MCOMCS$
 $SCOMRD = \neg(SREAD \& \neg SCOMCS)$
 $SWREN = \neg(SNMMPPX \& SREAD \& \neg SCOMCS)$
 $MWREN = \neg(SNMMPPX \& MREAD1 \& \neg MCOMCS)$
 $CLWR = \neg(CLWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$
 $CUWR = \neg(CUWR \& \neg SNMMPPX \& SREAD \& \neg SCOMCS \& \neg CPUCLK \mid \neg MUWR \& \neg SNMMPPX \& MREAD1 \& \neg MCOMCS \& \neg CPUCLK)$

A All AND logic can be converted to OR form. But since AND logic and inverters are used in the PAL16LB device it is kept in that form. The equations follow verilog syntax. The active low signals are not inverted, the bar is there only to show activeness.



ID[0..15]

A_H9
007644

GND 1 SEL Y0 10 ID8

MWREN 2 OEV Y1 9 ID9

SCOMRD 21 OEQ Y2 8 ID10

SNMMPPX 12 CLK Y3 7 ID11

VCC 22 VCC Q7 20 DB15

GND 11 GND Q6 19 DB14

VCC 26 VCC Q5 18 DB13

GND 20 GND Q4 17 DB12

VCC 26 VCC Q3 16 DB11

GND 23 GND Q2 15 DB10

VCC 26 VCC Q1 14 DB9

GND 23 GND Q0 13 DB8

DB[0..15] 007644

A_D10
007644

GND 1 SEL Y0 10 ID0

MWREN 2 OEV Y1 9 ID1

SCOMRD 21 OEQ Y2 8 ID2

SNMMPPX 12 CLK Y3 7 ID3

VCC 22 VCC Q7 20 DB7

GND 11 GND Q6 19 DB6

VCC 26 VCC Q5 18 DB5

GND 20 GND Q4 17 DB4

VCC 26 VCC Q3 16 DB3

GND 23 GND Q2 15 DB2

VCC 26 VCC Q1 14 DB1

GND 23 GND Q0 13 DB0

SDB[0..15] 007644

A_H10
007644

GND 1 SEL Y0 10 ID8

SWREN 2 OEV Y1 9 ID9

SCOMRD 21 OEQ Y2 8 ID10

SNMMPPX 12 CLK Y3 7 ID11

VCC 22 VCC Q7 20 SDB7

GND 11 GND Q6 19 SDB6

VCC 26 VCC Q5 18 SDB5

GND 20 GND Q4 17 SDB4

VCC 26 VCC Q3 16 SDB3

GND 23 GND Q2 15 SDB2

VCC 26 VCC Q1 14 SDB1

GND 23 GND Q0 13 SDB0

SDB[0..15] 007644

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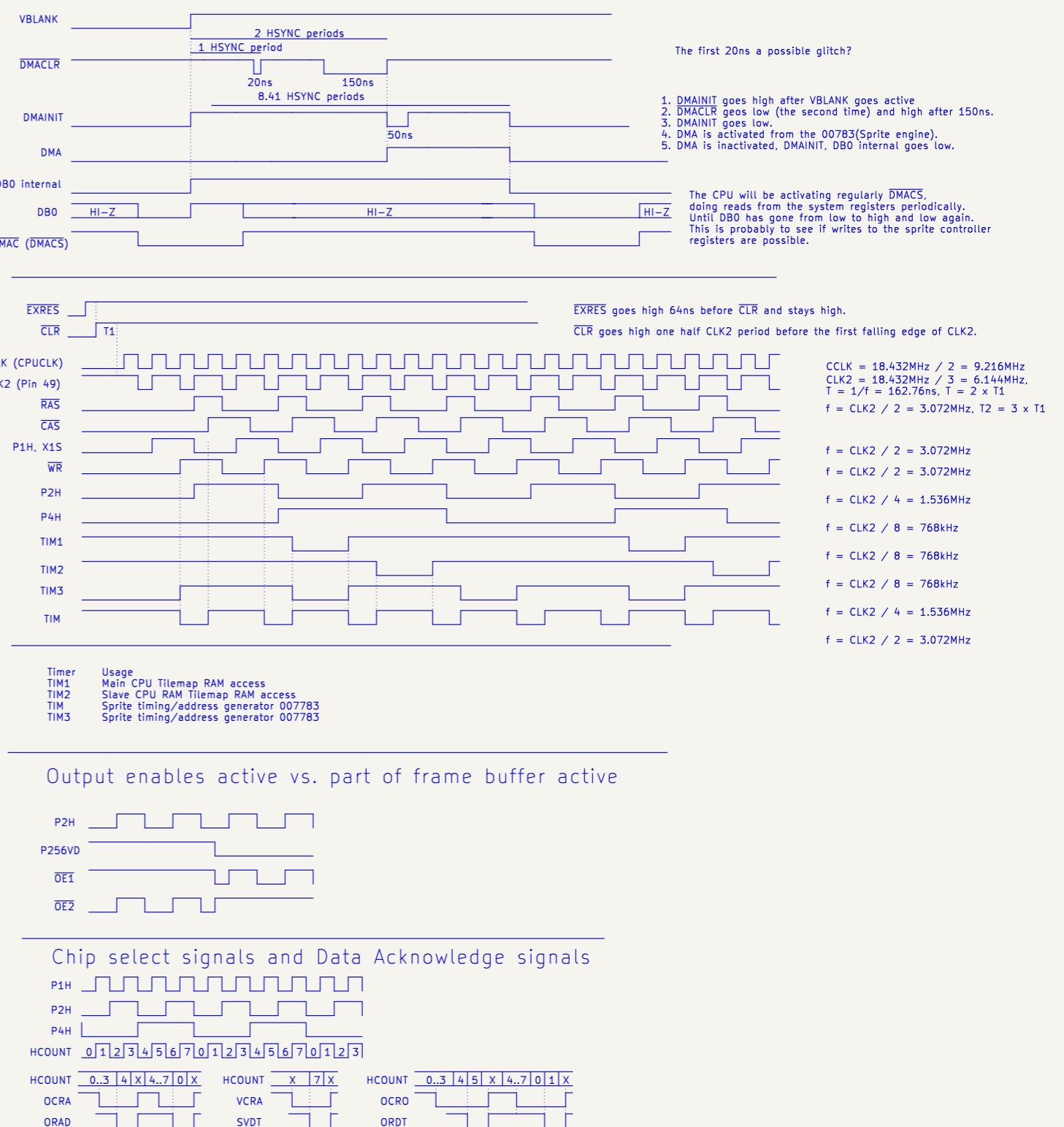
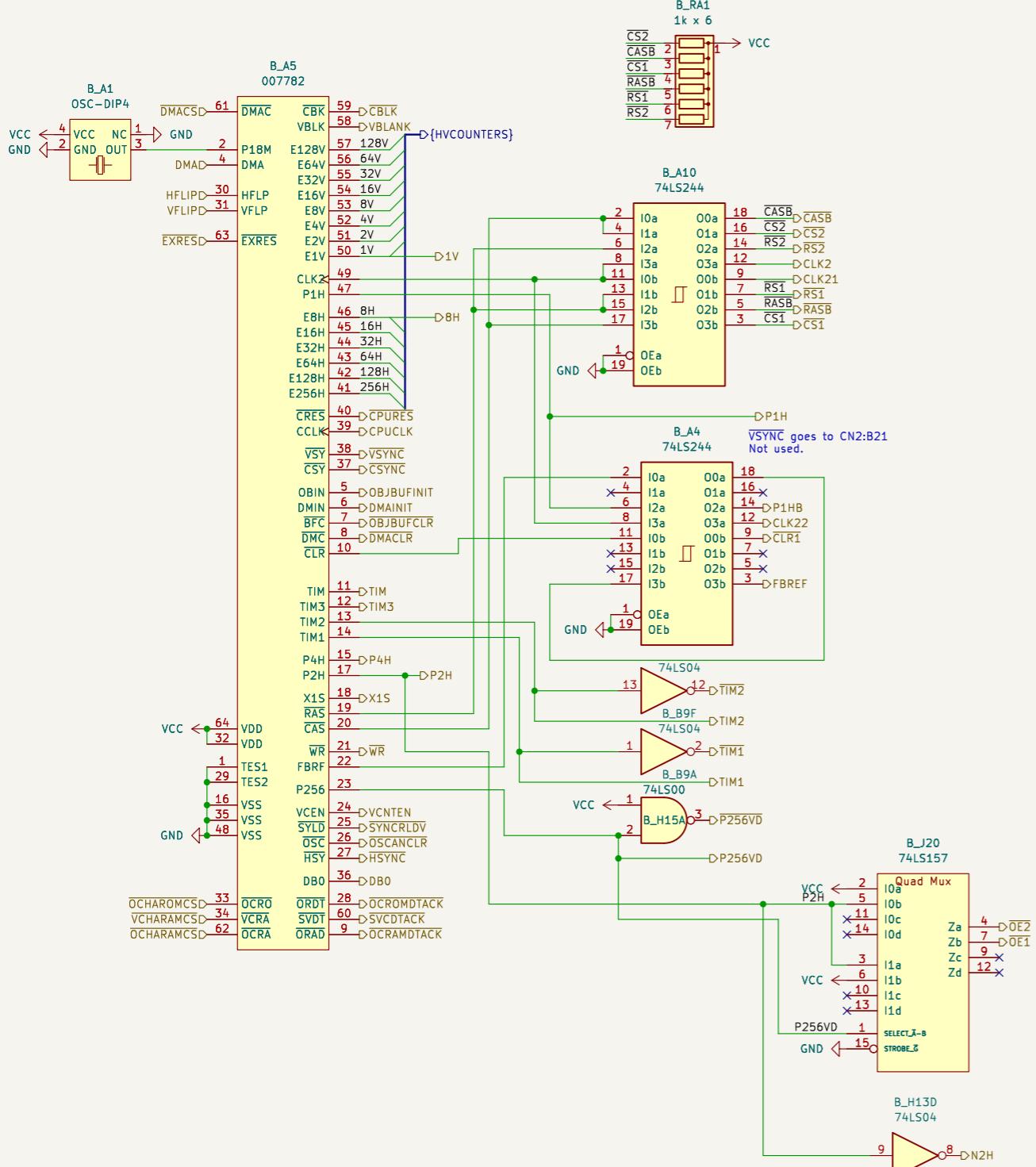
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Title: Twin 16 – Rev B

Size: A3	Date: 2024-03-10
KiCad E.D.A. kicad-cl 7.0.10-7.0.10-ubuntu20.04.1	Rev:

Id: 4/20	F
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DMA Synchronization



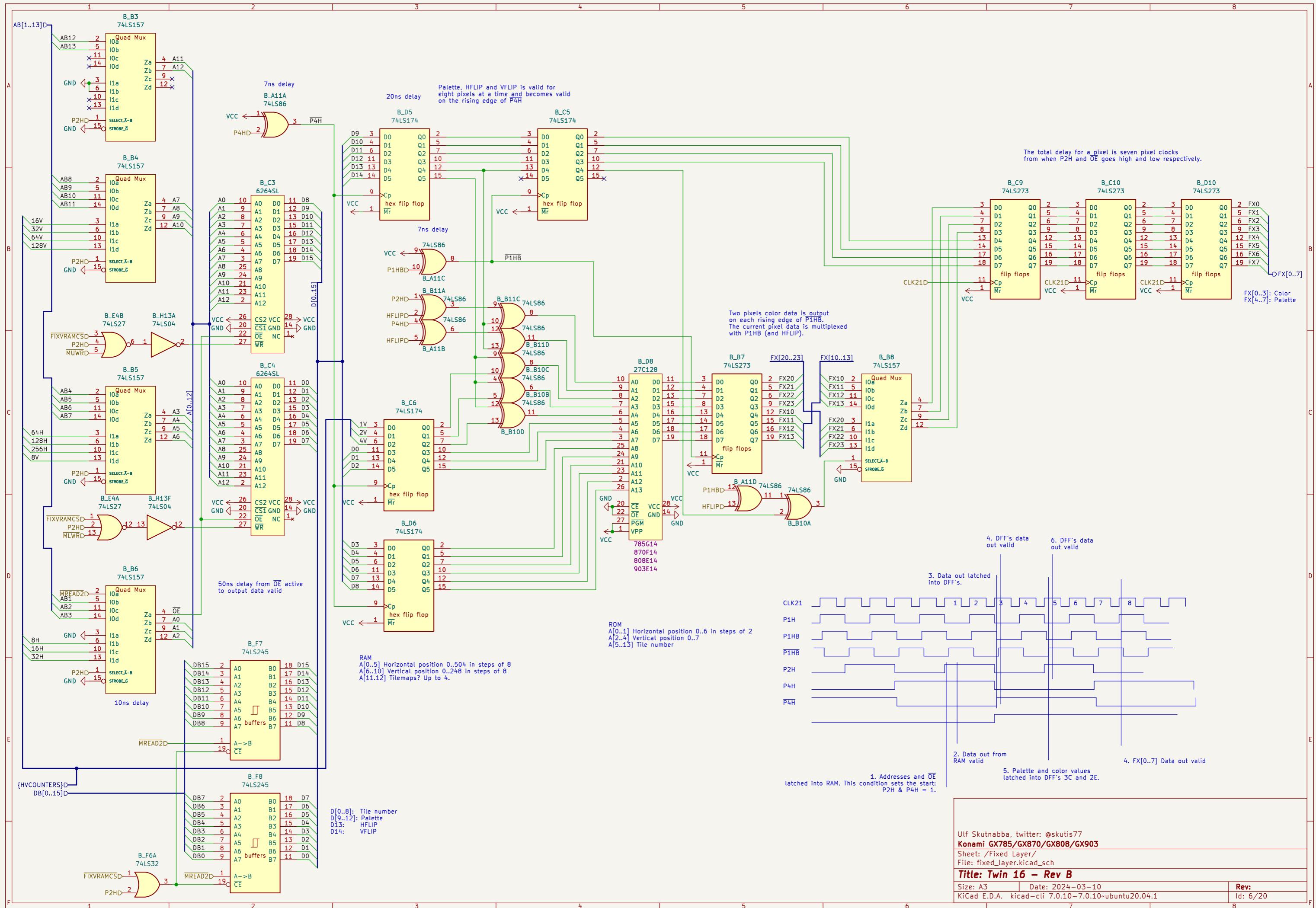
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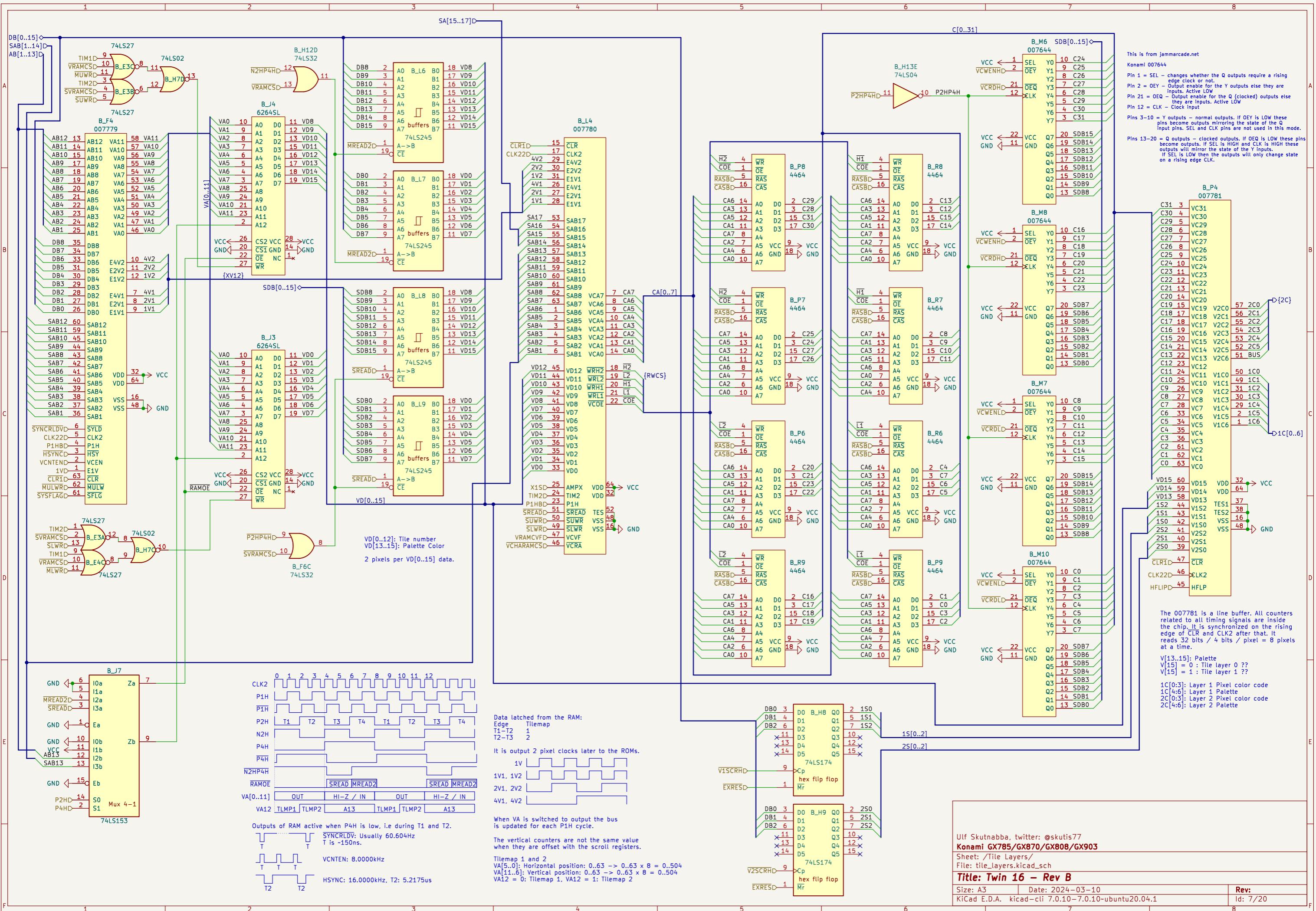
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File: timing.kicad_sch

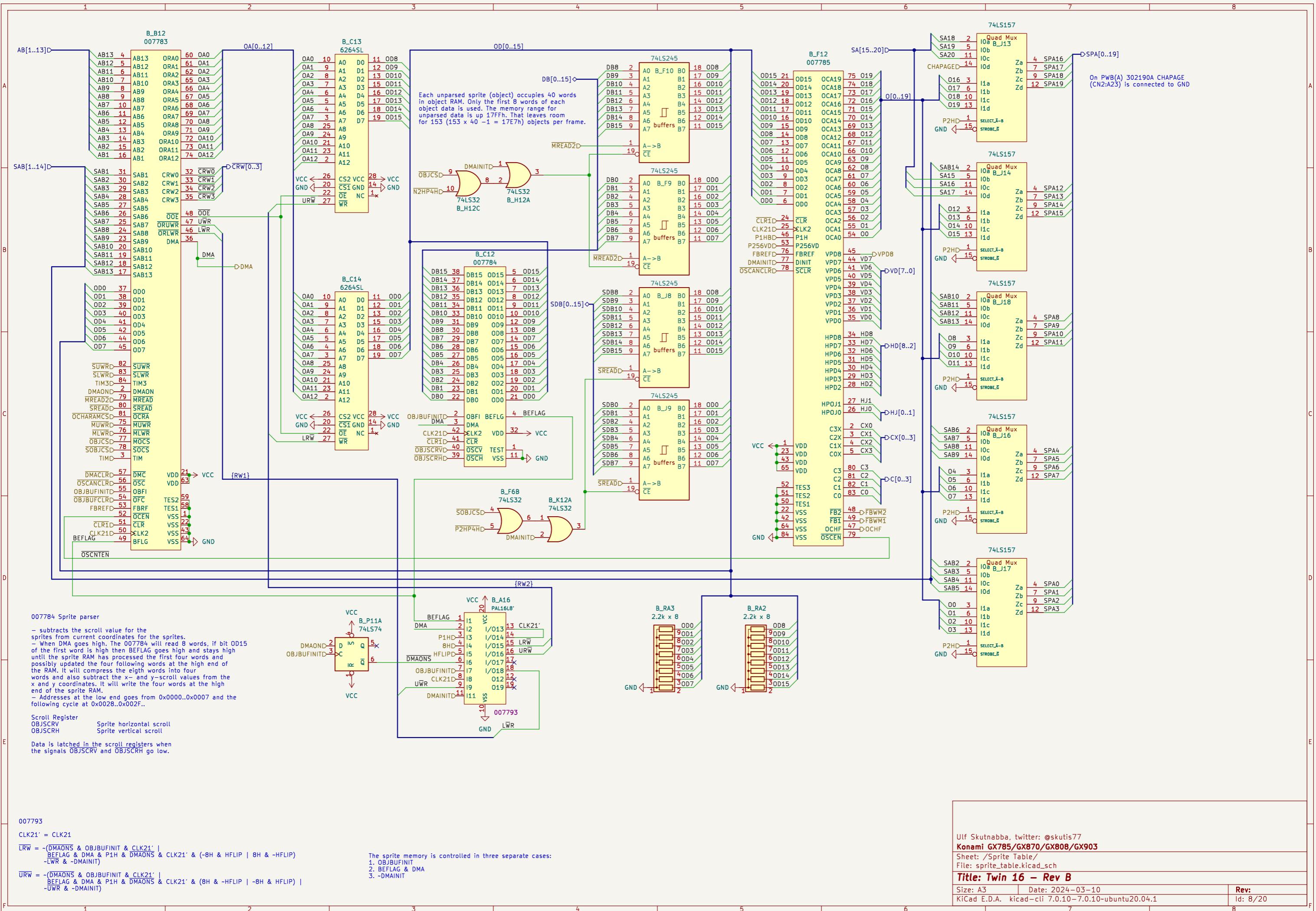
Title: Twin 16 – Rev B

Size: A3 | Date: 2024-03-10
KiCad E.D.A. kicad-cl 7.0.10-7.0.10-ubuntu20.04.1

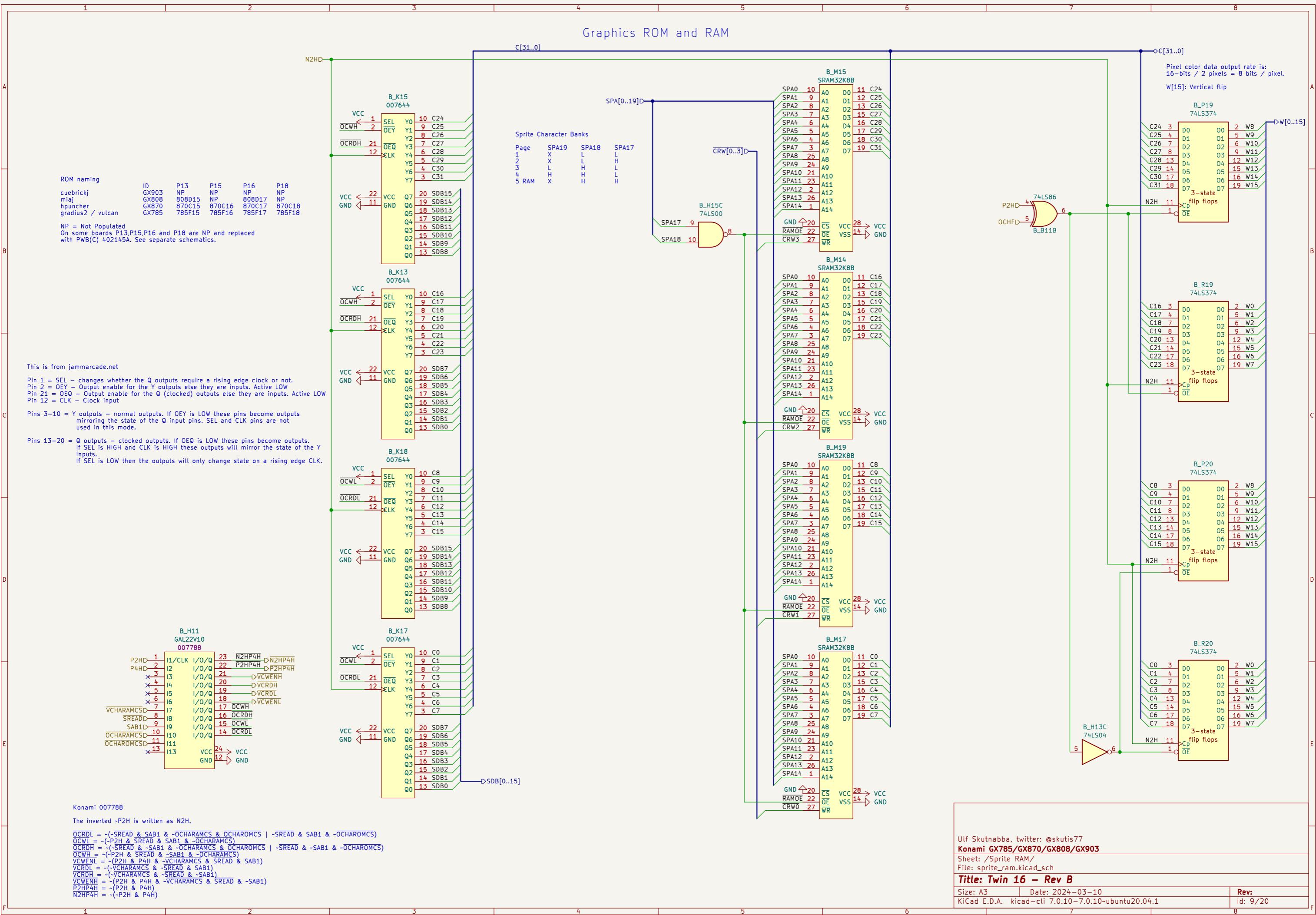
Rev: 5/20

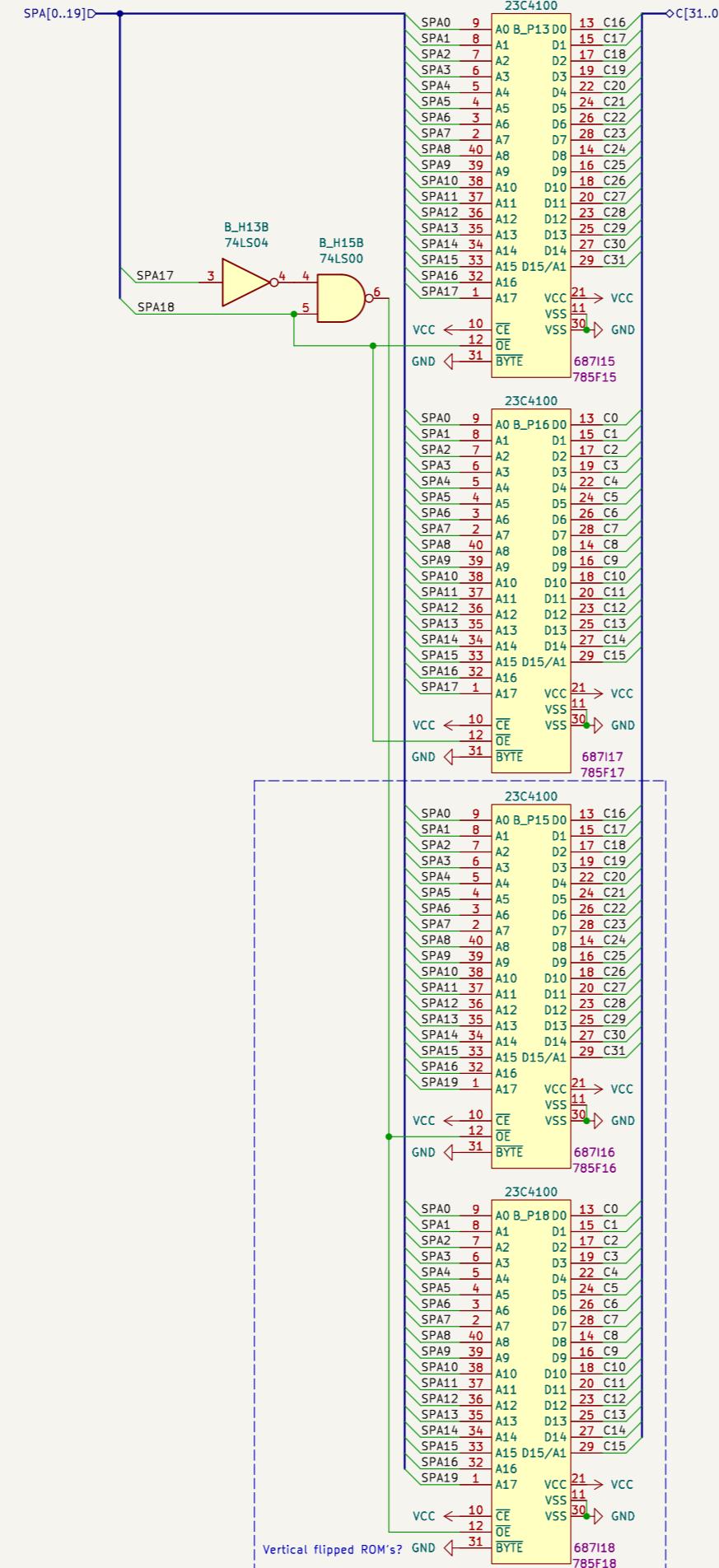






Graphics ROM and RAM



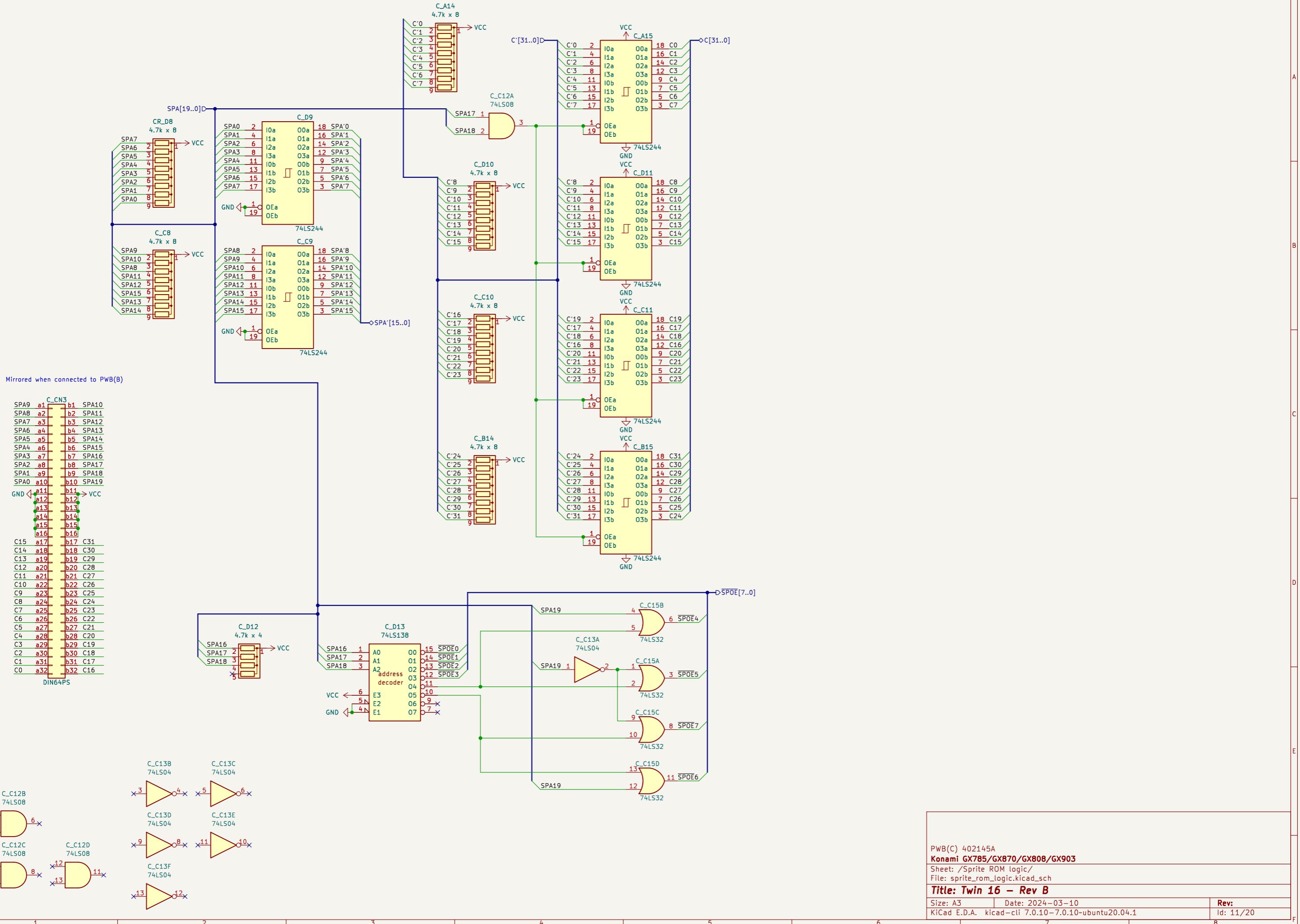


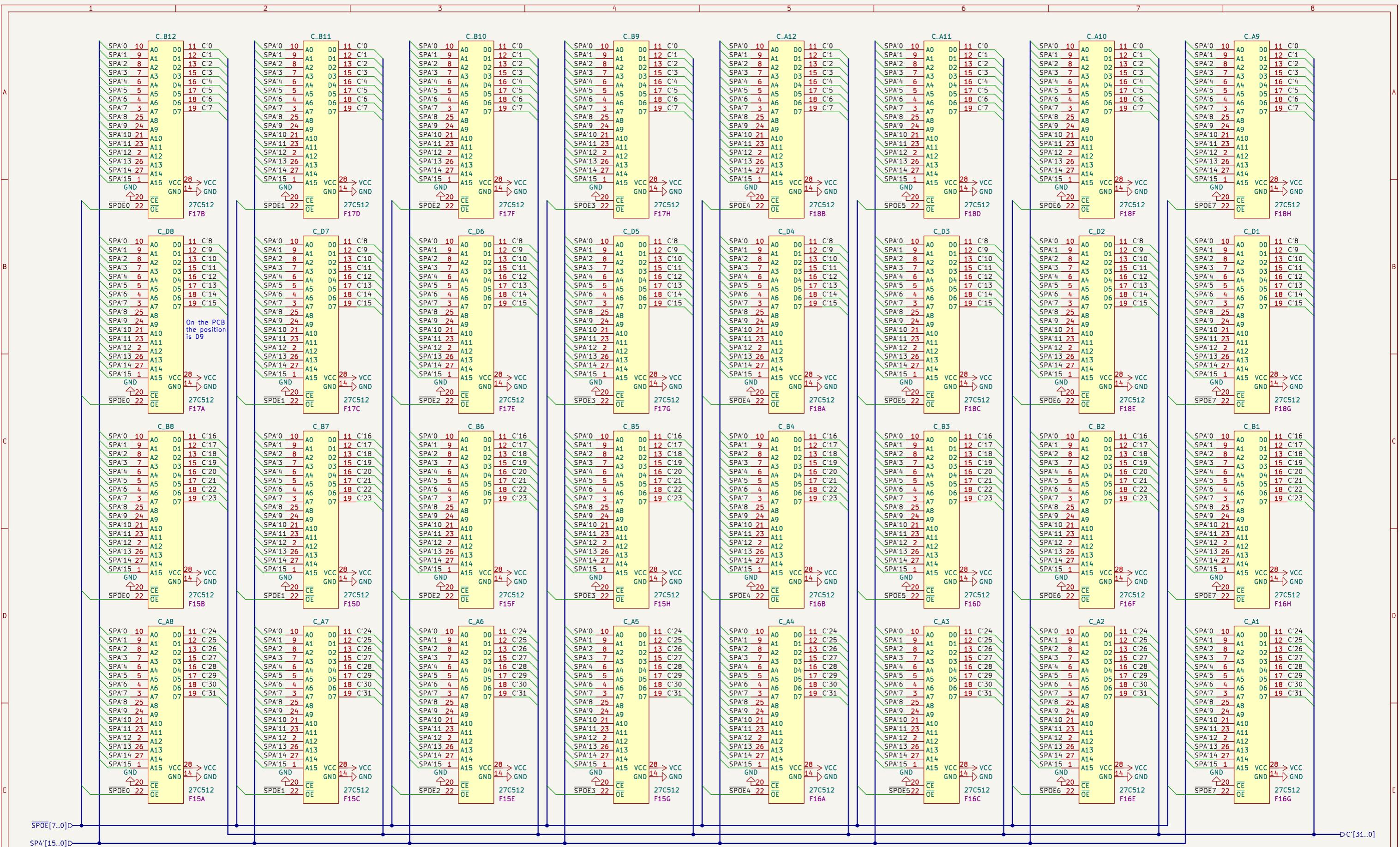
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File: sprite_rom_1.kicad_sch

Title:

Size: A3 Date: 2024-03-10
KiCad E.D.A. kicad-cli 7.0.10-7.0.10~ubuntu20.04.1

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Id: 10/20





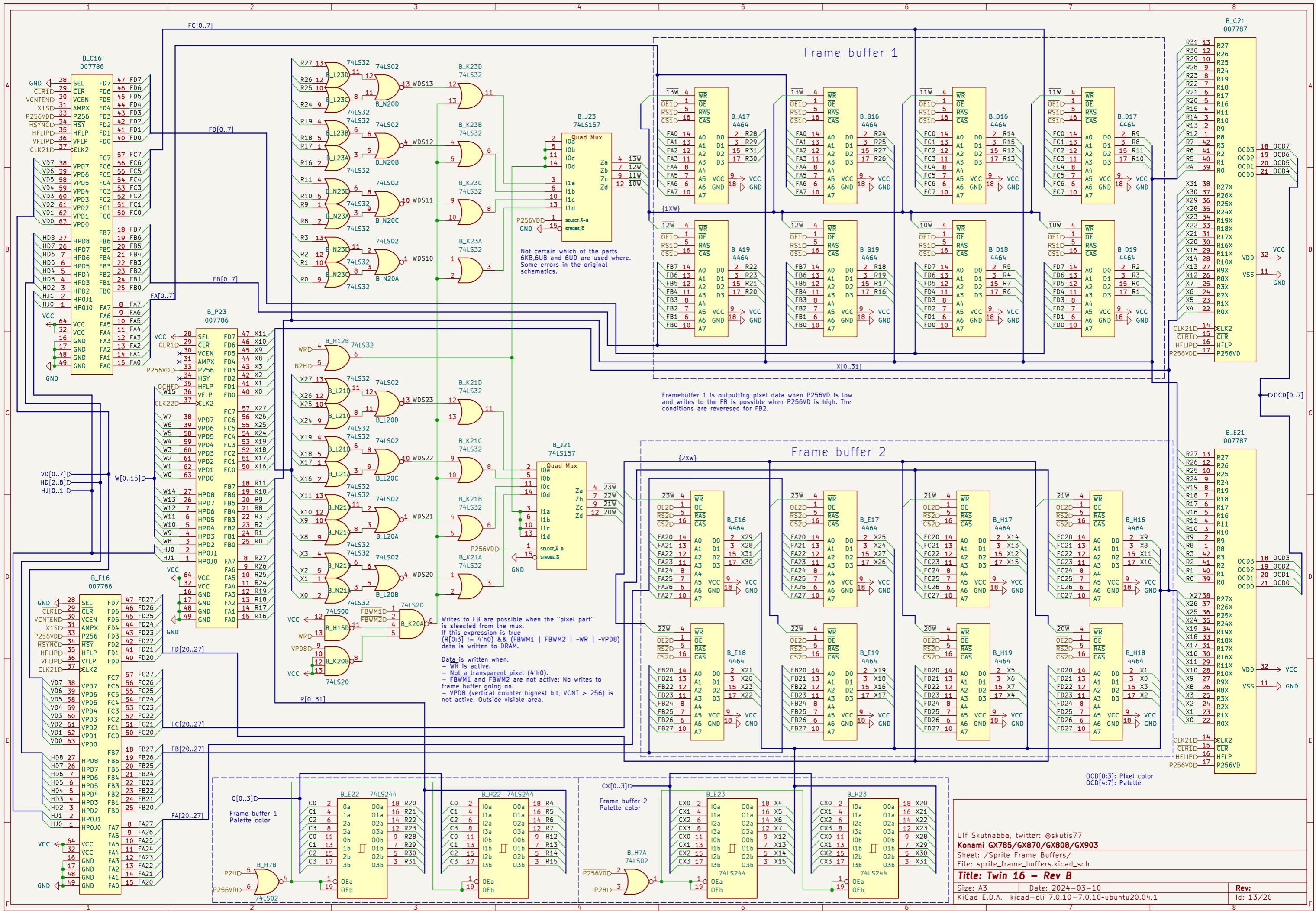
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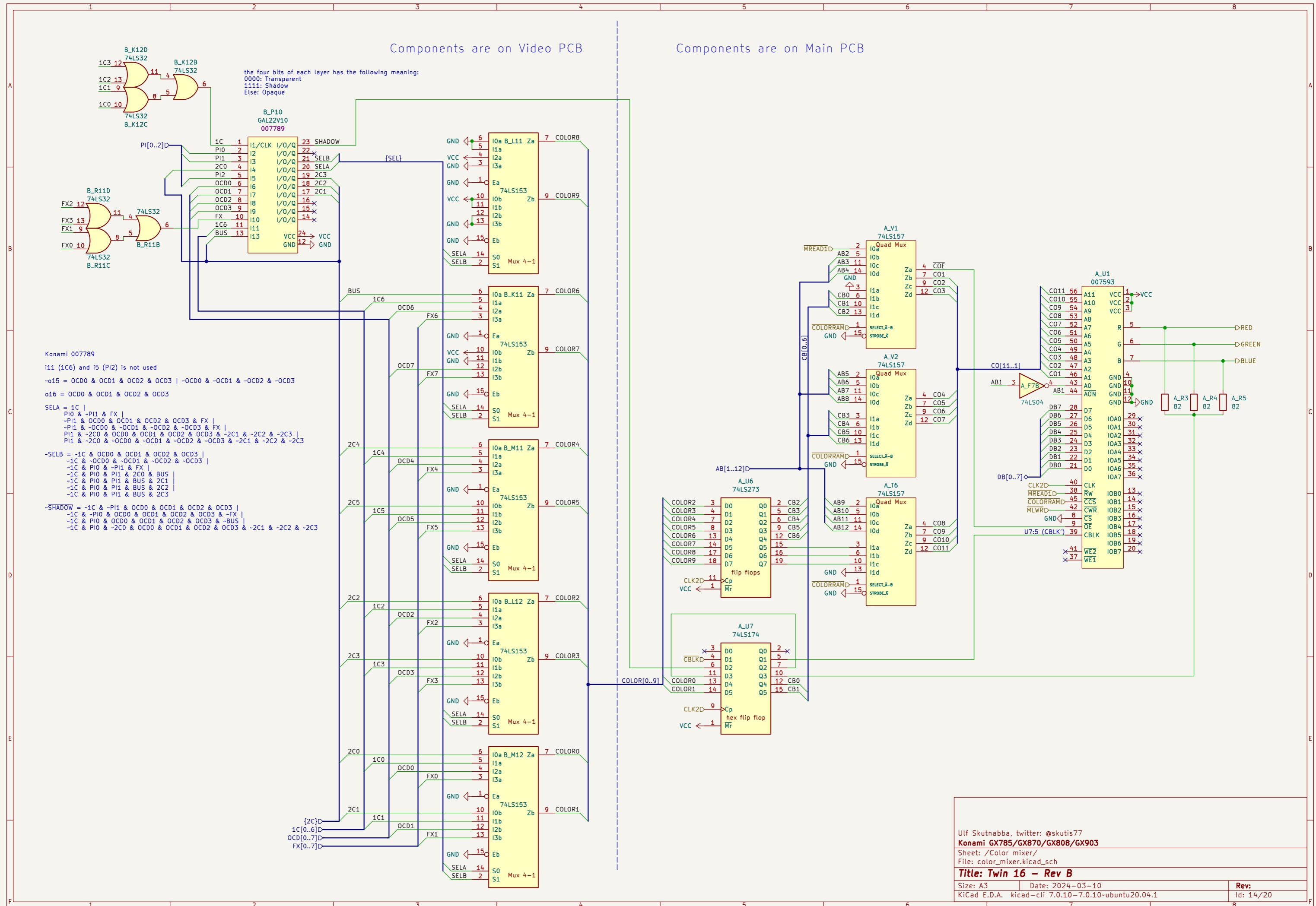
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File: sprite_rom_2.kicad_sch

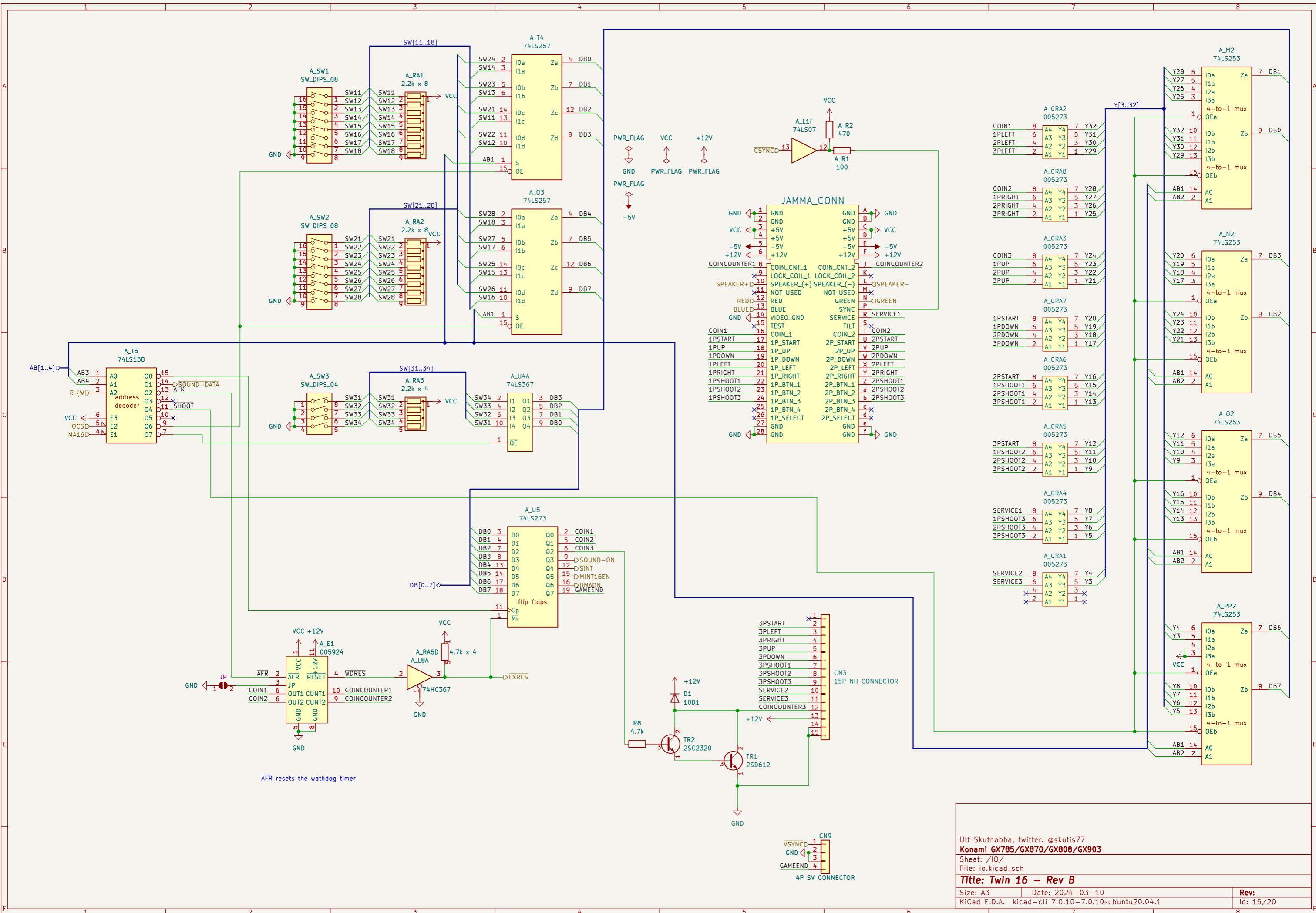
Title: Twin 16 – Rev B

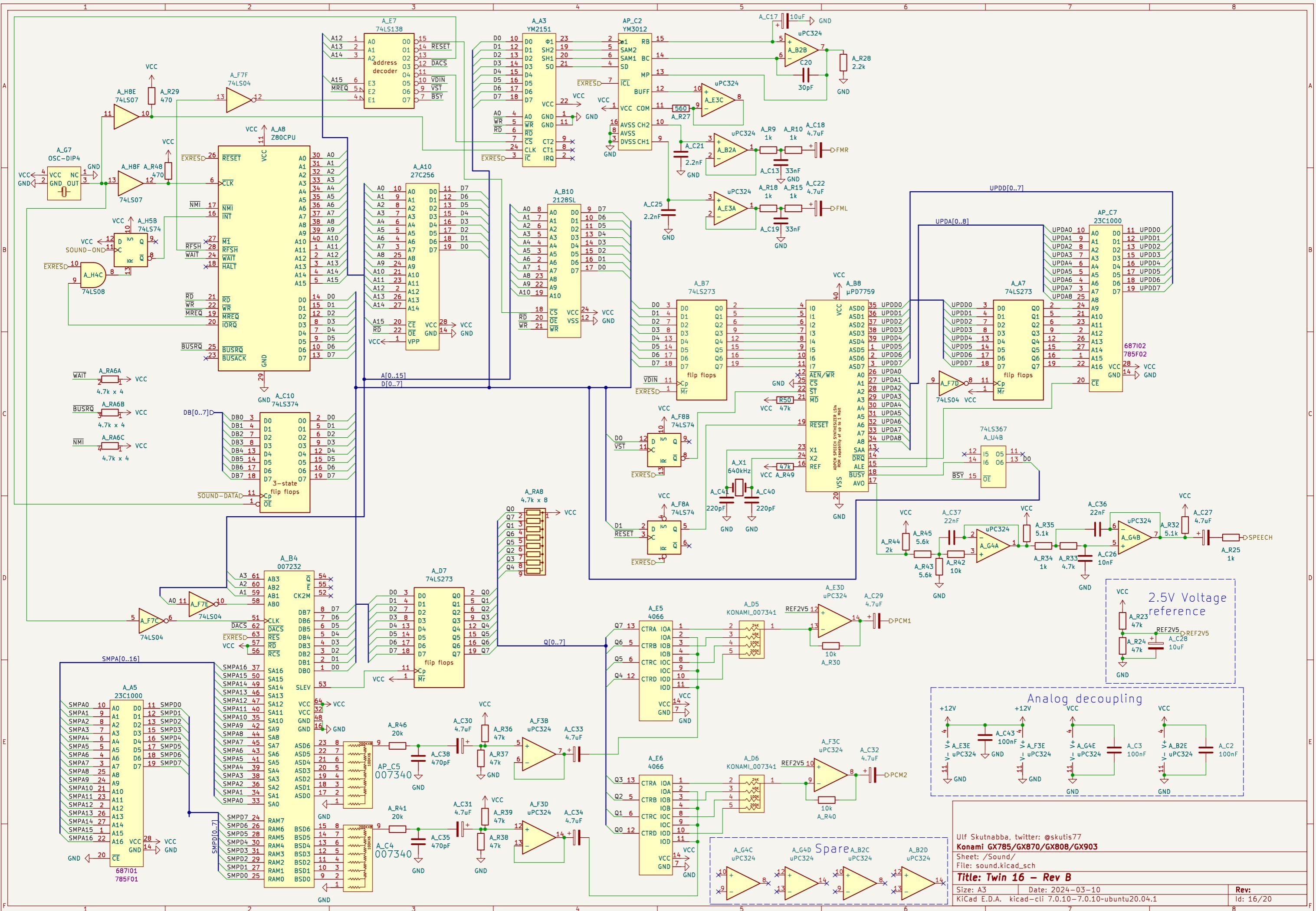
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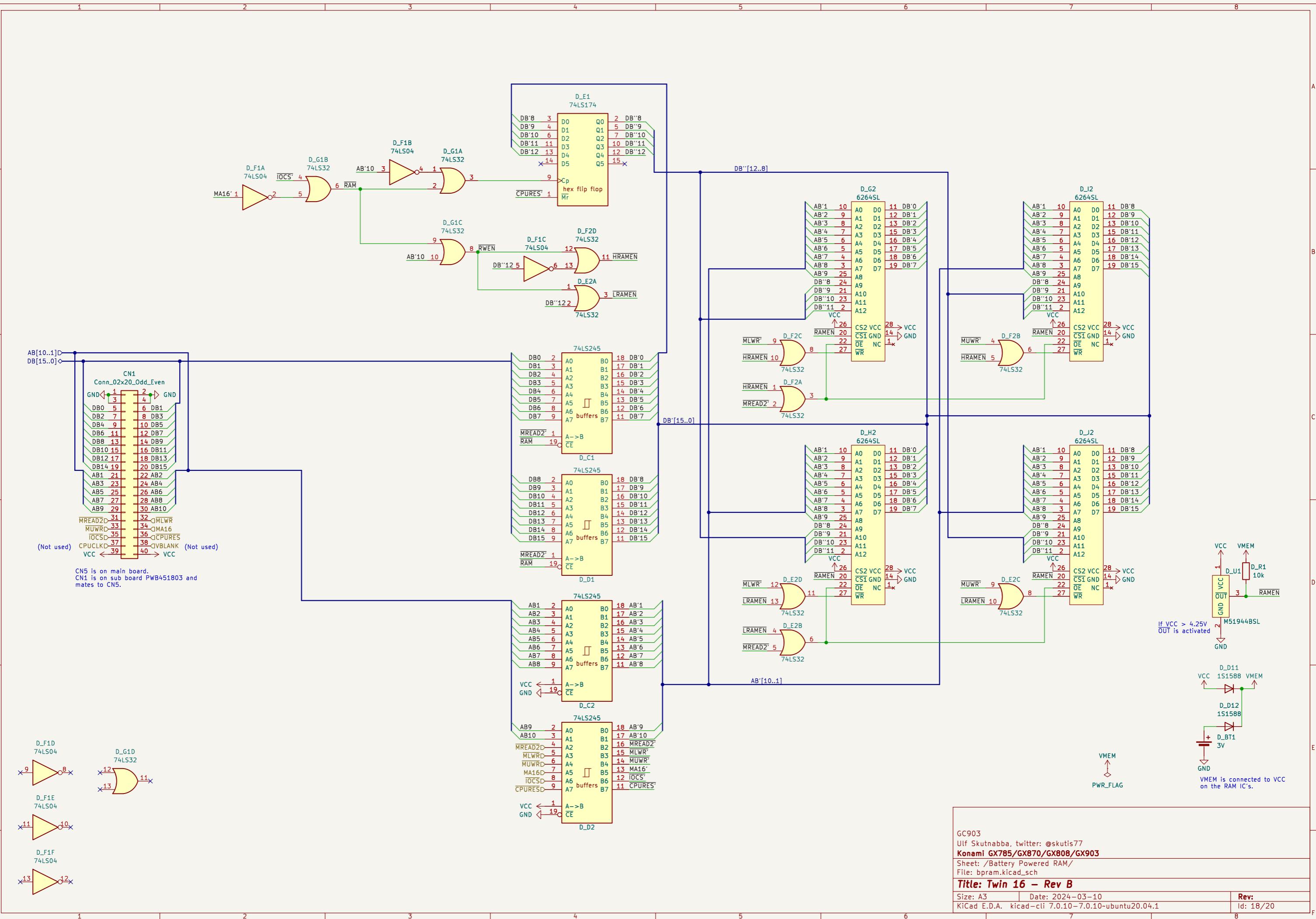
7 8



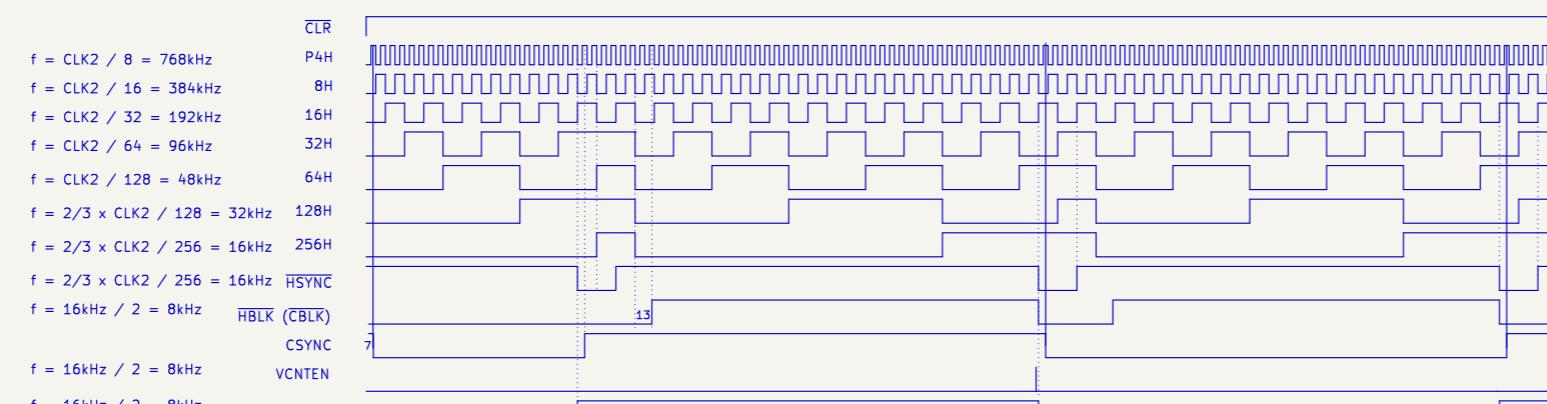








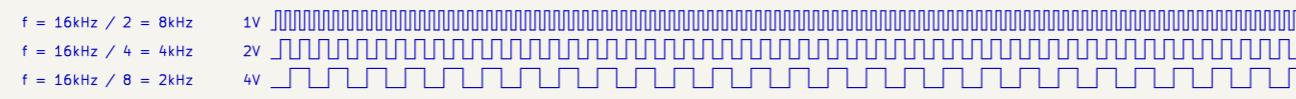
Horizontal signals



– The first VCNTEN is skipped after reset.
It goes low 140ns before HSYNC goes low,
and high again when HSYNC goes low.
VCNTEN is active right before every second falling edge of
HSYNC.

– CPURES goes high, and stays high, on the seventh falling edge
of HSYNC.

Vertical signals



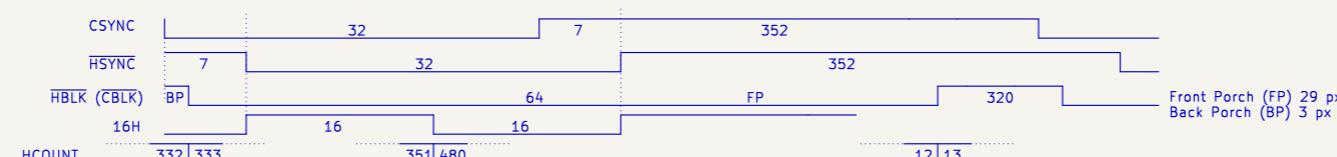
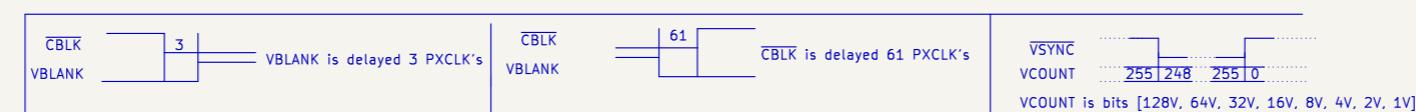
Every 16th pulse is long.
Every 8th pulse is long.
Every 4th pulse is long.
Every 2nd pulse is long.
High period is longer

VBLANK High: $7 \times 16 \times 2 = 224$, Low: $5 \times 4 \times 2 = 40$
SYNCRLDV goes low 140ns before FBREF goes low.
SYNCRLDV goes high again when FBREF goes low.

OBJBUFCLR goes low one pixel clock before the rising edge
of VBLANK and high again when VBLANK goes high.

60.606Hz, OSCANCLR goes low for 140ns ~ One pixel clock cycle.
P256VD goes high/low one
P4H cycle (8 pixels) after VSYNC goes high.

FBREF is measured at pin 22. At U186:3 FBREF is delayed by 22ns going high and 12ns going low.



The horizontal blanking part is shown of the composite blanking signals.

HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]

HSYNC = $6.144\text{MHz} / 384 = 16\text{kHz}$

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Sheet: /Timing diagrams/

File: timing_diagrams.kicad_sch

Title: Twin 16 – Rev B

Size: A3 Date: 2024-03-10
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Rev: Id: 19/20

