

Ulf Skutnabba, twitter: @skutis77

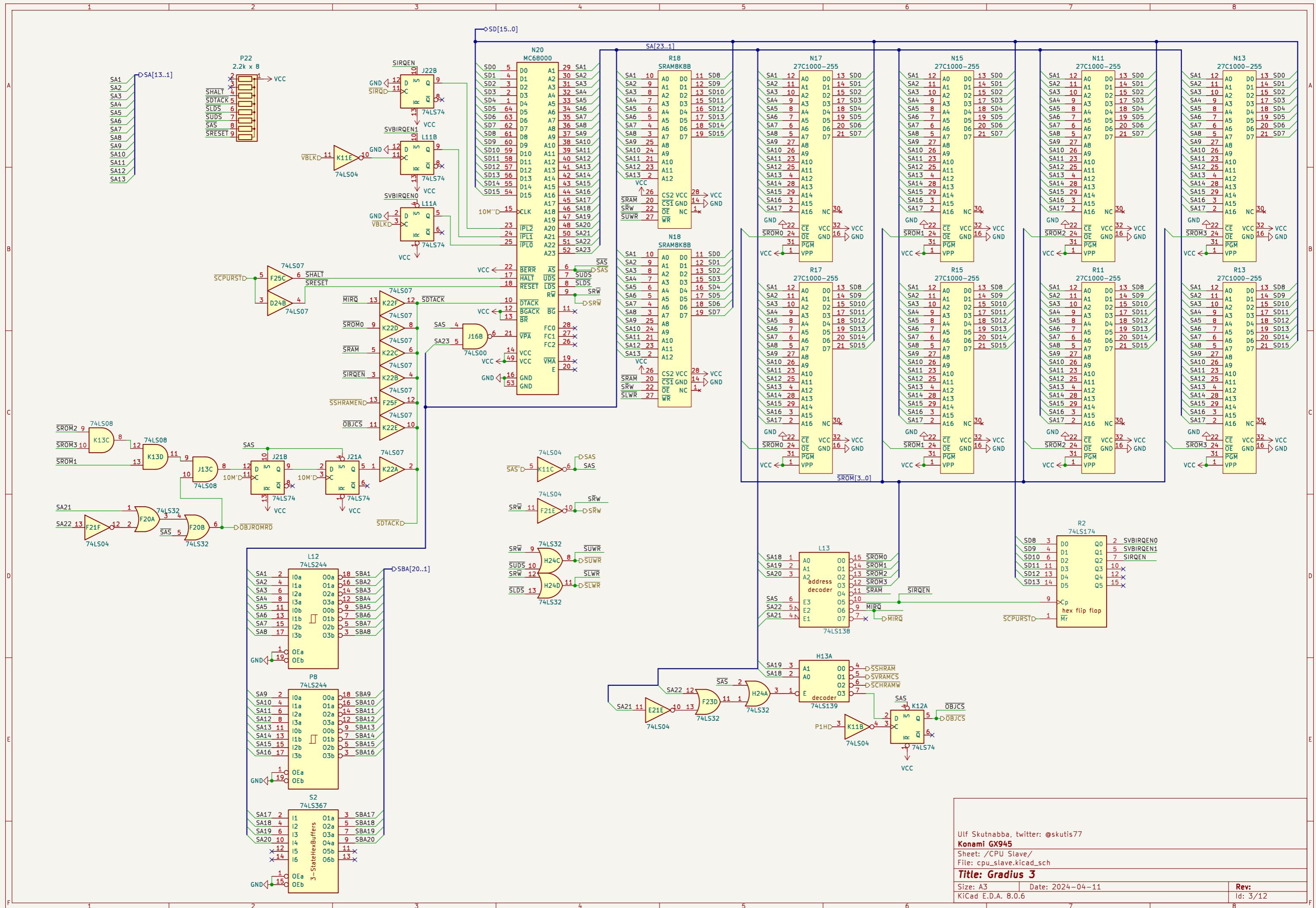
Konami GX945

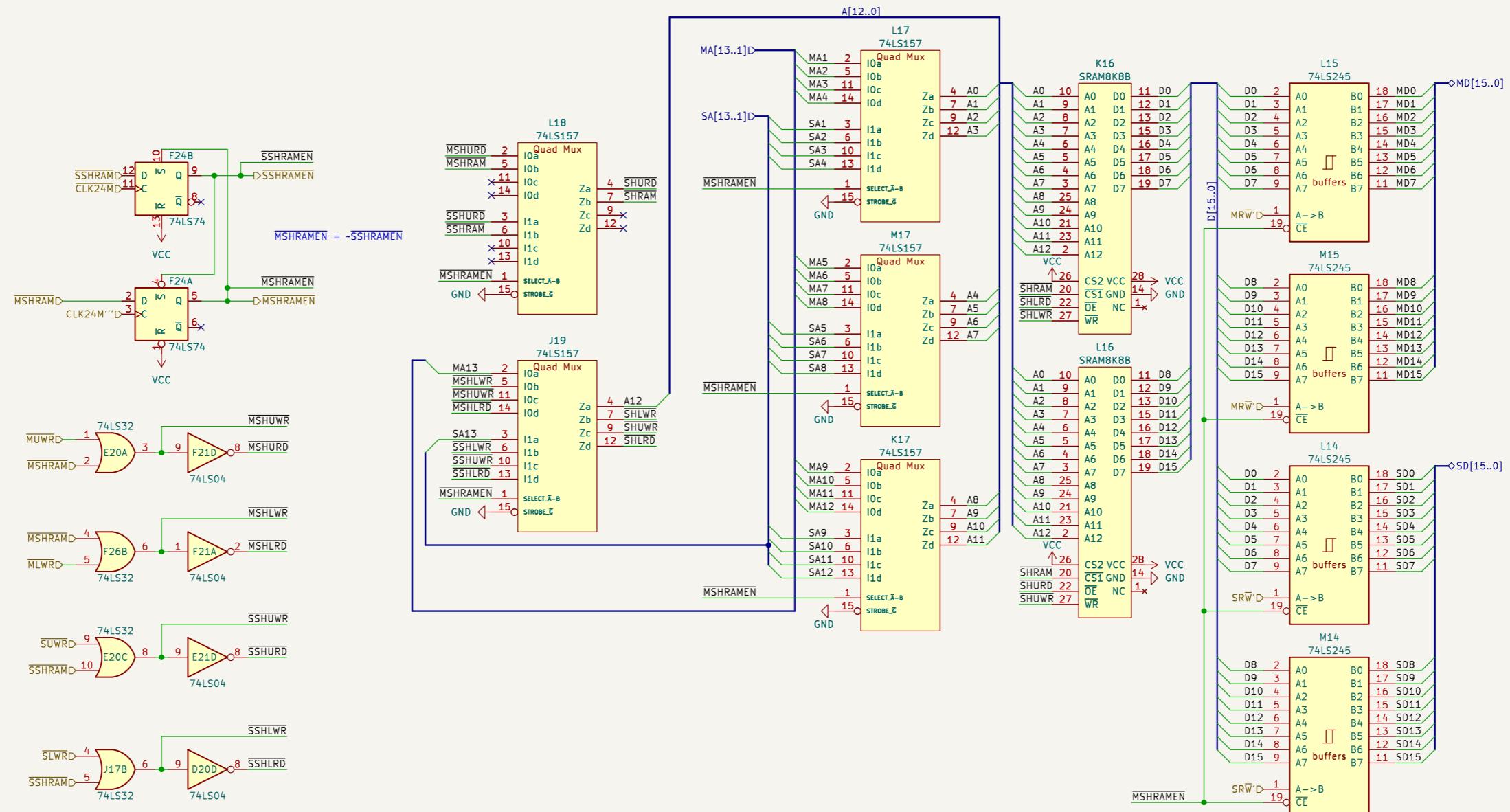
Sheet: /CPU Master/
File: cpu_master.kicad_sch

Title: Gradius 3

Size: A3 Date: 2024-04-11
KiCad E.D.A. 8.0.6

Rev: Id: 2/12





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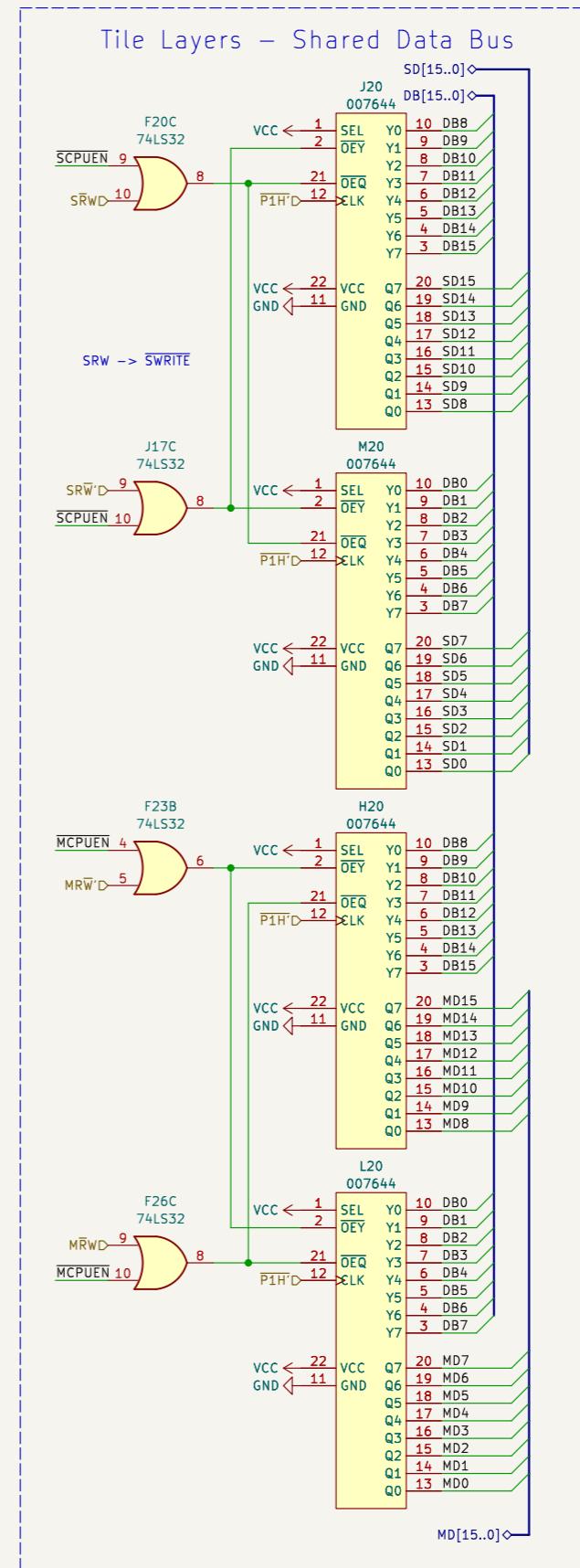
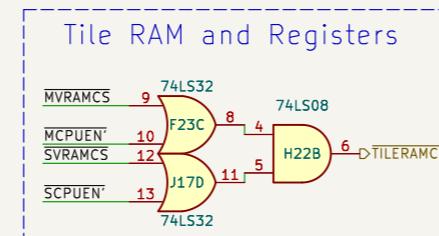
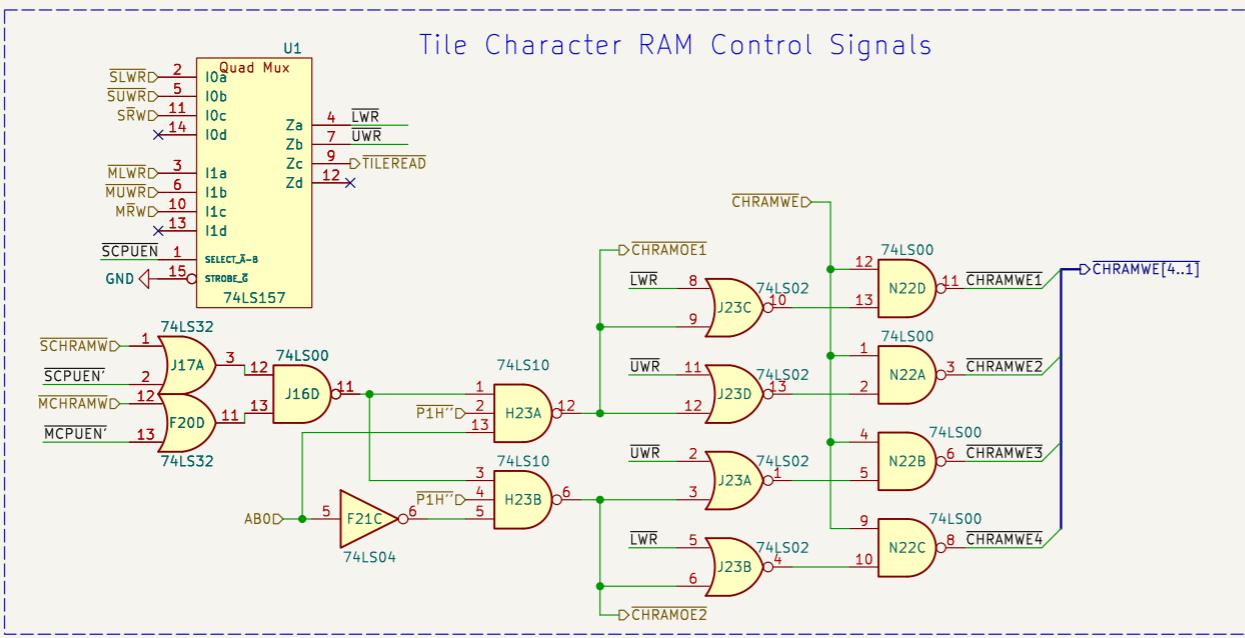
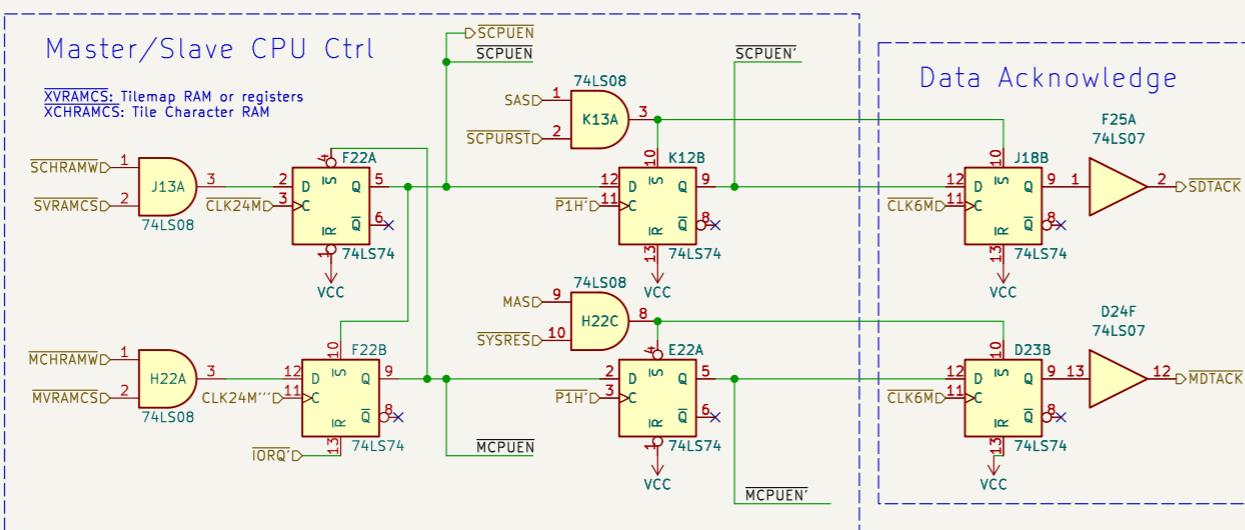
Sheet: /Shared RAM/

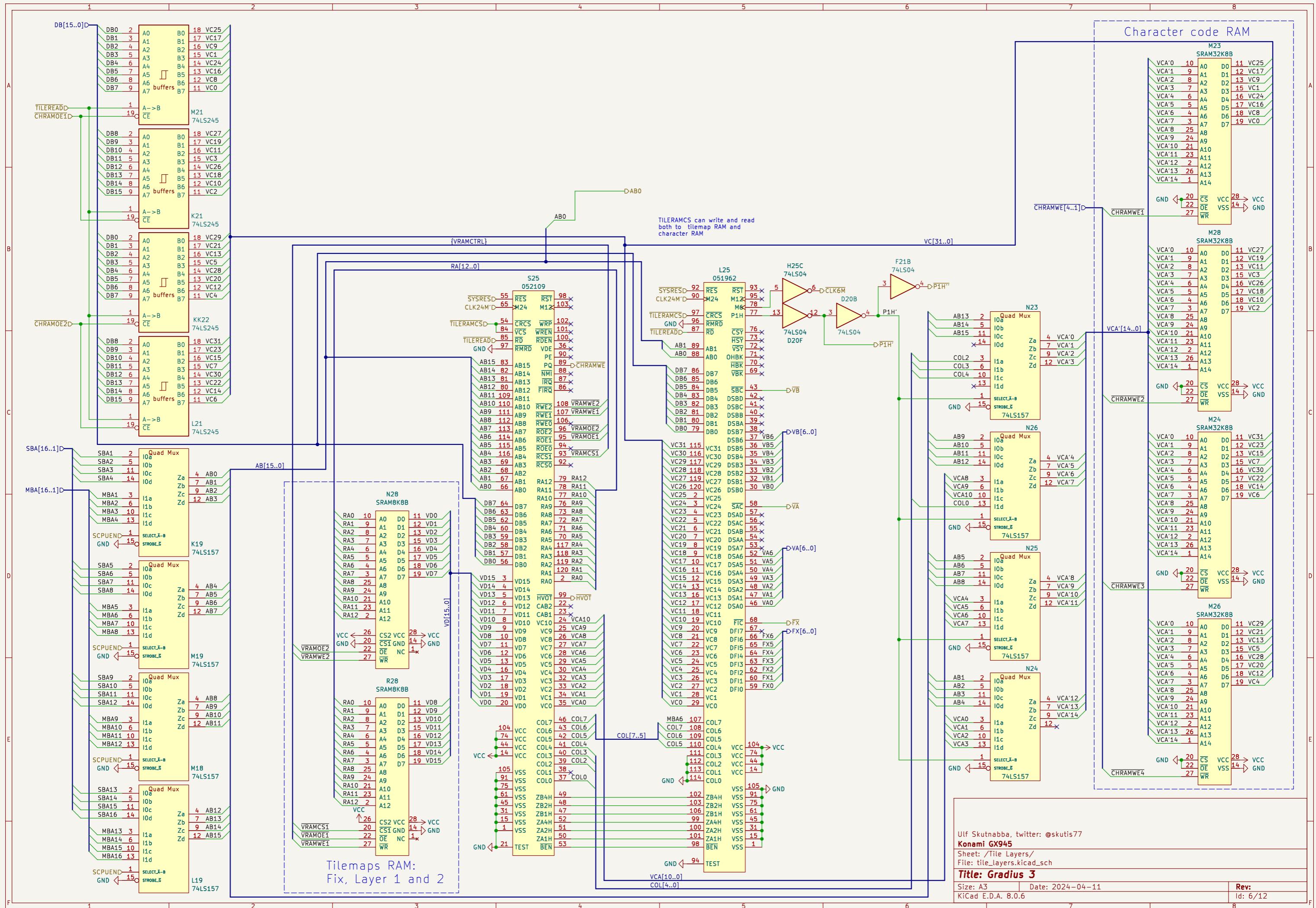
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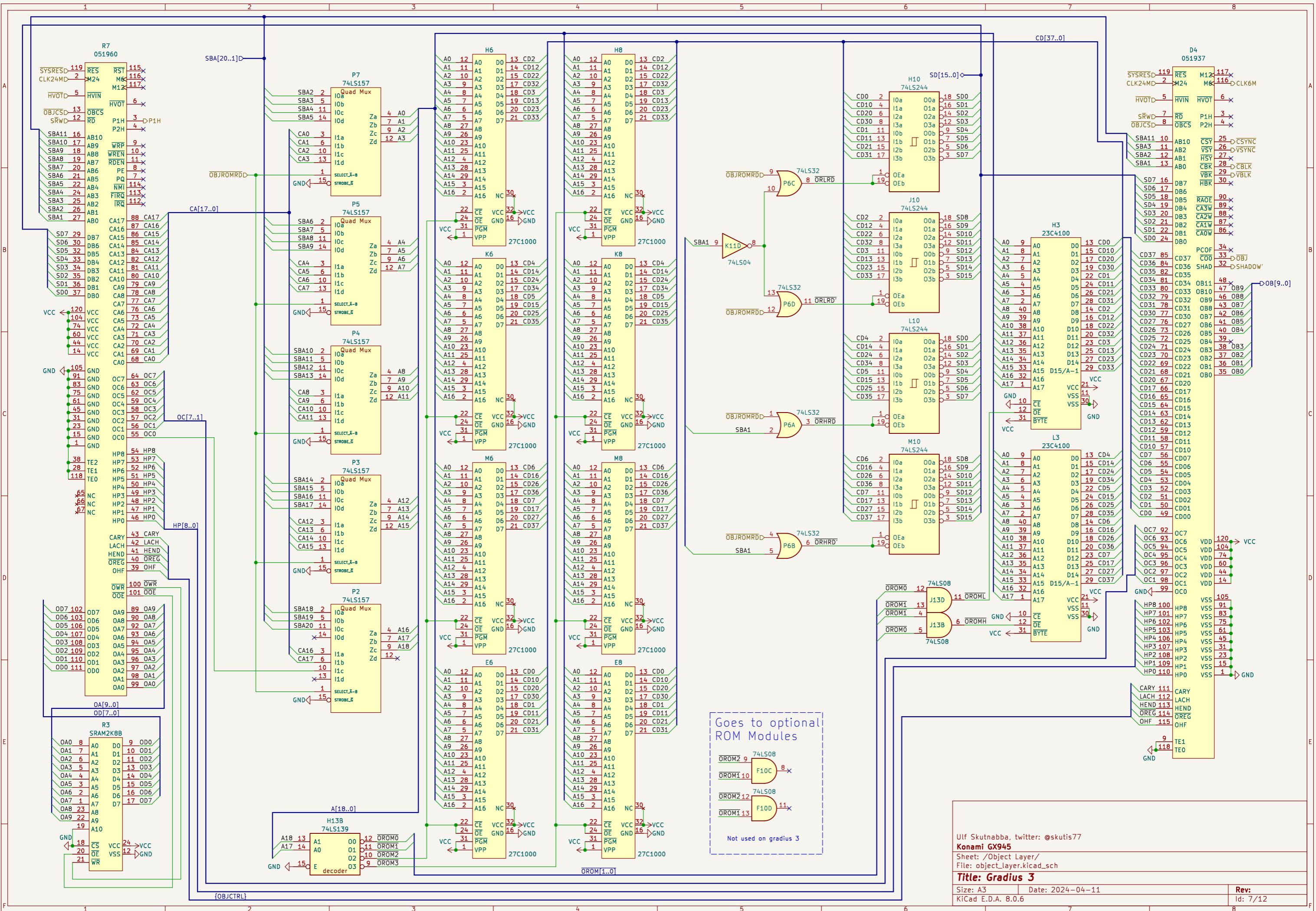
Title: *Gradius 3*

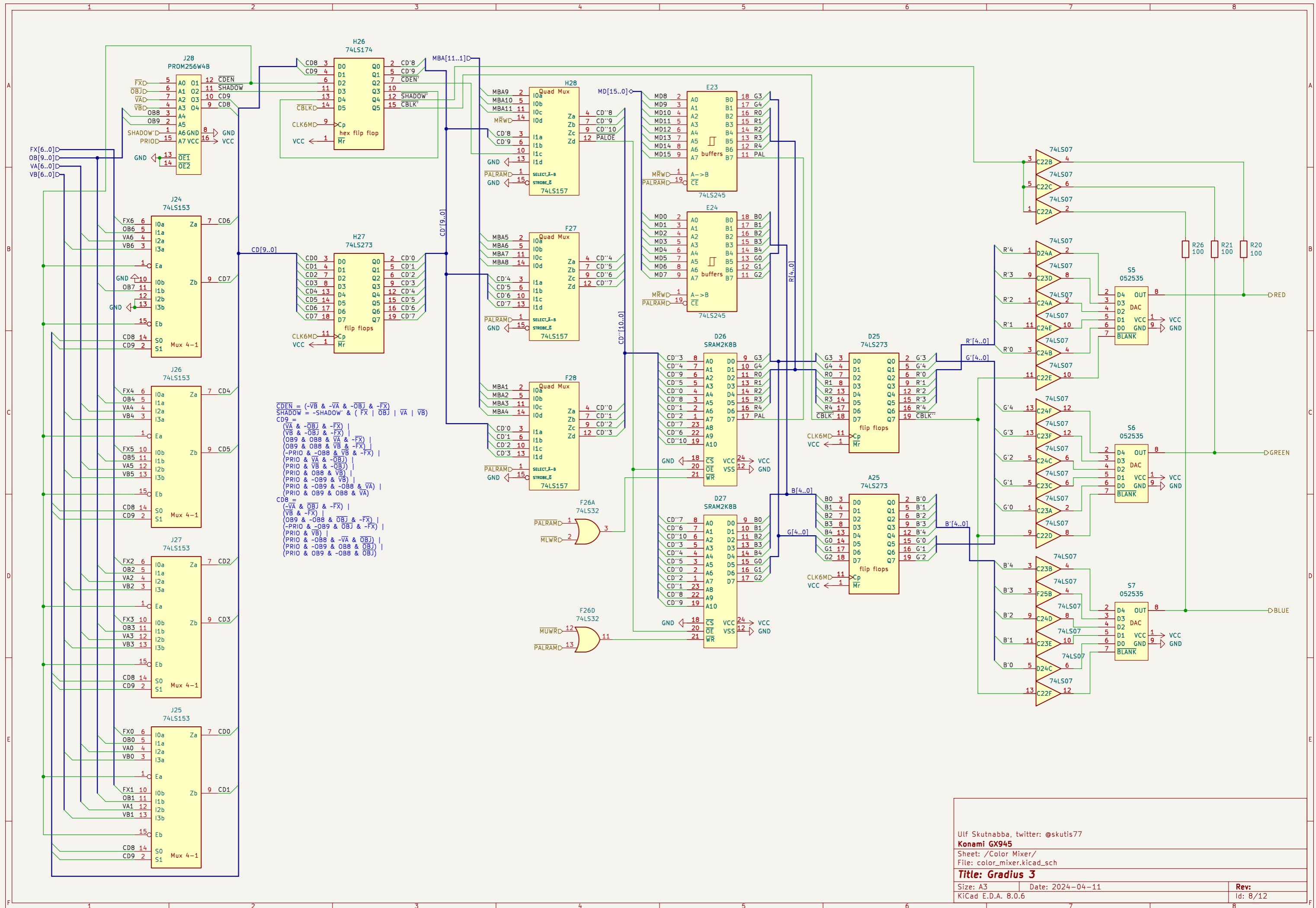
Size: A3 Date:

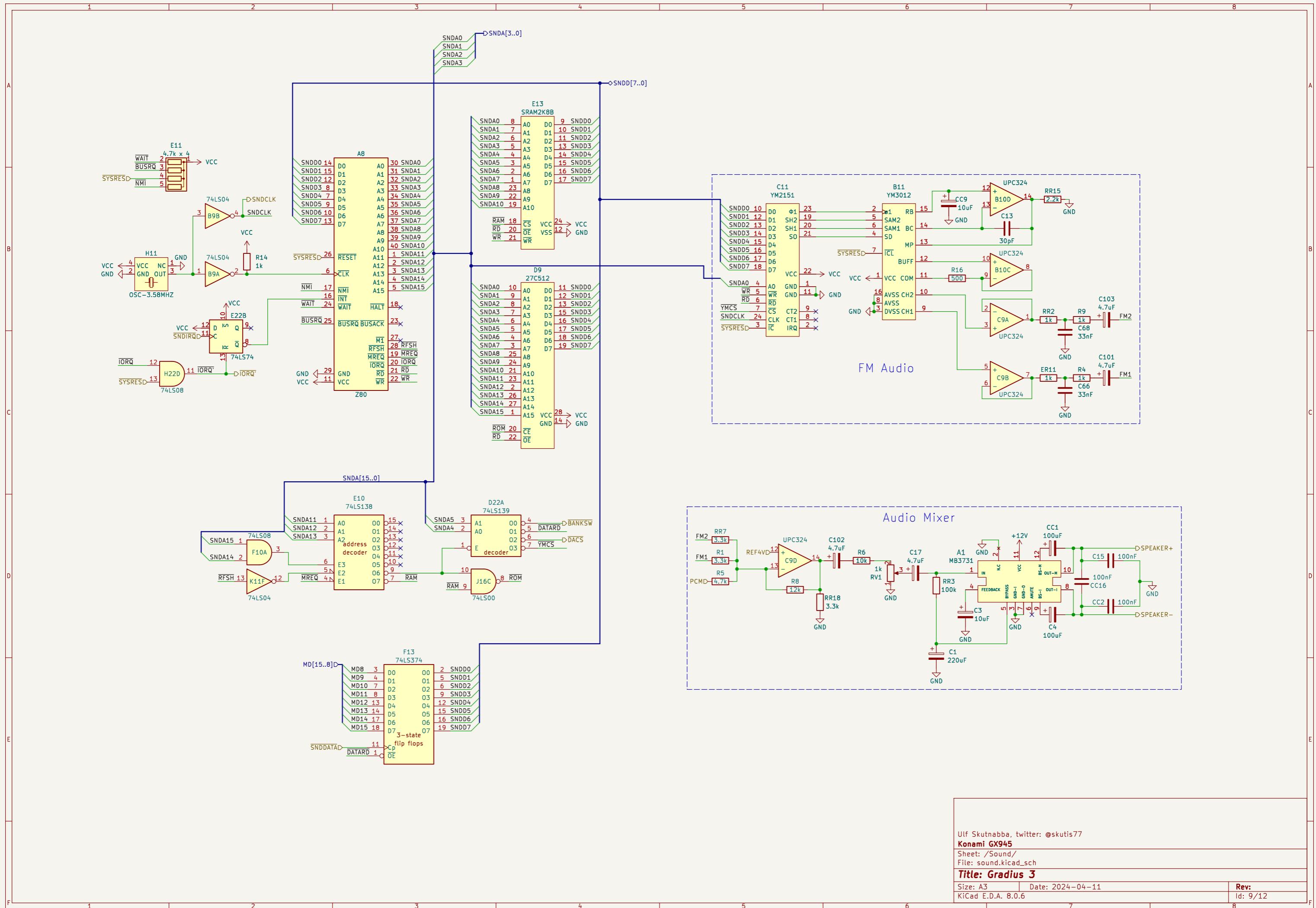
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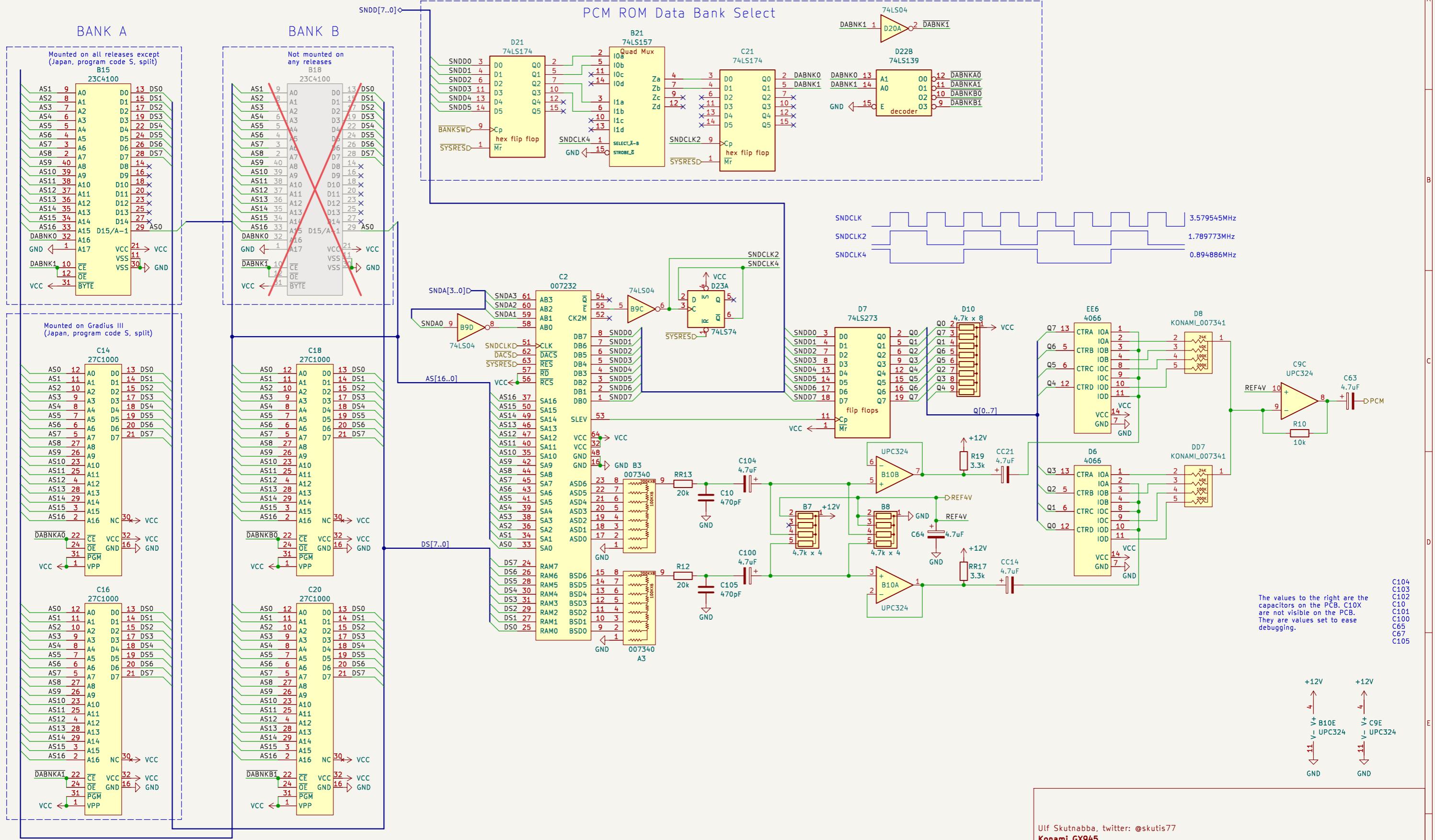








B15 and B18 do not follow the standard Mask ROM behaviour.
The BYTE mode select must be selected from factory and pin 31 is probably not connected.



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Sheet: /PCM/

File: pcm.kicad_sch

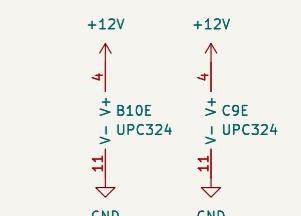
Title: Gradius 3

Size: A3 Date: 2024-04-11

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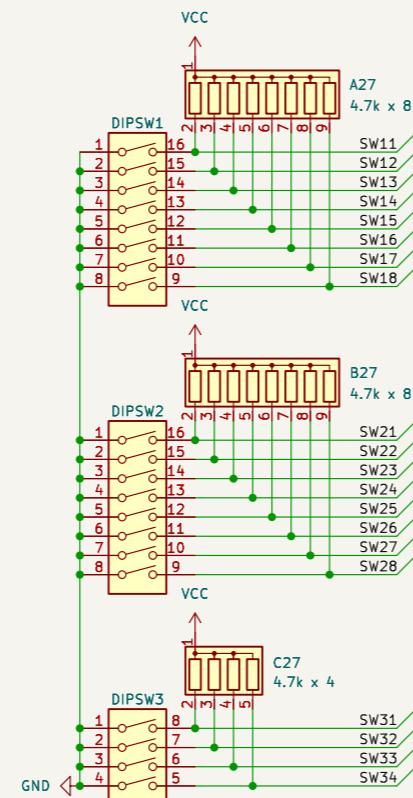
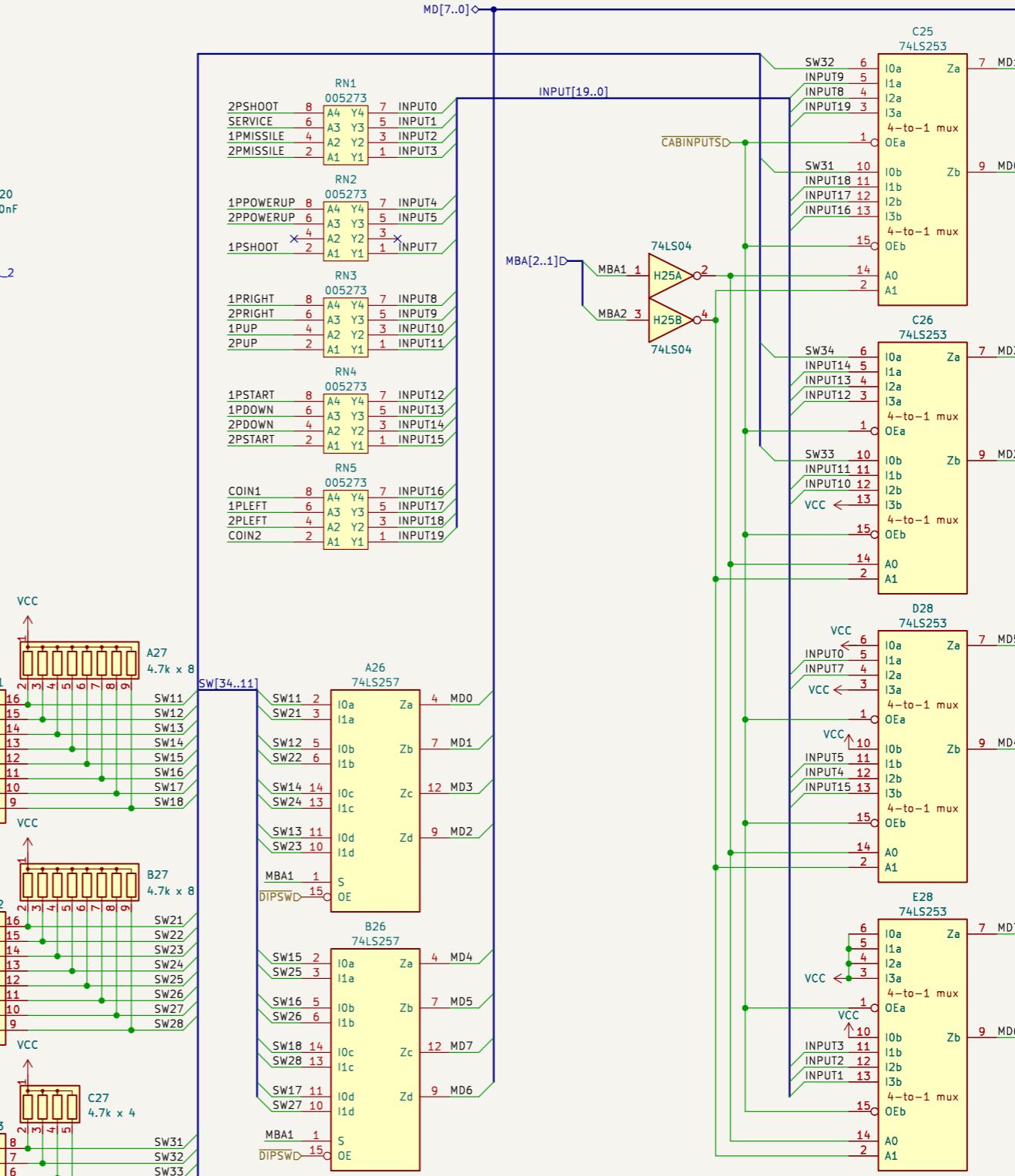
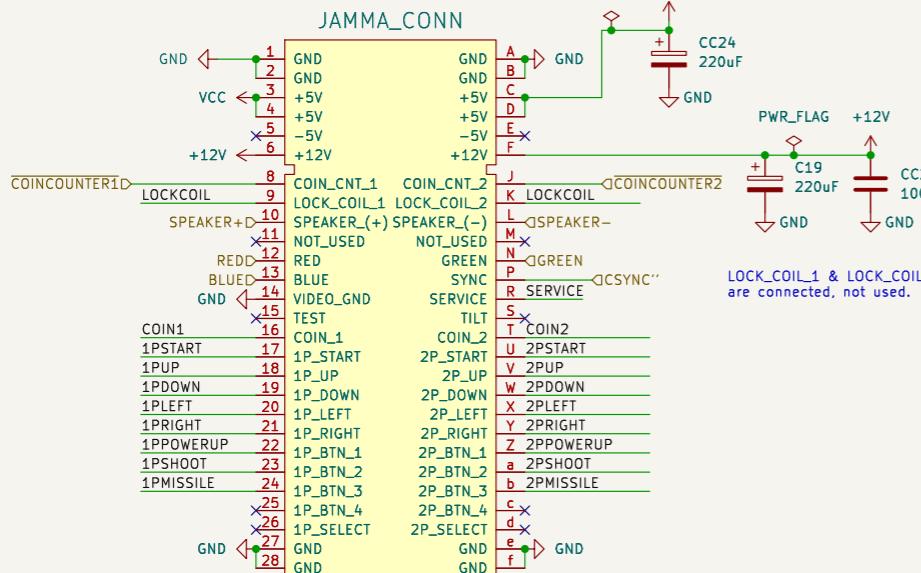
C104
C103
C102
C10
C101
C100
C65
C67
C105

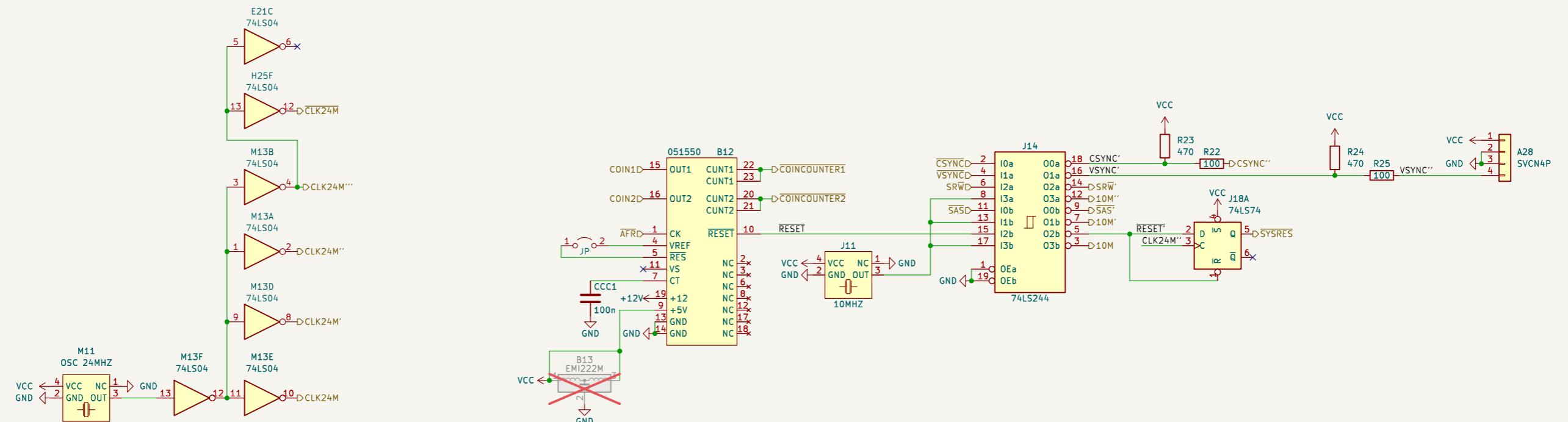
The values to the right are the capacitors on the PCB. C10X are not visible on the PCB. They are values set to ease debugging.



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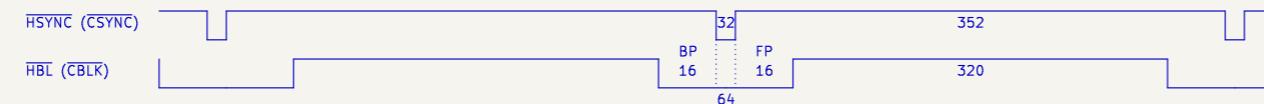
Horizontal and vertical synch timing diagrams

The pixel clock is derived from the 24MHz oscillator.
Pixel clock OVCK: $f = 24\text{MHz} / 4 = 6\text{MHz}$

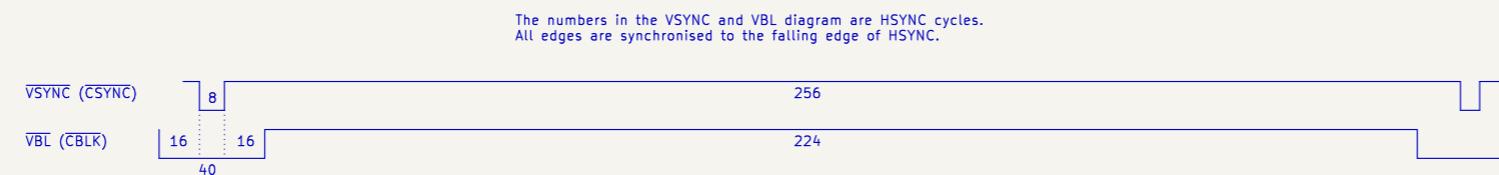
The numbers in the HSYNC and HBL diagram are pixel clock cycles.
All edges are synchronised to the rising edge of the pixel clock.

The signals have been measured at the output of the
graphic chips.

If horizontal blanking is measured at the RGB DACs, the blanking
is delayed 2 pixel clocks relative to composite sync. This
gives BP = 14 and FP = 18.



HSYNC and HBL
Frequency $f = 6\text{MHz} / 384 = 15.625\text{kHz}$.
Period $T = 1/f = 64\text{us}$.



VSYNC and VBL:
Frequency $f = 15.625\text{kHz} / 264 = 59.1856\text{Hz}$
Period $T = 1/f = 1 / 59.1856\text{Hz} = 16.896\text{ms}$

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Sheet: /Misc/

File: misc.kicad_sch

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