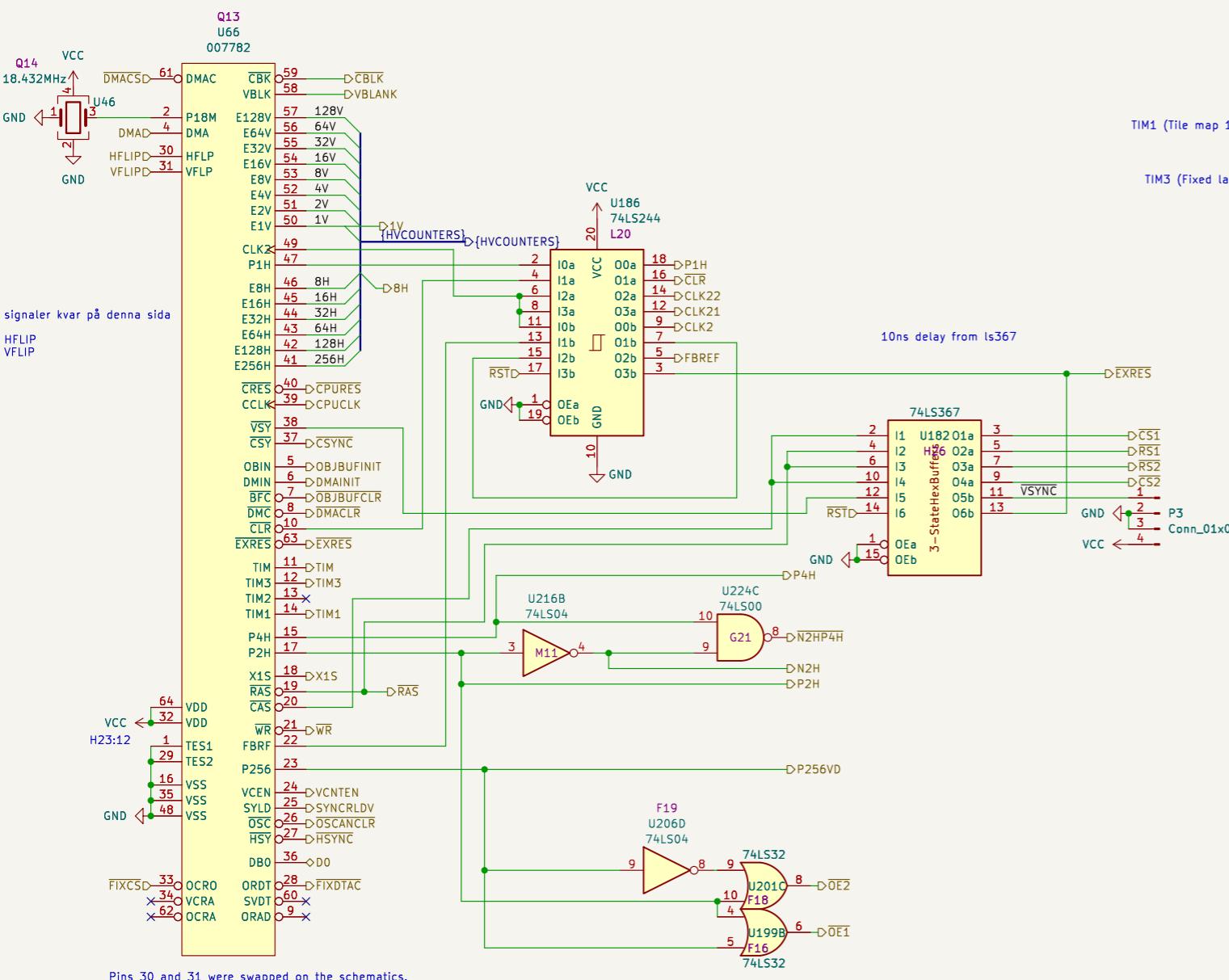
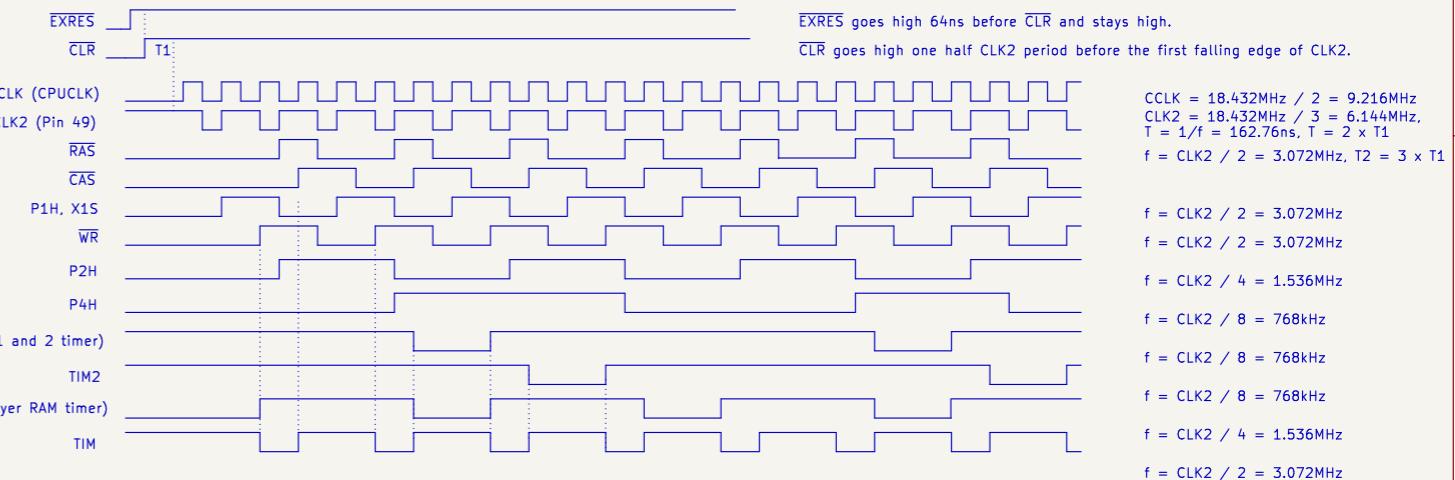
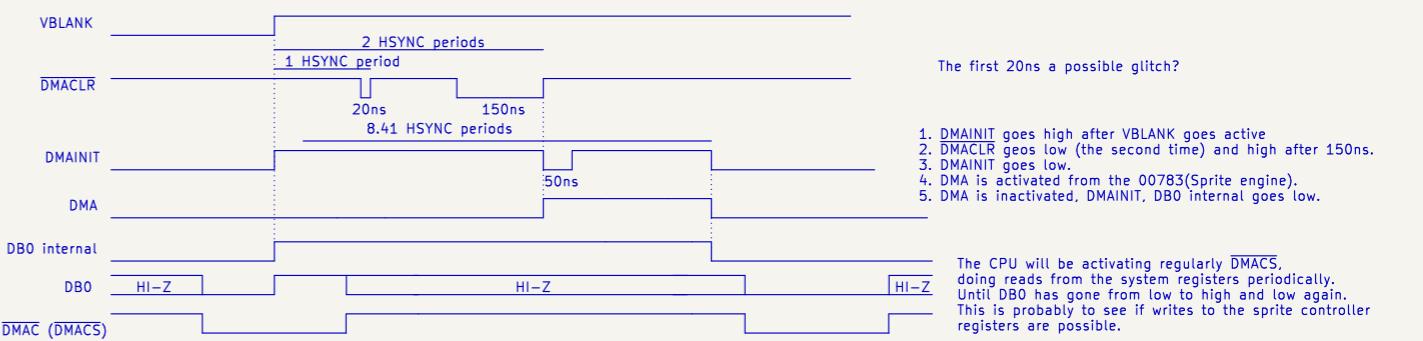
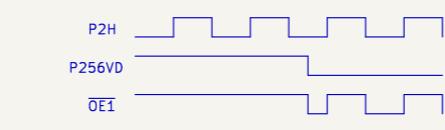


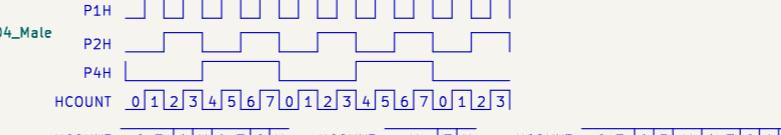
DMA Synchronization



Output enables active vs. part of frame buffer active



Chip select signals and Data Acknowledge signals



Timing

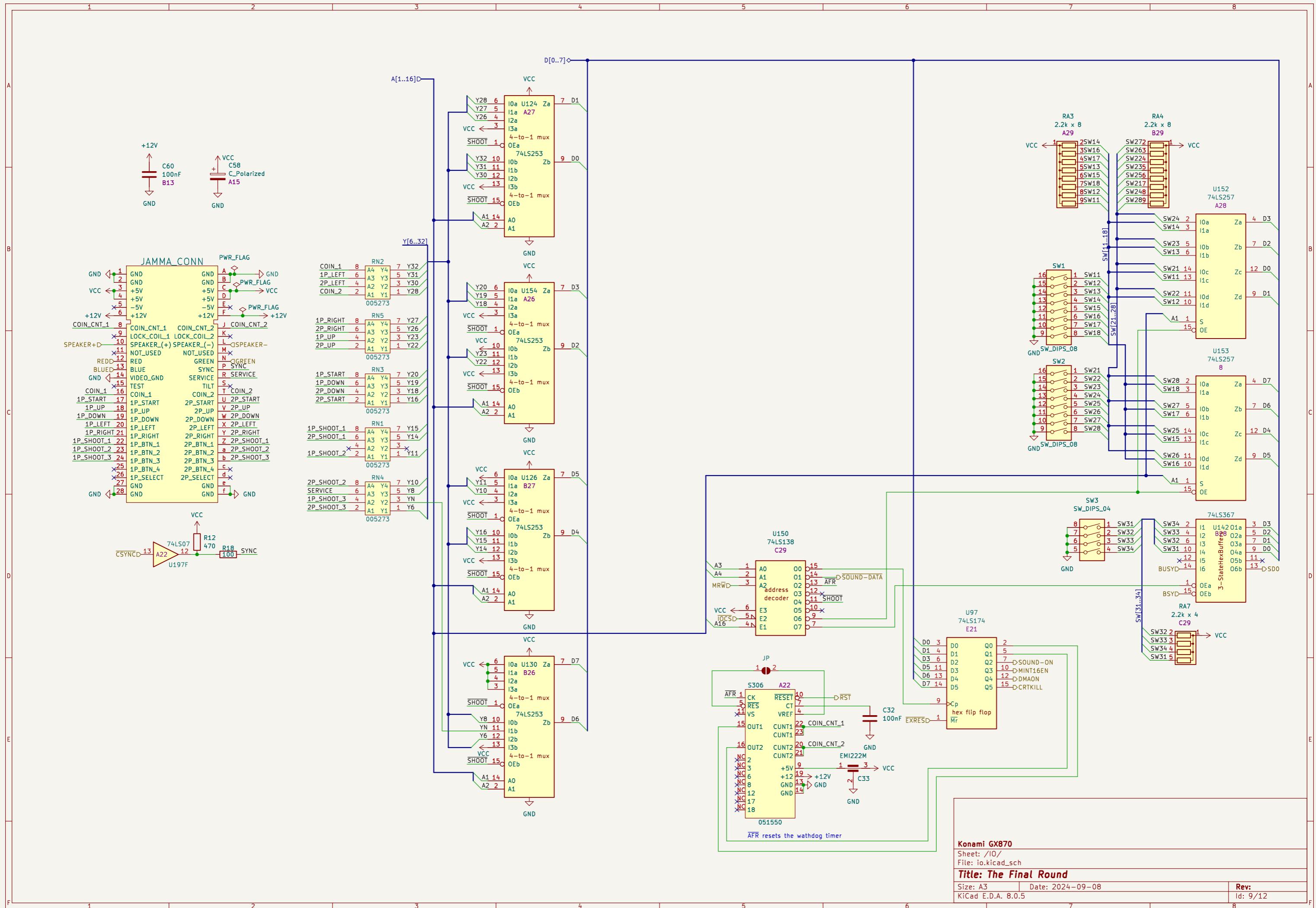
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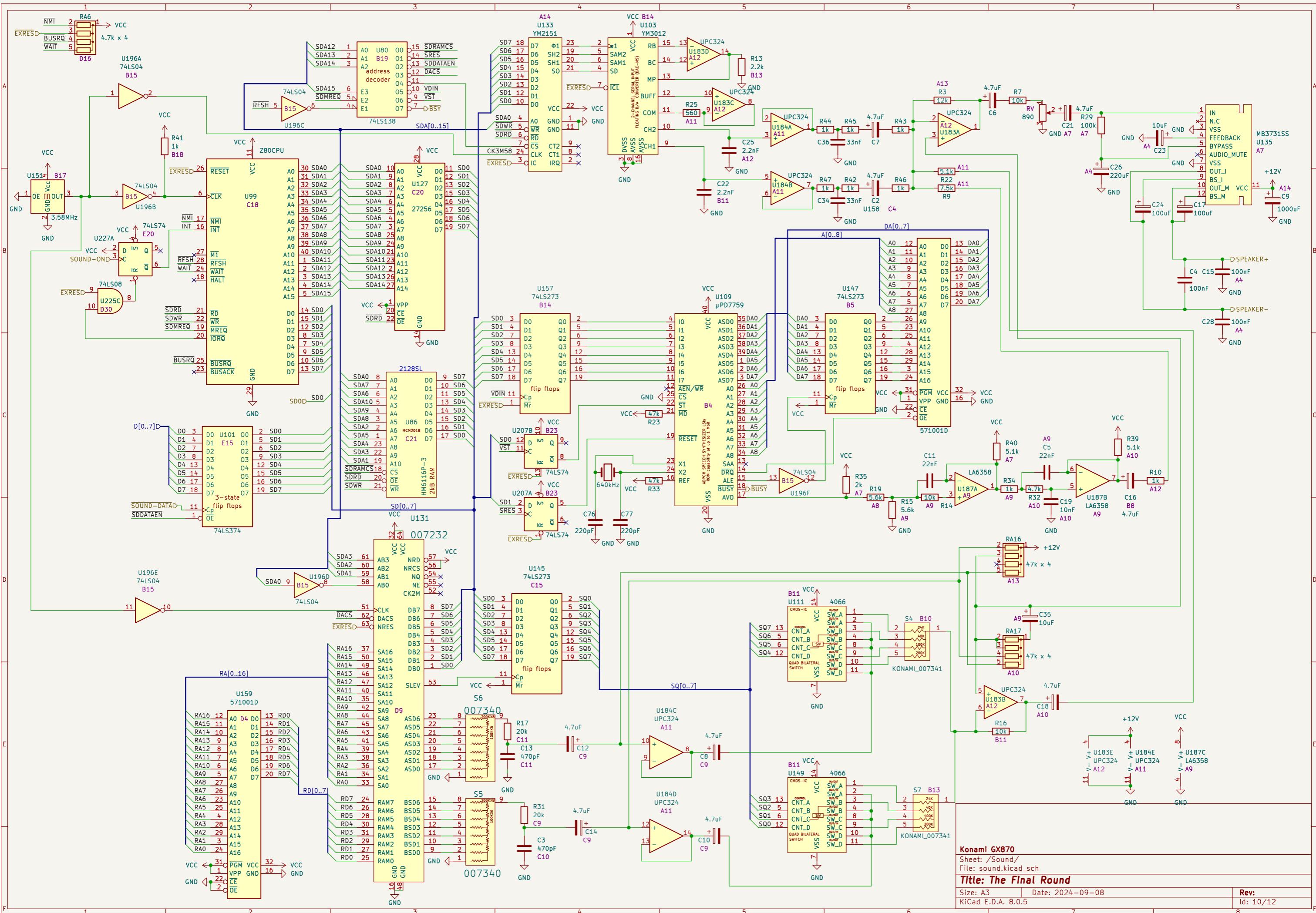
Sheet: /Timing/
File: timing.kicad_sch

Title: The Final Round

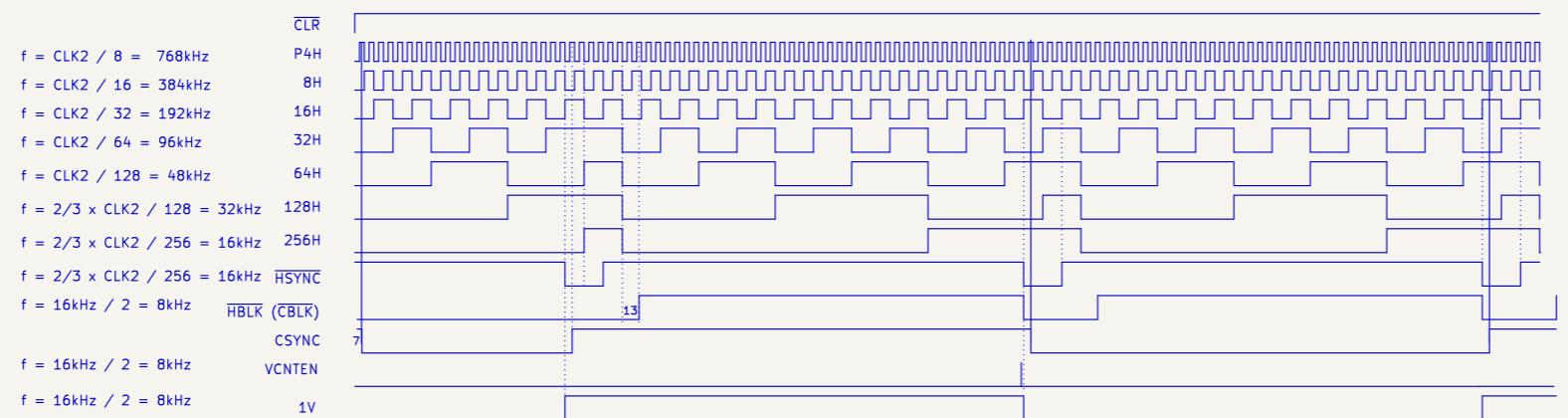
Size: A3 | Date: 2024-09-08
KiCad E.D.A. 8.0.5

Rev:
Id: 8/12



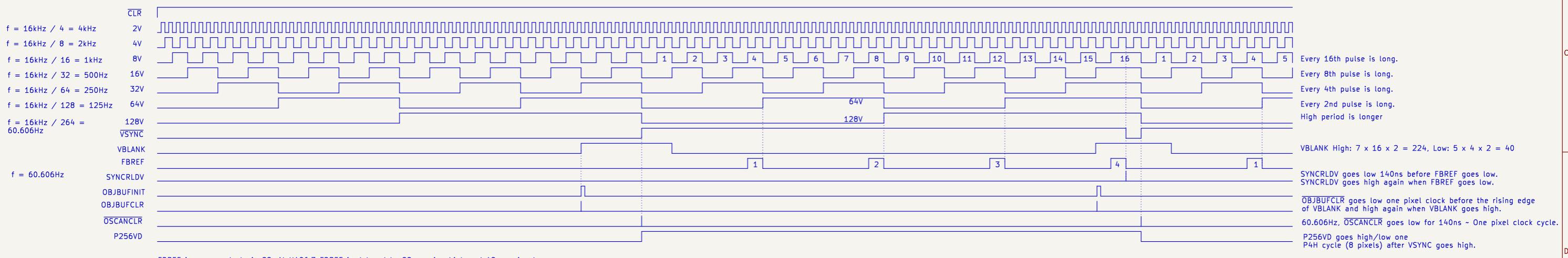
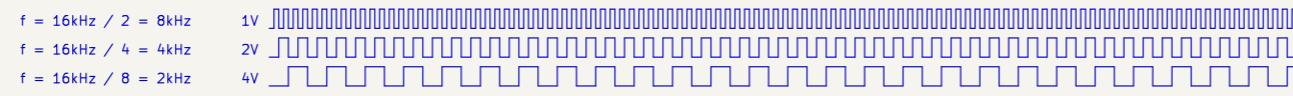


Horizontal signals



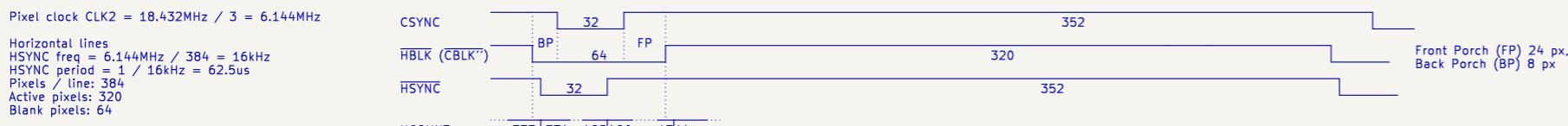
The first HSYNC is at HCOUNT 175 after reset.

Vertical signals

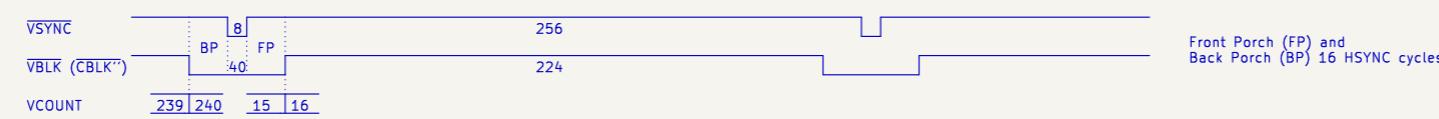


Horizontal and vertical synch timing diagrams

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.
All edges are synchronised to the rising edge of CLK2.



The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.
All edges are synchronised to the falling edge of HSYNC.



HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK^{''} is at the output of color mixer.

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Sheet: /Timing diagrams/
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A

B

C

D

E

F

A

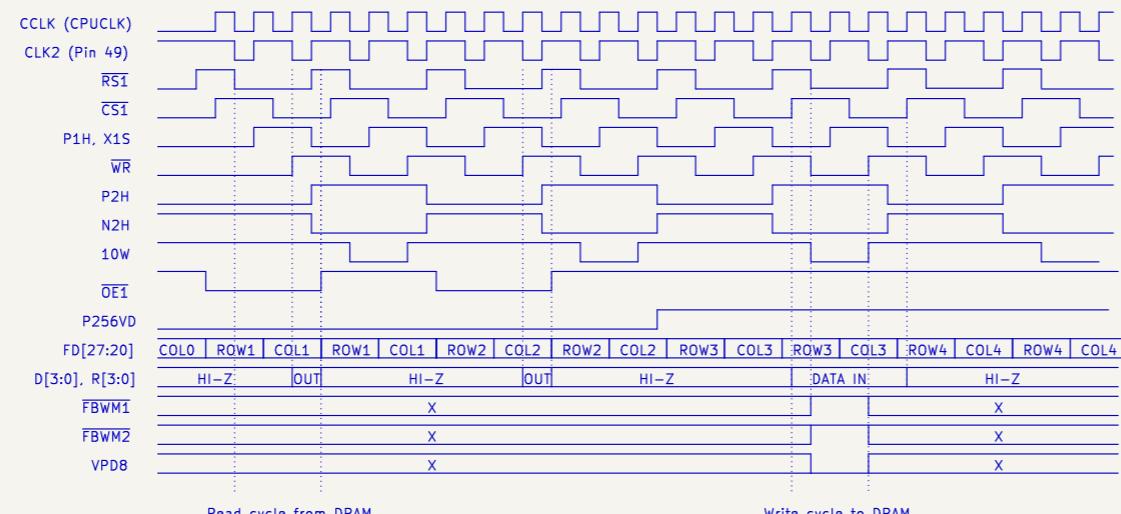
B

C

D

E

F

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Sheet: /Sprite timing diagrams/
File: sprite_timing_diagrams.kicad_sch

Title: The Final Round

Size: A3 | Date: 2024-09-08
KiCad E.D.A. 8.0.5

Rev: | Id: 12/12