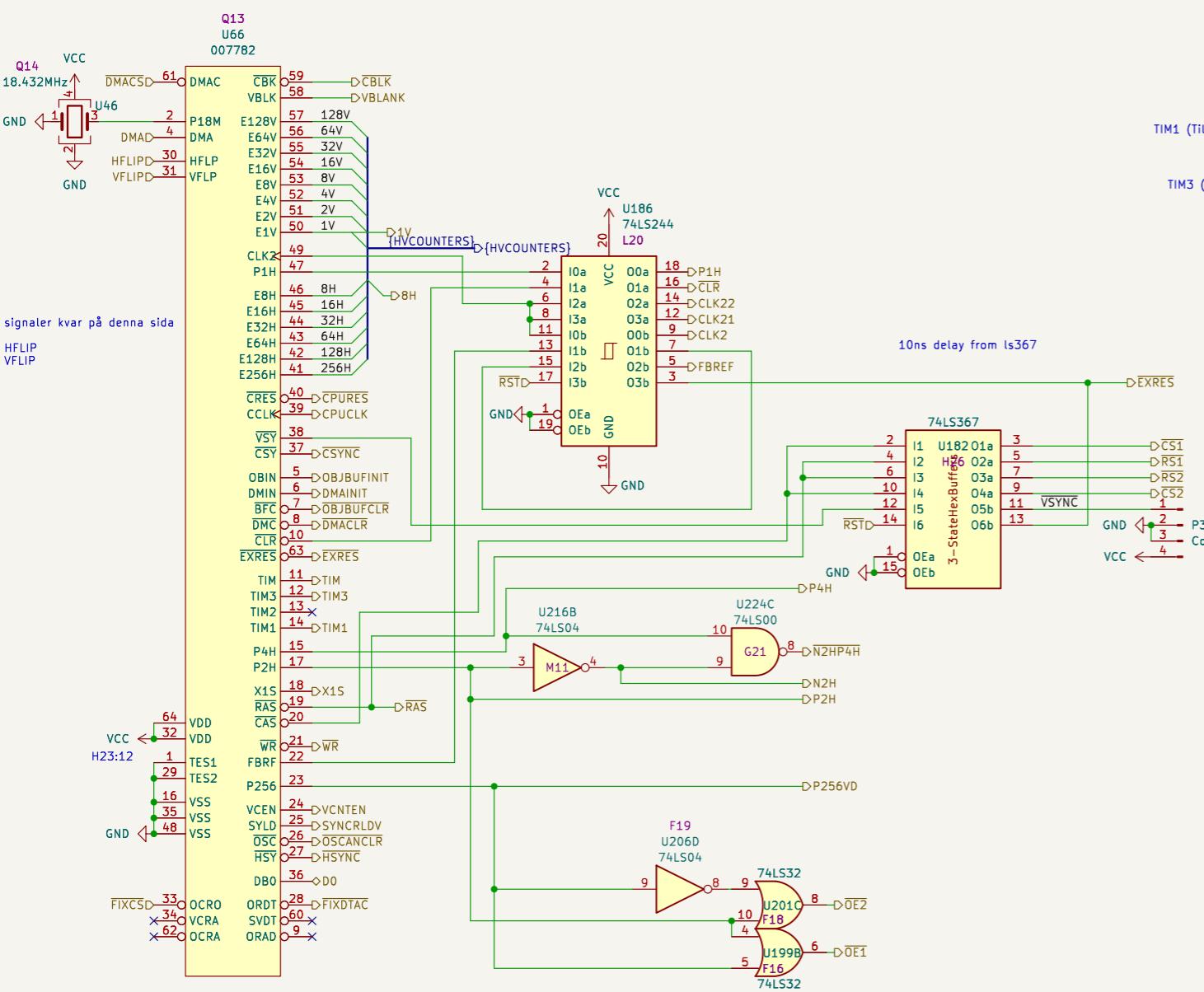
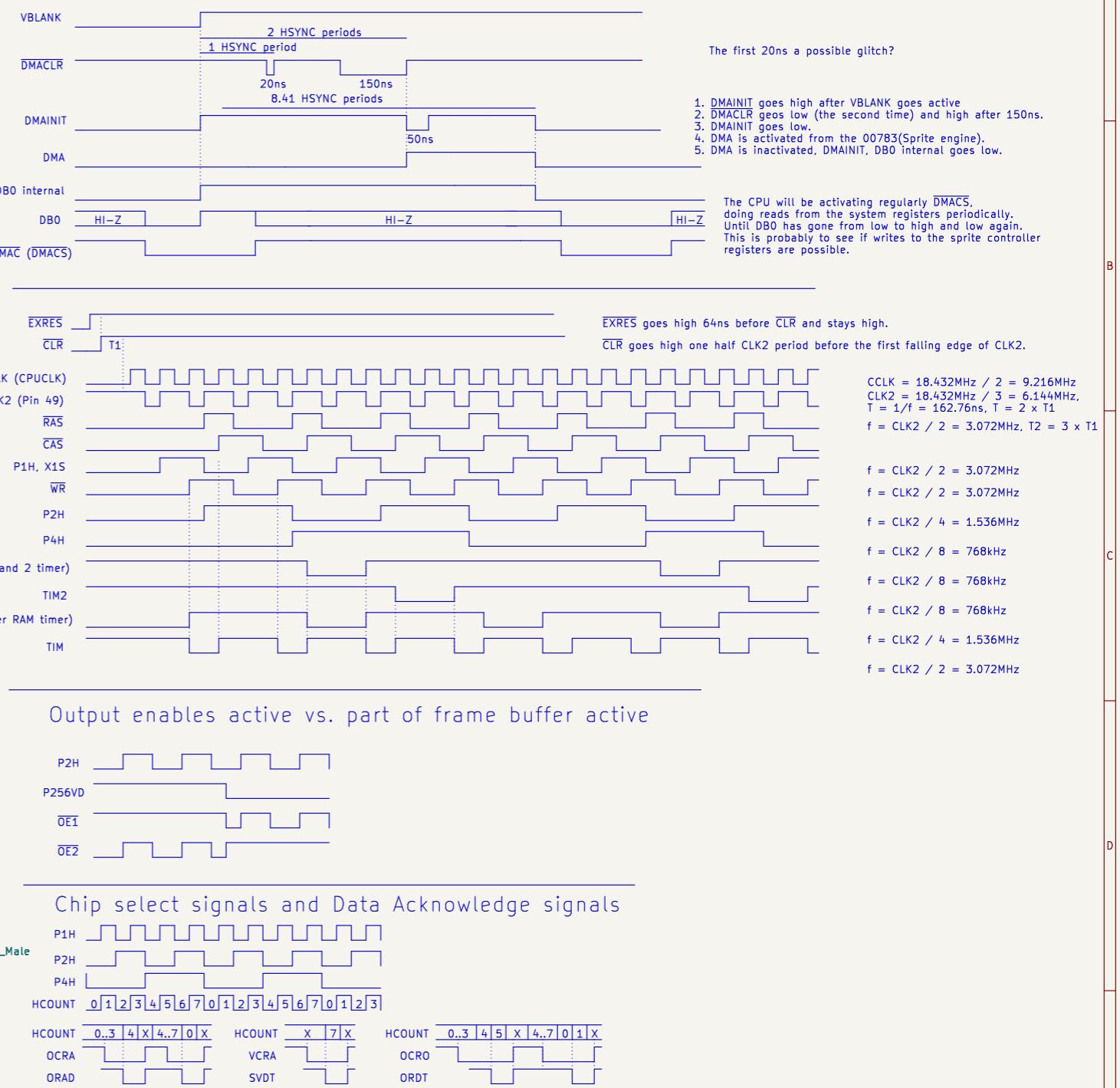


## DMA Synchronization



Pins 30 and 31 were swapped on the schematics.

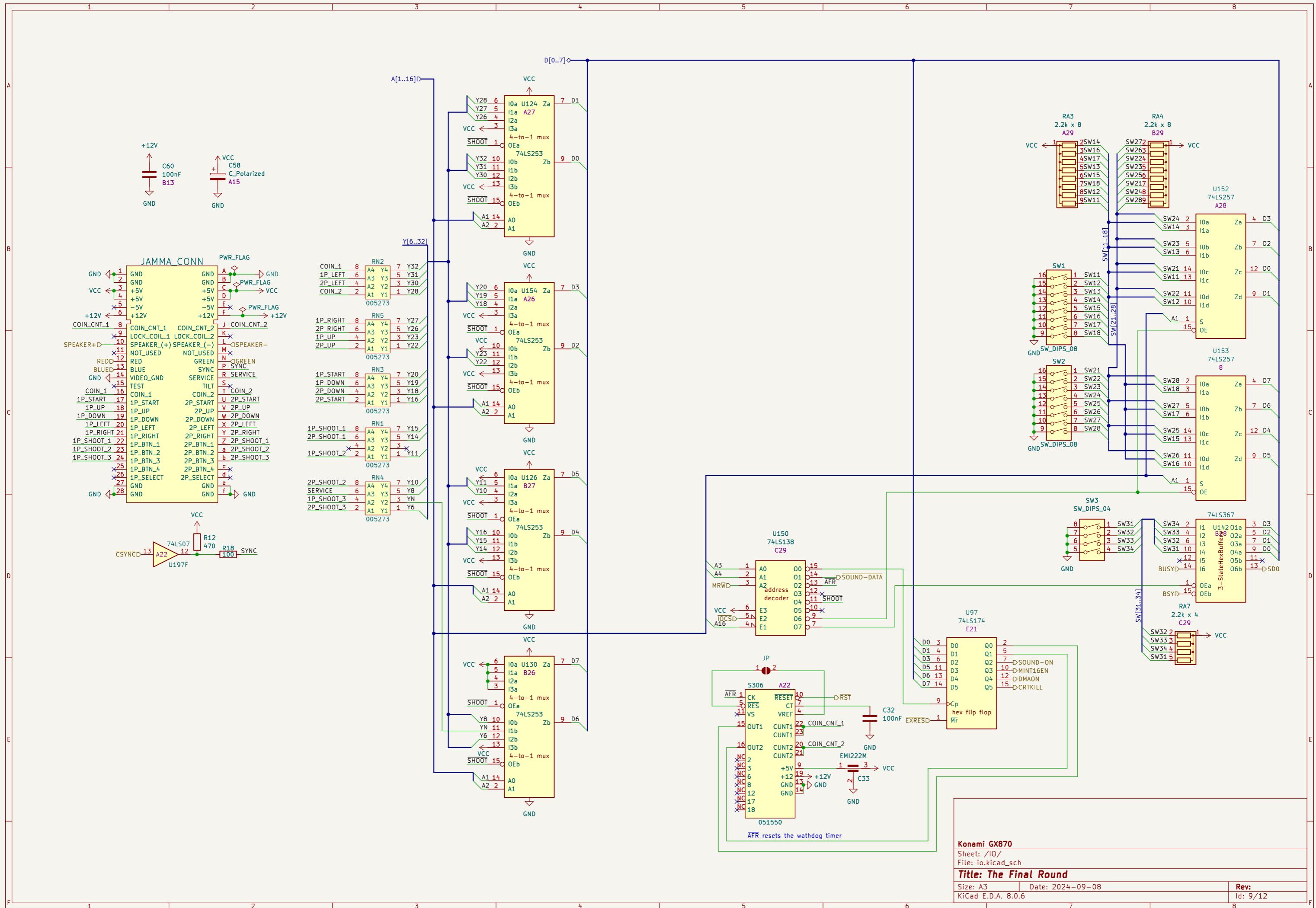


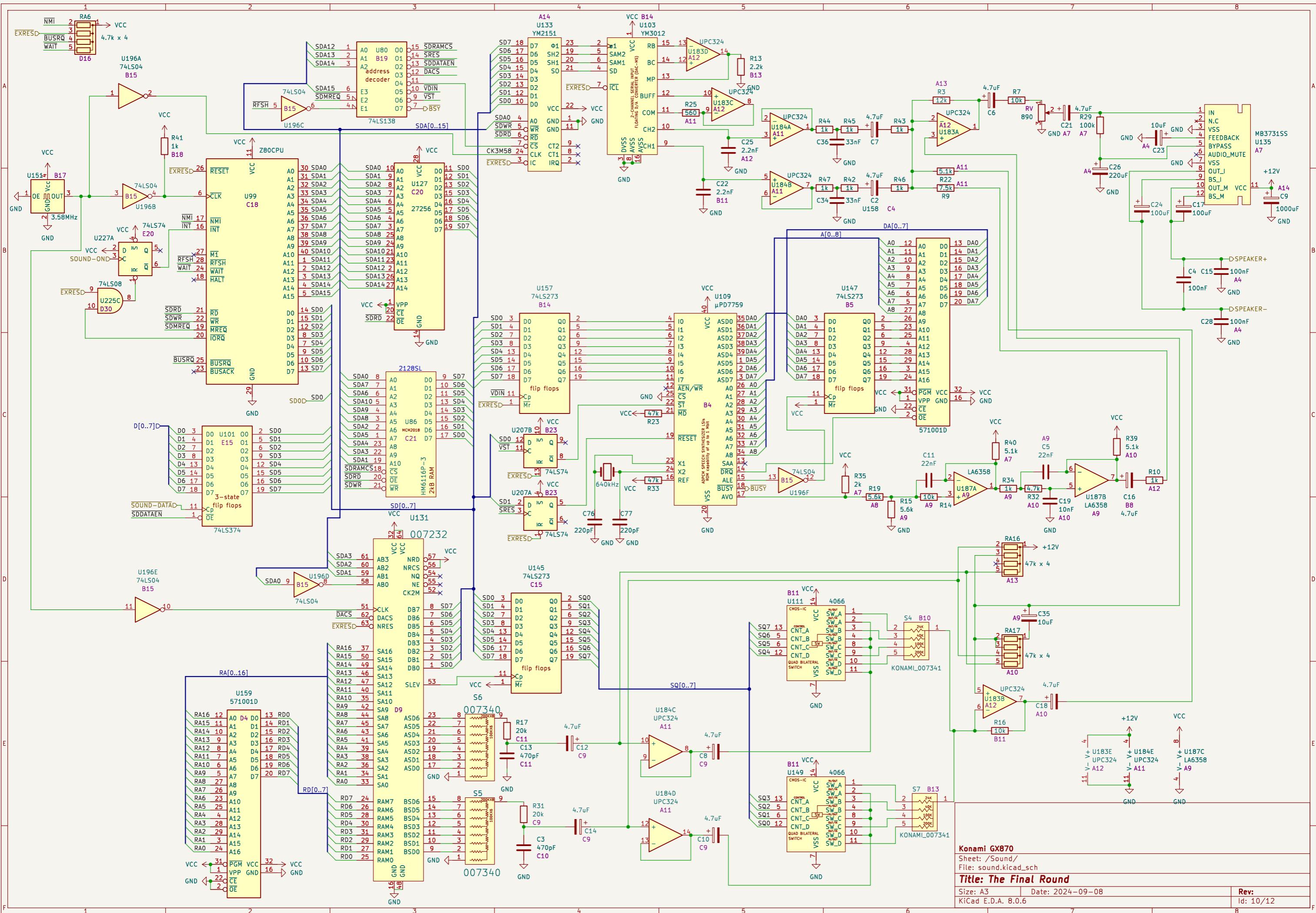
Timing  
**Konami GX870**  
Sheet: /Timing.  
File: timing.kicd

## Title: The Final Round

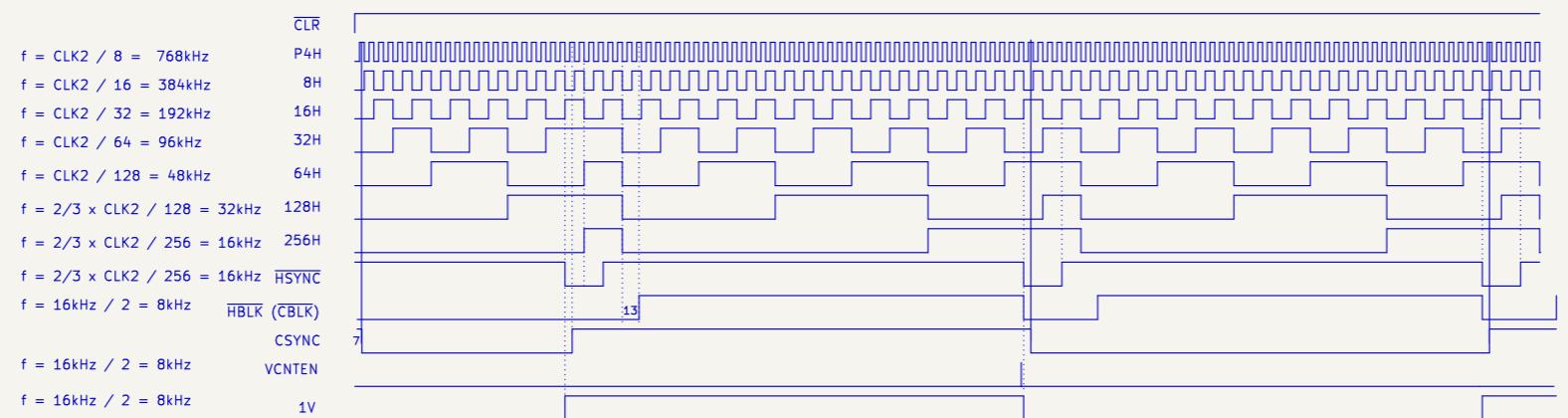
Size: A3 Date: 2024-09-08  
KiCad E.D.A. 8.0.6

Rev:  
Id: 8/12





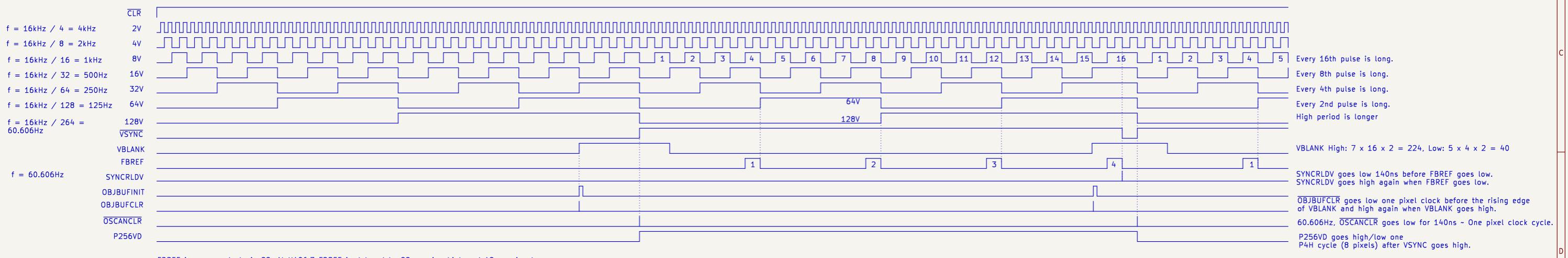
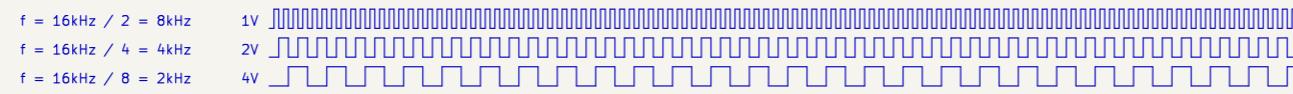
## Horizontal signals



- The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

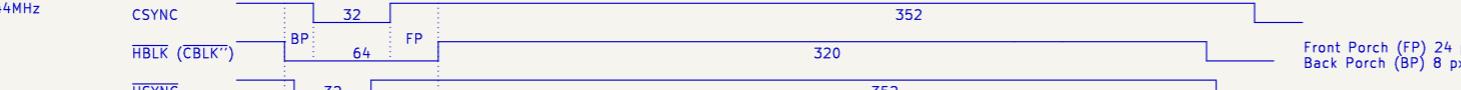
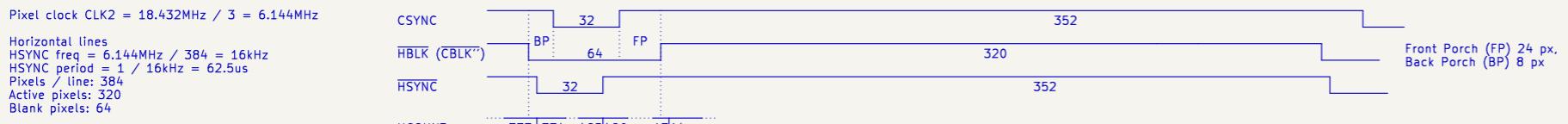
- CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals

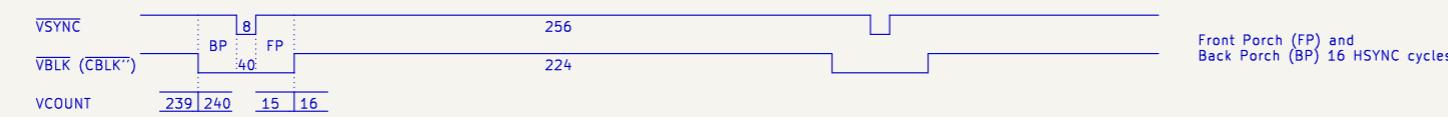


## Horizontal and vertical synch timing diagrams

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.  
All edges are synchronised to the rising edge of CLK2.



The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.  
All edges are synchronised to the falling edge of HSYNC.



Front Porch (FP) and  
Back Porch (BP) 16 HSYNC cycles.

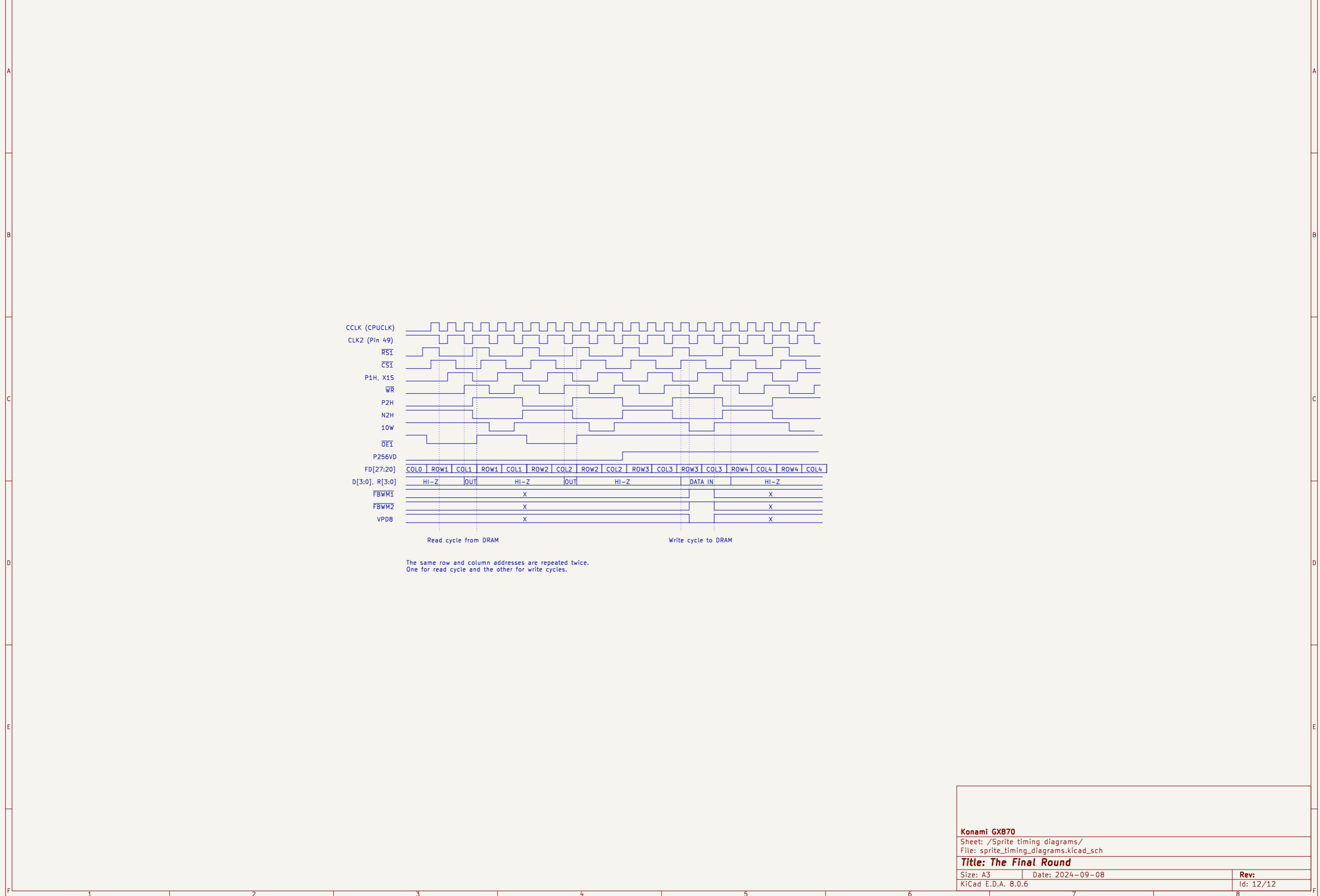
### Konami GX870

Sheet: /Timing diagrams/  
File: timing\_diagrams.kicad\_sch

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