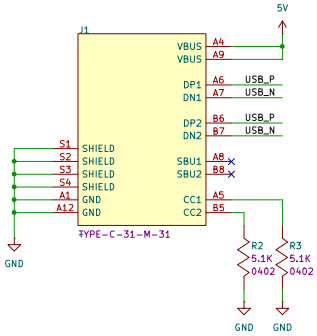
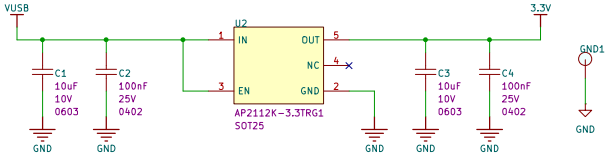
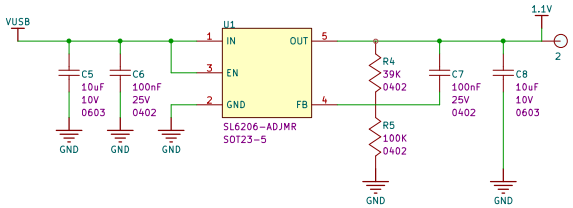
INPUT POWER



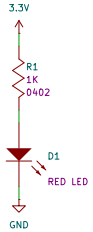
LDO 5V TO 3.3V



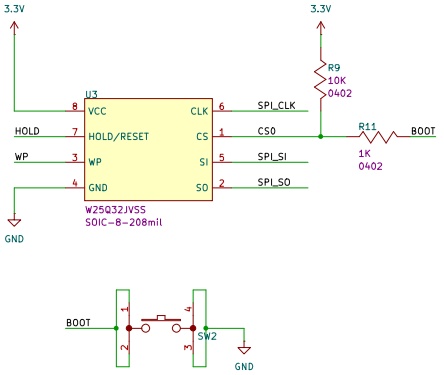
LDO 5V TO 1.1V



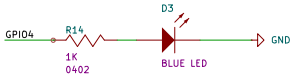
POWER LED

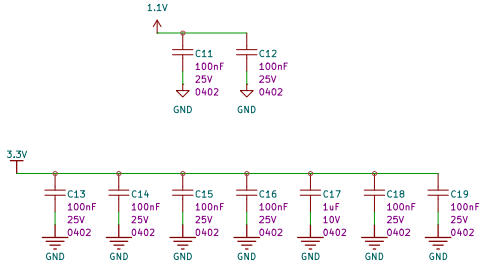


SPI Flash

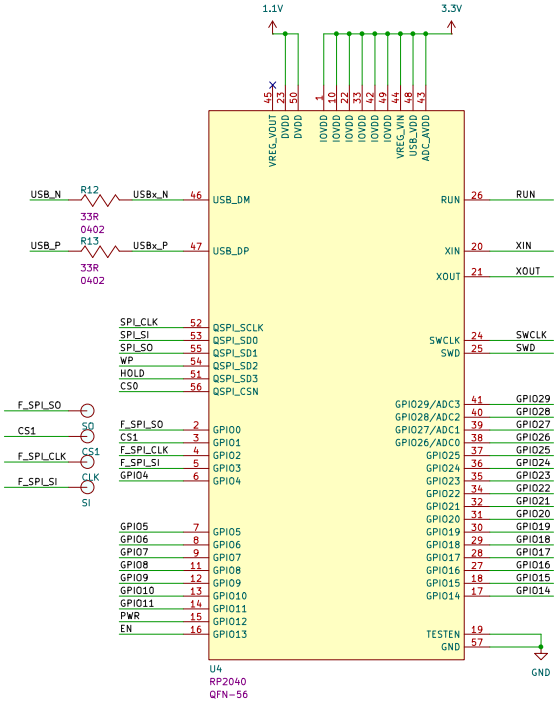


Status LED(RP2040)

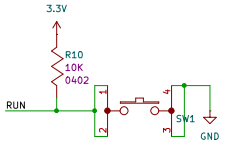




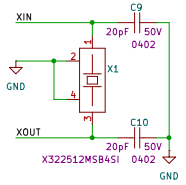
RP2040



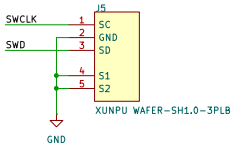
RESET BUTTON



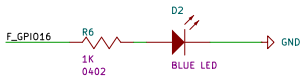
OSCILLATOR



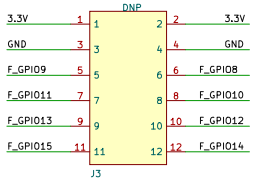
JST Debug Connector



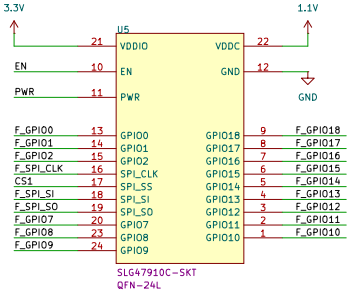
Status LED(FPGA)

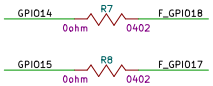


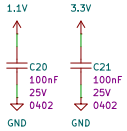
PMOD



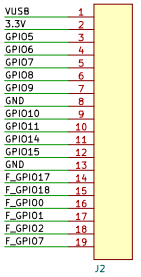
FPGA SLG47910

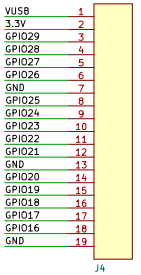






GPIO PINS





Configuration of Enable and Power Reset of FPGA

GPIO12 of RP2040 is connected to PWR

GPIO13 of RP2040 is connected to EN

PWR (nRST)	EN (nSLEEP)	Description
0	X	**Device Reset/Off State:** • Configuration of FPGA Core is not retained, and Array Power is gated • PLL, OSC, and OTP memory are disabled • BRAM data is not retained unless BRAM Keep Register value at Reset = 1 (see Reg [193] in Appendix: Register Definitions) • GPIO in Hi-Z state and not retained unless REG_GPIO_KEEP = 1.
1	0	**Lower Power/Retention State:** • Configuration of FPGA Core is retained, and Array Power is gated • PLL, OSC and OTP memory are disabled • BRAM data is retained if BRAM (0..3) Register Enable = 0 (see Reg[320] in Appendix: Register Definitions) and if BRAM (4..7) Register Enable = 0 (see Reg[321] in Appendix: Register Definitions) • GPIO is not in Hi-Z state and data is retained.
1	1	**Configuration Mode:** • From internal OTP • From external SPI • From MCU interface • FPGA Core, GPIO, BRAM, PLL, and OSC are controlled by IOBs.