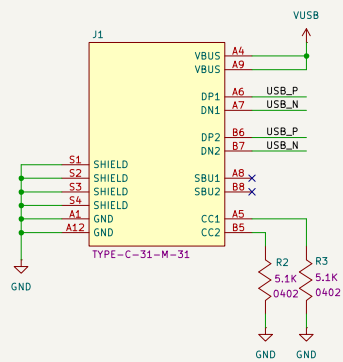
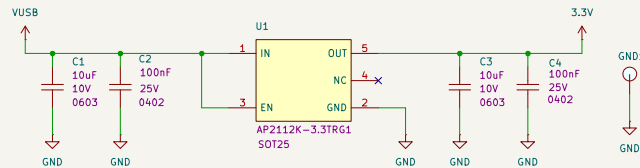


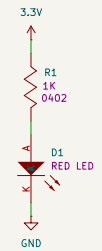
INPUT POWER



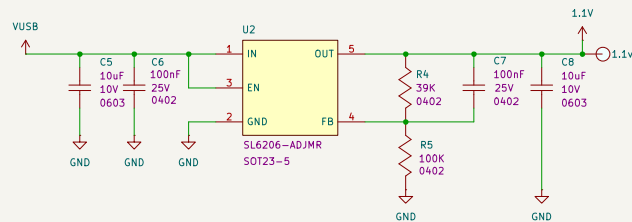
LDO 5V TO 3.3V



POWER LED



LDO 5V TO 1.1V



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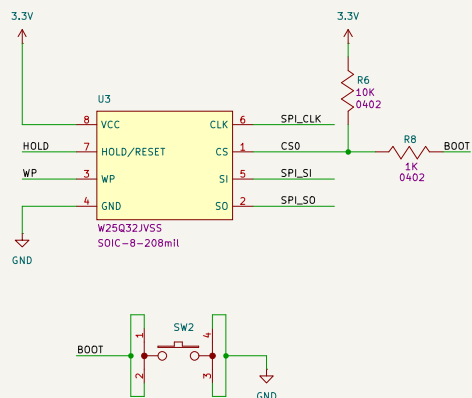
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File: Power.kicad_sch

Title: Shrike-lite

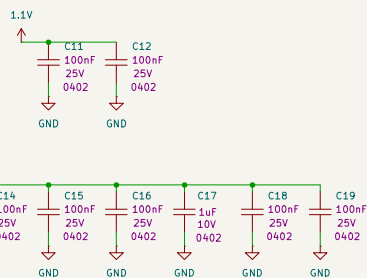
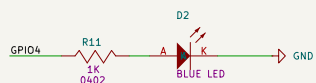
Size: A3 Date: 2026-01-29
KiCad E.D.A. 9.0.2

Rev: 0.5
Id: 4/4

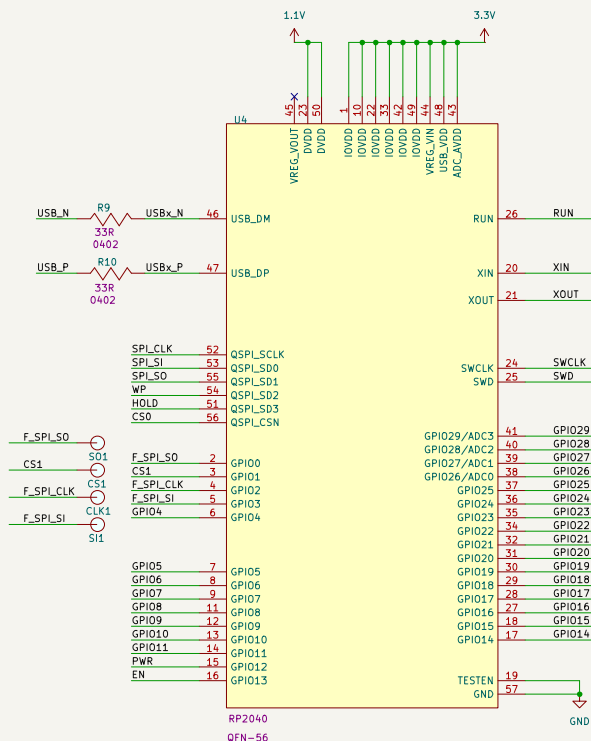
SPI Flash



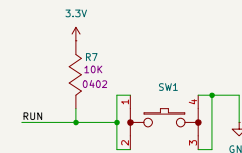
Status LED(RP2040)



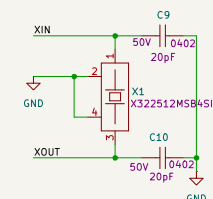
RP2040



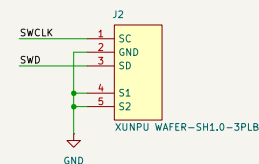
RESET BUTTON



OSCILLATOR



JST Debug Connector



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Sheet: /RP2040/

File: RP2040.kicad_sch

Title: **Shrike-lite**

Size: A3 Date: 2026-01-29

KiCad E.D.A. 9.0.2

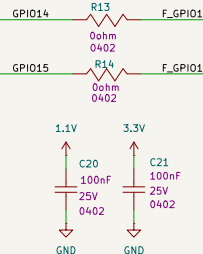
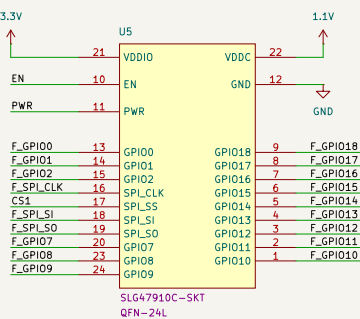
Rev: 0.5

Id: 4/4

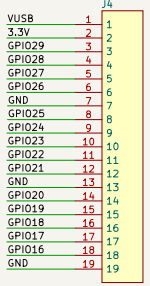
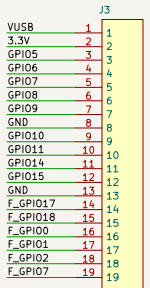
Status LED(FPGA)



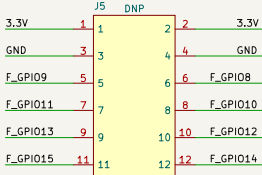
FPGA SLG47910



GPIO PINS



PMOD




Configuration of Enable and Power Reset of FPGA

GPI012 of RP2040 is connected to PWR

GPI013 of RP2040 is connected to EN

PWR (nRST)	EN (nSLEEP)	Description
0	X	Device Reset/Off State: <ul style="list-style-type: none">Configuration of FPGA Core is not retained, and Array Power is gatedPLL, OSC, and OTP memory are disabledBRAM data is not retained unless BRAM_Keep Register value at Reset = 1 (see Reg 1193) in Appendix: Register Definitions)GPIO is in Hi-Z state and not retained unless REG_GPIO_KEEP = 1
1	0	Lower Power/Retention State: <ul style="list-style-type: none">Configuration of FPGA Core is retained, and Array Power is gatedPLL, OSC and OTP memory are disabledBRAM data is retained (BRAM (0..3) Register Enable = 0 (see Reg 1203) in Appendix: Register Definitions) and eBRAM (4..7) Register Enable = 0 (see Reg 1211) in Appendix: Register Definitions)GPIO is not in Hi-Z state and data is retained
1	1	Configuration Mode: <ul style="list-style-type: none">From Internal OTPFrom external SPIFrom MCU interfaceFPGA Core, GPIO, BRAM, PLL, and OSC are controlled by I2C0s

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Sheet: /FPGA/
File: FPGA.kicad_sch

Title:

Size: A3 Date: 2026-01-29 Rev: 0.5
KiCad E.D.A. 9.0.2 Id: 4/4