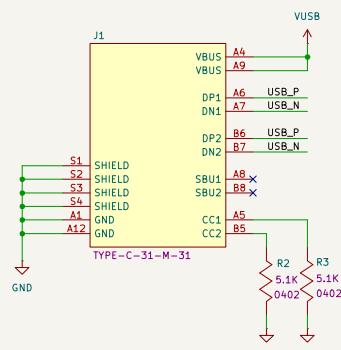
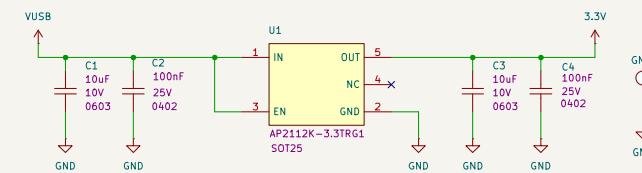


1 2 3 4 5 6 7 8

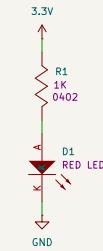
INPUT POWER



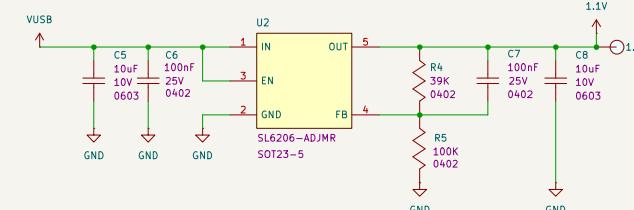
LDO 5V TO 3.3V



POWER LED



LDO 5V TO 1.1V



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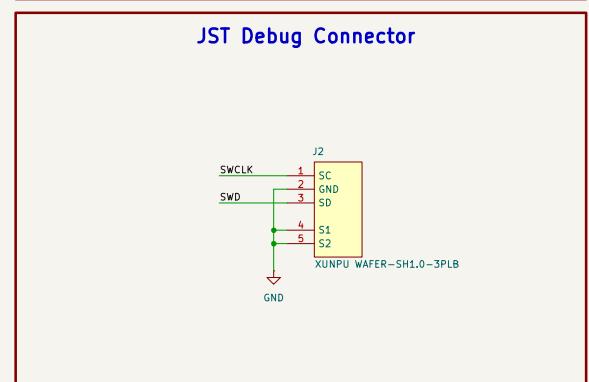
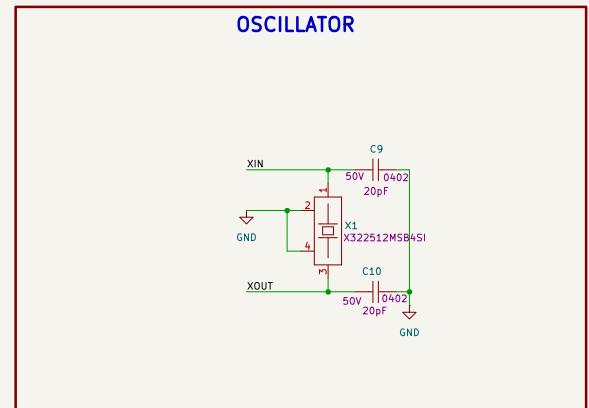
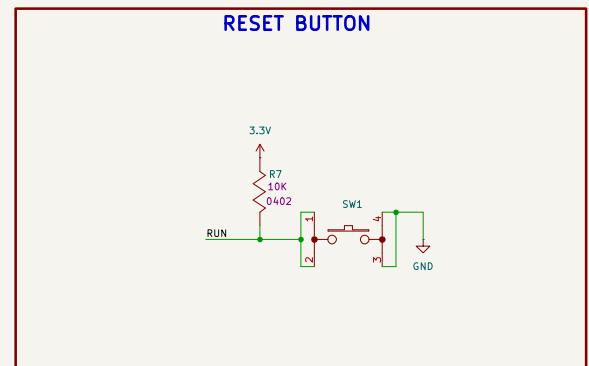
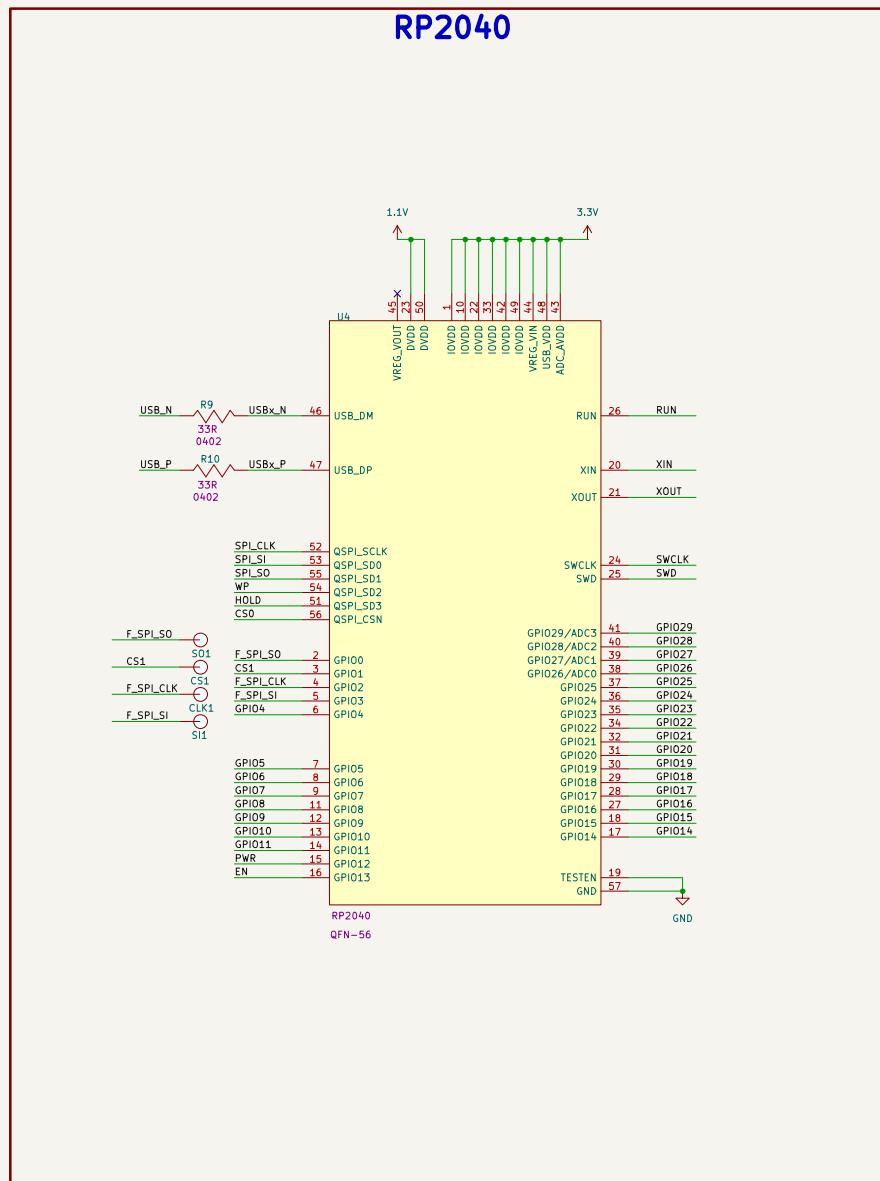
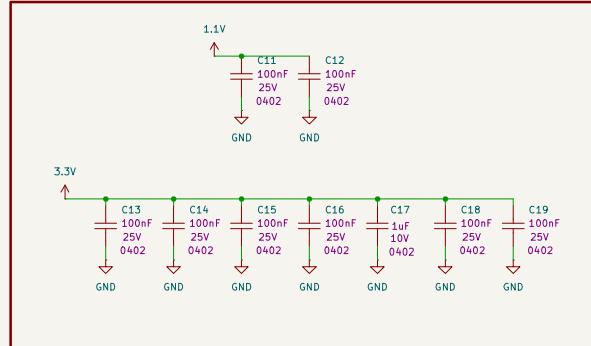
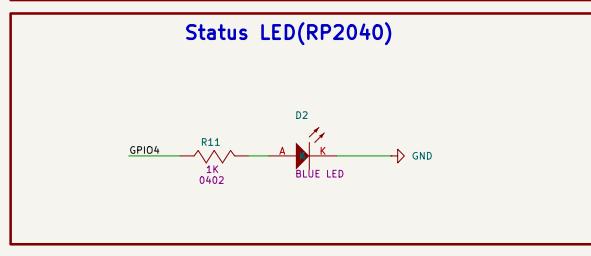
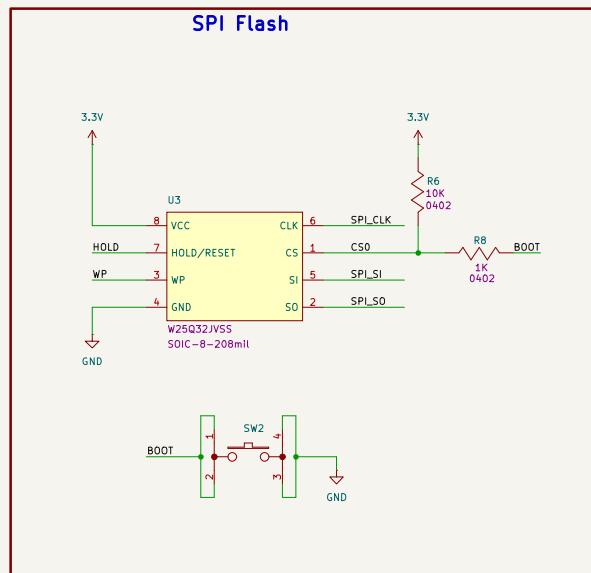
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Title: Shrike-lite

Size: A3 Date: 2026-01-29
KiCad E.D.A. 9.0.2

Rev: 0.5
Id: 4/4

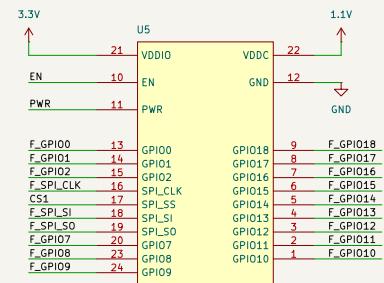
1 2 3 4 5 6 7 8



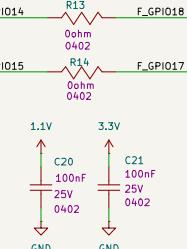
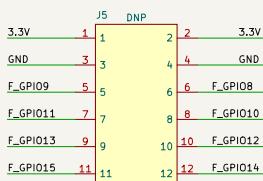
Status LED(FPGA)



FPGA SLG47910



PMOD



Configuration of Enable and Power Reset of FPGA

GPIO12 of RP2040 is connected to PWR

PWR (nRST)	EN (nSLEEP)	Description
0	X	Device Reset/Off State: • Configuration of FPGA Core is not retained, and Array Power is gated • PLL, OSC, and OTP memory are disabled • BRAM data is not retained unless BRAM Keep Register value at Reset = 1 (see Reg [193] in Appendix: Register Definitions) • GPIOs are not retained unless REG_GPIO_KEEP = 1.
1	0	Lower PowerRetention State: • Configuration of FPGA Core is retained, and Array Power is gated • PLL, OSC, and OTP memory are disabled • BRAM data is retained (BRAM (0..3) Register Enable = 0 (see Reg[220] in Appendix: Register Definitions) and if BRAM (4..7) Register Enable = 0 (see Reg[321] in Appendix: Register Definitions)) • GPIO is not in Hi-Z state and data is retained.
1	1	Configuration Mode: • Power is supplied from: • From external SPI • From MCU Interface • FPGA Core, GPIO, BRAM, PLL, and OSC are controlled by IOBs.

GPIO13 of RP2040 is connected to EN

GPIO PINS

	J3
VUSB	1
3.3V	2
GPIO5	3
GPIO6	4
GPIO7	5
GPIO8	6
GPIO9	7
GND	8
GPIO10	9
GPIO11	10
GPIO14	11
GPIO15	12
GND	13
F_GPIO17	14
F_GPIO18	15
F_GPIO10	16
F_GPIO1	17
F_GPIO2	18
F_GPIO7	19

	J4
VUSB	1
3.3V	2
GPIO23	3
GPIO28	4
GPIO27	5
GPIO26	6
GND	7
GPIO25	8
GPIO24	9
GPIO23	10
GPIO22	11
GPIO21	12
GND	13
GPIO20	14
GPIO19	15
GPIO18	16
GPIO17	17
GPIO16	18
GND	19



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Title:

Size: A3 Date: 2026-01-29
KiCad E.D.A. 9.0.2 Rev: 0.5

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