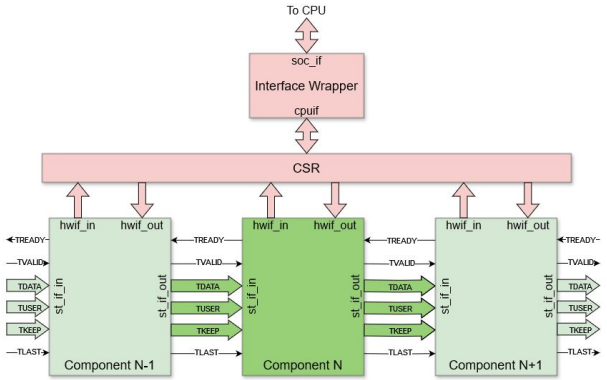
Mixed Endianness & Implementation Plan Meeting
11/26/2024

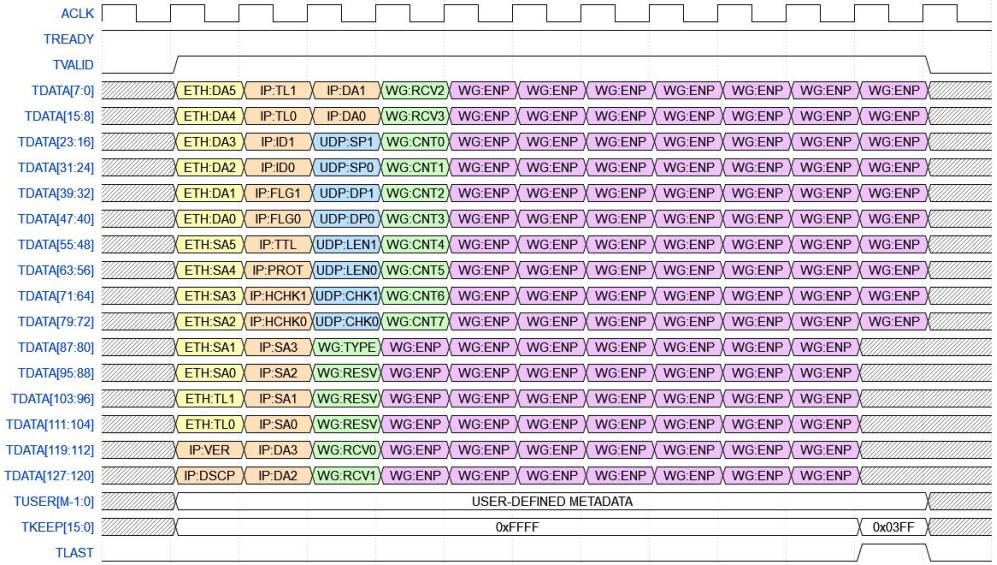
Outline

- Mixed Endianness Issue
- Implementation and Test Plan
  - ALINX Ethernet example
  - Ibex Demo System example

Mixed Endianness Issue

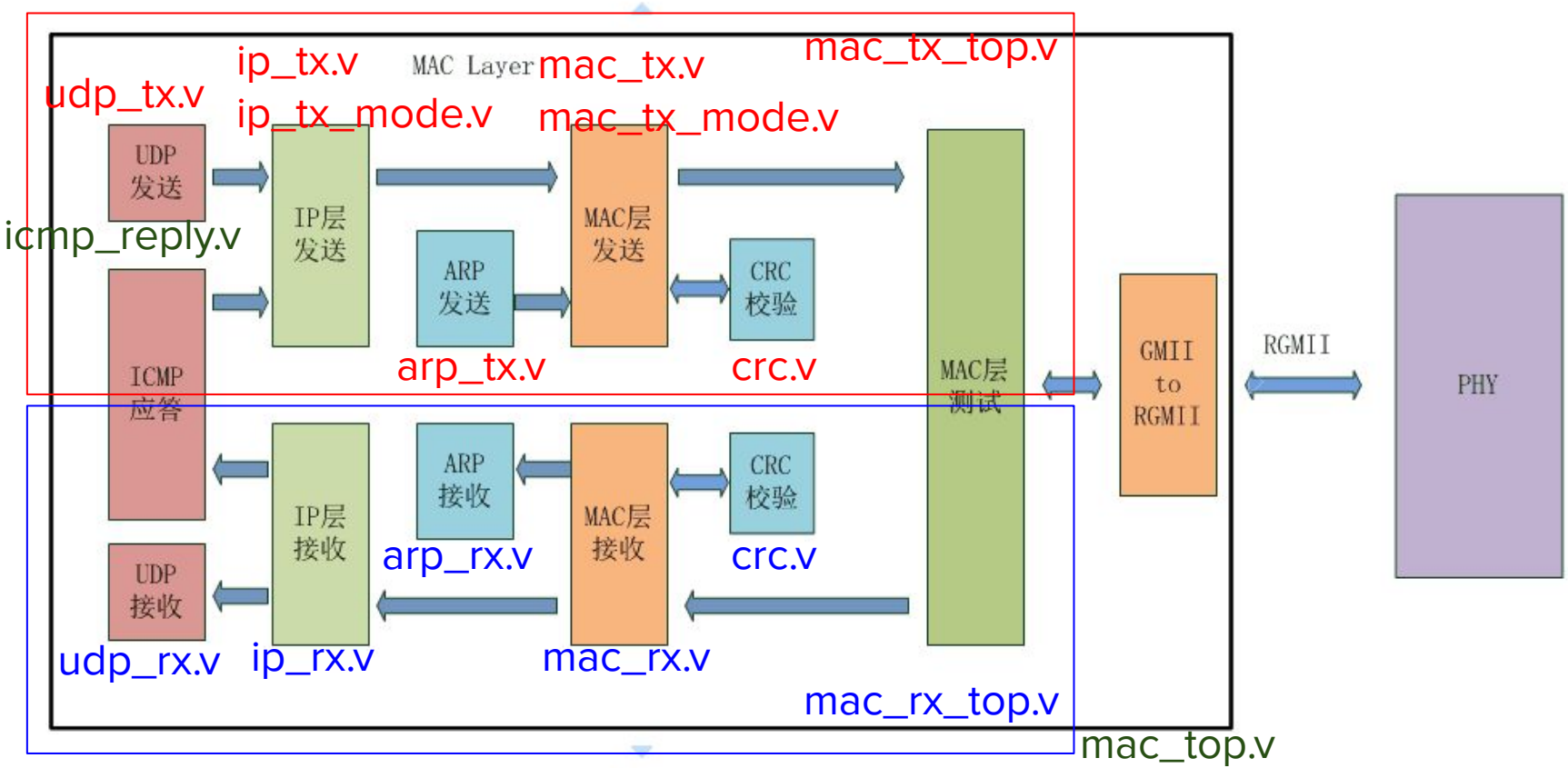
- Little-endian
  - AXI4-Stream
  - CPU (e.g. RISC-V)
  - WireGuard Protocol Header
- Big-endian
  - Ethernet, IP, UDP (network-byte order)





- Where to switch endianness?
  - SW (CPU)
  - CSR
  - DPE

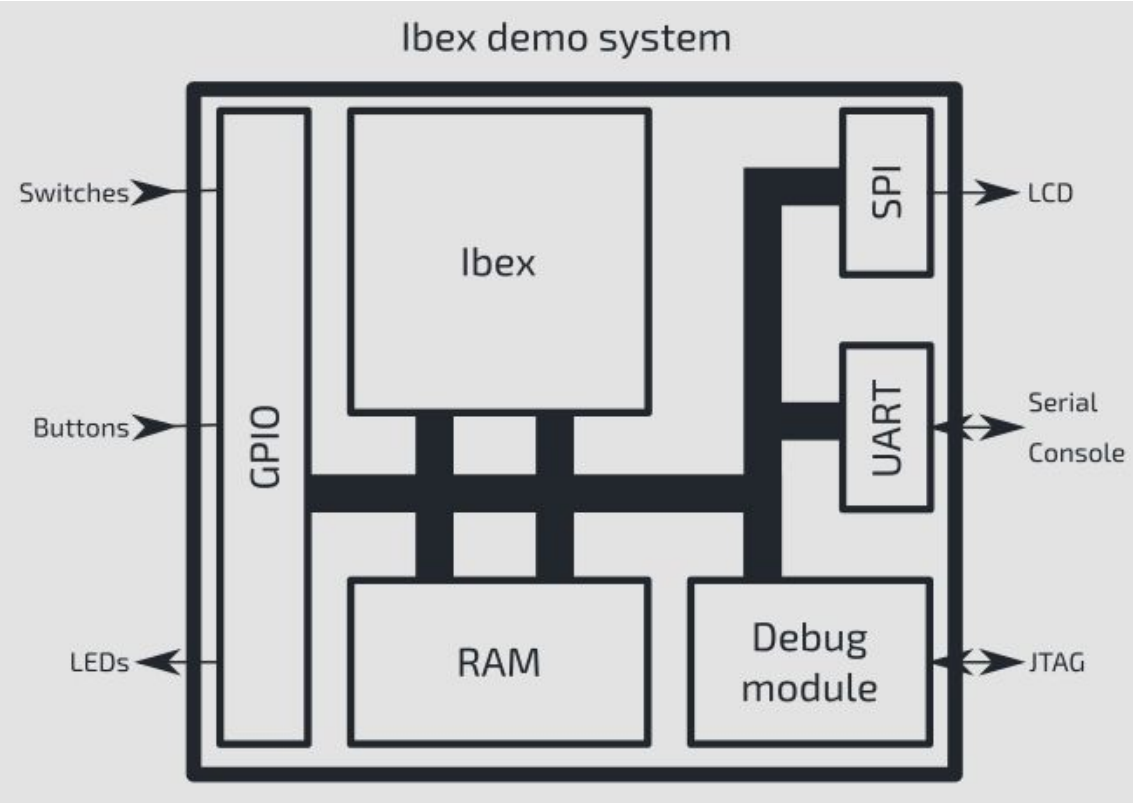
ALINX Ethernet example



ALINX Ethernet example

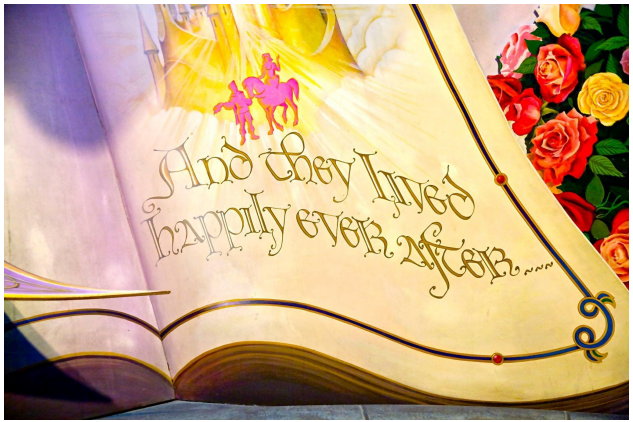
- Tasks:
  - Test provided example, i.e. PC <–> ALINX board
    - Chapter 6 from *ethernet_test.pdf*
  - Clean and simplify RTL
    - Remove unnecessary UDP, IP and ICMP RTLs
    - Encapsulate Rx/Tx MAC, Rx/Tx ARP and CRCs into single MAC RTL
  - Make a simple Ethernet bridge
    - Instantiate MAC for each Ethernet PHY (ports)
    - Connect the Rx MAC output of the port 1 to the Tx MAC input of the port 2, and vice-versa
    - Connect PC1 to the port 1 and PC2 to the port 2
    - Ping test PC1 <–> ALINX board <–> PC2
  - Rework Tx/Rx MAC interfaces into AXI4-Stream Packet interfaces

Ibex Demo System example



Ibex Demo System example

- Tasks:
  - Test provided example, i.e. *Hello World*
  - Test debug module
  - Investigate the possibility of CSR integration at the GPIO location
  - Test simple PeakRDL workflow:
    - Describe a simple register for the GPIO LEDs
    - Compile RDL to SystemVerilog and C headers
    - Integrate generated code into the Hello World example
    - Test GPIO LEDs by writing to CSR



Thank you!