JL2121(D) Datasheet

Gigabit Ethernet PHY

Doc No.: DS009-JL2121(D)-v1.11-Preliminary (July, 2022)

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Chapter 1. Overview

The JL2121(D) is a single port Gigabit Ethernet PHY transceiver supports 1000BASE-T, 100BASE-TX, and 10BASE-T in IEEE802.3 standards. Data transfer between MAC and PHY via RGMII bus. Built on advanced mixed-signal technology and process node, JL2121(D) offers unparallel performance in power consumption and cable range with reduced EMI/EMC, suitable for a wide range of applications.

The JL2121(D) MDI interface integrates MDI termination resistors to PHY, which reduces BOM and simplifies layout.

The JL2121(D) supports single 3.3V power supply with configurable RGMII bus I/O voltage supporting 3.3V, 2.5V, 1.8V.

The JL2121(D) supports Synchronous Ethernet (SyncE) and Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE1588 version 2 and IEEE 802.1AS.

The JL2121(D)I is manufactured to industrial grade standards, can operate in -40 ~ +85°C environment temperature condition.

1.1. Feature List

- 1000BASE-T/100BASE-TX/10BASE-T IEEE 802.3 Compliant
- Supports RGMII to Copper
- Supports Parallel Detection
- Supports Base Line Wander Correction
- Built-in Wake-on-LAN (WOL)
- Crossover Detection & Auto-Correction
- Supports Interrupt function
- Automatic polarity correction
- Selectable 3.3/2.5/1.8V signal voltage for RGMII
- Integrate Switching/Linear Regulator
- Supports 3.3V Single power supply
- LEDs for Network Status
- Supports 25MHz external crystal or OSC
- Selectable 25MHz/125MHz clock output
- Provides 125MHz clock source for MAC
- Support downshift mode for two-pair cables using and terrible cables using conditions
- Supports Synchronous Ethernet and Precision Time Protocol (PTP) including IEEE 1588v1, v2 and 802.1AS
- Supports Synchronous Ethernet (SyncE) Clock Recovery
- Temperature Range: -40°C ~ +85°C

- 40-pin QFN package

Features	JL2121	JL2121D
RGMII to Copper	Yes	Yes
SGMII to Copper	No	No
RGMII to Fiber/SGMII	No	No
RGMII to Copper/Fiber/SGMII with Auto-Media-Detect	No	No
Media Conversion	No	No
PTP	Yes	Yes
SyncE	Yes	Yes
WOL	Yes	Yes
Integrated Regulator	Buck	LDO
Package	QFN40 5mm x 5mm	QFN40 5mm x 5mm

1.2. Applications

- Enterprise & SOHO
- Wireless Router
- Industrial controls and automation
- LED Display

1.3. Application Diagrams

1.3.1. UTP Application Diagram

- RGMII to Copper Application

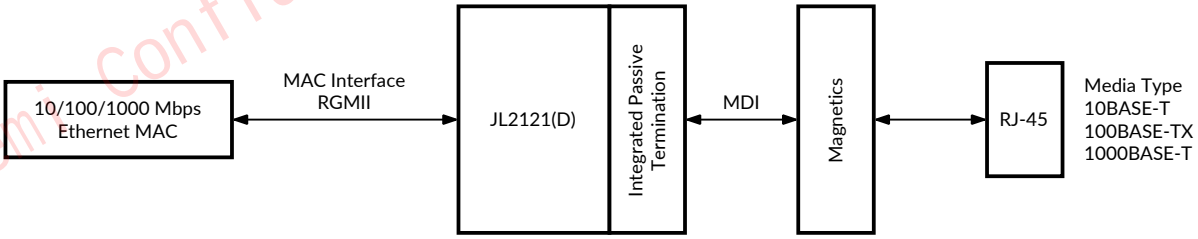


Figure 1. RGMII to Copper Application Diagram

Chapter 2. Revision History

Revision	Date	Details
v1.01-Preliminary	2020.12.03	Initial Draft
v1.02-Preliminary	2021.03.01	Update DVDD10/AVDD10 Specifications
v1.03-Preliminary	2021.06.20	1. Update chapter: Register Descriptions; 2. Update Overview chapter: Add Application Diagrams; 3. Update Pin Configuration and Function chapter: 3.1 Add Pin Type; 3.2 Change the pin descriptions in Power Supply Pins table; 4. Update Specifications chapter: 4.1 Add Crystal Requiements table; 4.2 Add Oscillator/External Clock Requiements table; 4.3 Add RGMII Interface table in DC specifications; 4.4 Change RGMII Timing figure to delete RTBI function; 5. Update Function Descriptions chapter: 5.1 Add MDI Interface Reference Design figure; 5.2 Add Hardware Configuration Reference Design figure; 5.3 Add RGMII Interface Reference Design figure; 5.4 Add LED Duplex with Strap Reference Design figure; 5.5 Add description of application in the LED function; 5.6 Add the Power function description; 5.7 Add the Power Interface Reference Design figure; 5.8 Add the Clock Interface Reference Design figure and change the description of Clock function; 6. Update Register Descriptions chapter: Change the Page and Register value from DEC to HEX; 7. Update Order Information and Support chapter: Add the silk screen figure;
v1.04-Preliminary	2021.06.23	1. Split JL2x01 datasheet document to JL2121 datasheet and JL2201 datasheet 2. Add SMI timing diagram 3. Add LCR register bit 15 LED_MODE function 4. Add Register Type description 5. Change package A(thin of ic) value 6. Add silkscreen description in chapter Order Information 7. Delete the overview item in chapter Function Description
v1.05-Preliminary	2021.07.13	1. Update the Design Guide chapter. 1.1 Add the diagram of REG_OUT pin layout guide 1.2 Change the diagram of power decoupling layout guide.
v1.06-Preliminary	2021.08.31	1. Remove JL2201(D) informations from Feature List table and Ordering Guide table and Application Diagrams. 2. Add Power Consumption table to DC Specifications chapter 3. Change the pin name AVDD1V0 DVDD1V0 to AVDDL DVDDL, and change this pin type voltage from 1.0V to 0.9V 4. Change the voltage description of REG_OUT pin from 1.0V to 0.9V 5. Change the $T_{operation}$ in Recommended Operating Conditions table 6. Change the WOL funtion description in Functional Description Chapter 7. Change the Loopback function description in Functional Description Chapter 8. Change the RGMII I/O voltage from 2.5V to 2.75V when V_SEL[1:0]=0b01, and add the method how to change the voltage to 2.5V by setting register 9. Fine tune some V_{IH} and V_{IL} value in RGMII interface table of DC Characteristics chapter 10. Update the Packaging Information dimension table 11. Add software reset de-assert time description to BMCR register table

Revision	Date	Details
v1.07-Preliminary	2021.10.14	1. Remove V_{IH} MAX value in Crystal Requirements table. 2. Remove V_{IH} MAX value in Oscillator/External Clock Requirements table. 3. Add 4.7uH inductor description which can be used to REG_OUT. 4. Fix the description error of IODVDD using in function descripiton chapter and pin description chapter. 5. Add 1000Base-X ANAR, 1000Base-X ANLPAR, SGMII ANAR, SGMII ANLPAR, four registers to register description chapter 6. Change the description of power in "Funciton Descript" chapter. 7. Add the t_3 RSTn hold time after powers are ready in "power up and reset timing" diagram and table. 8. Change the exposed pad dimension to 3.2~3.8. 9. Separate power diagram to buck and ldo situation.
v1.08-Preliminary	2021.11.22	1. Remove the support of IODVDD 1.5V. 2. Add RGMII Timing With Delay Intergrated At Transmitter table and diagram in "AC Specifications" Chapter. 3. Add more description to V_SEL[1:0] = 00 condition in Strap pin table
v1.09-Preliminary	2021.12.30	1. Change the description of V_SEL[1:0] strap pin in Strap Option table. 2. Change the default value of V_SEL[1:0] strap pin. 3. Add Thermal Information table to Specifications chapter include $R_{\theta JA}$ and $R_{\theta JC(top)}$ charactorastics
v1.10-Preliminary	2022.5.12	1. Remove 1000Base-X ANAR, 1000Base-X ANLPAR, SGMII ANAR, SGMII ANLPAR, four registers from register description chapter. 2. Change Auto-Negotiation Advertisement Register [15:5] type to RW. 3. Add power domain diagram. 4. Change V_SEL=0b01 description from 2.75V to 2.5V in Strap Option table of Pin Description chapter and Power section of Feature Description chapter.
v1.11-Prelimiary	2022.7.1	1. Add power consumption section to Chapter DC Specfications. 2. Add Downshift feature and description to datasheet. 3. Change model number of PHYID2 register to 0b000011. 4. Add PTP feature and description to datasheet. 5. Change the PIN31 name from INTn/WOL to INTn/PMEn and the type form O to OD.

Chapter 3. Pin Configuration and Functions

3.1. Pin Type

I:	Input	O:	Output
IO:	Bi-Directional Input and Output	LI:	Latch Input During Power On Reset
PU:	With Internal Pull-up	PD:	With Internal Pull-down
P:	Power	G:	Ground
OD:	Open Drain	Z:	Tri-state output

3.2. JL2121(D) Package Pin Assignments

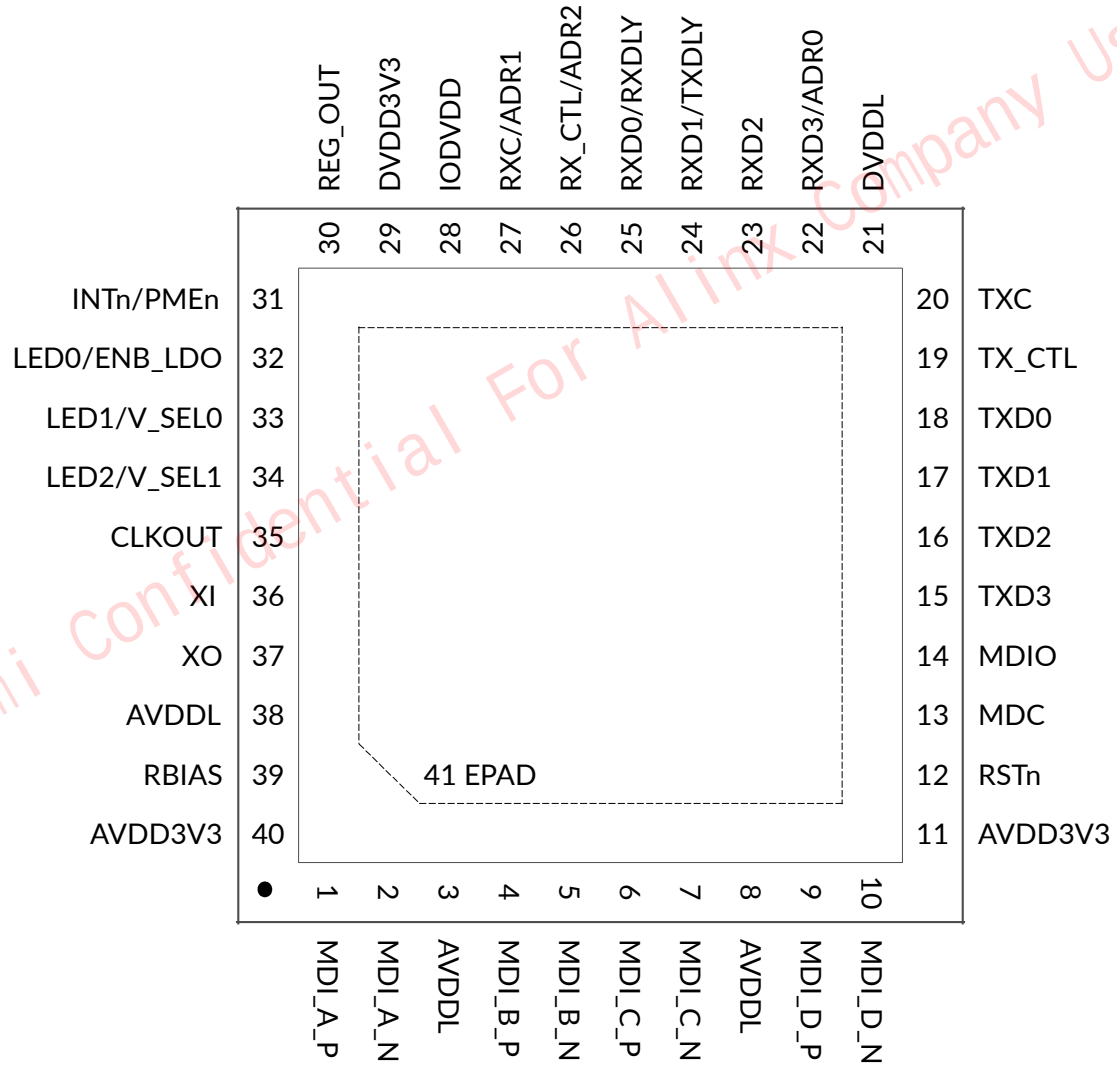


Figure 2. Package 40-Pin (Top View)

Table 1. JL2121(D) Package Pin Assignments

Pin No.	Pin Name	Type	Strap	Description
1	MDI_A_P	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
2	MDI_A_N	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
3	AVDDL	P		0.9V Analog power input
4	MDI_B_P	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
5	MDI_B_N	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
6	MDI_C_P	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
7	MDI_C_N	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
8	AVDDL	P		0.9V Analog power input
9	MDI_D_P	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
10	MDI_D_N	I/O		Media Dependent Interface, Differential Transmit and Receive Signals
11	AVDD3V3	P		3.3V Analog power Input
12	RSTn	I		PHY reset, active low
13	MDC	I/PU		Management data clock
14	MDIO	I/O/PU		Management data Input/Output
15	TXD3	I/PD		Transmit Data
16	TXD2	I/PD		Transmit Data
17	TXD1	I/PD		Transmit Data
18	TXD0	I/PD		Transmit Data
19	TX_CTL	I/PD		Transmit control signal
20	TXC	I/PD		Transmit reference clock
21	DVDDL	P		0.9V Digital core power input
22	RXD3/ADR0	O/LI/PU	PHY ADDRESS[0]	Receive Data
23	RXD2	O/LI/PD		Receive Data
24	RXD1/TXDLY	O/LI/PD	RGMII transmit timing control	Receive Data
25	RXD0/RXDLY	O/LI/PU	RGMII receive timing control	Receive Data
26	RX_CTL/ADR2	O/LI/PD	PHY ADDRESS[2]	Receive control signal
27	RXC/ADR1	O/LI/PD	PHY ADDRESS[1]	Receive reference clock
28	IODVDD	P		Digital I/O power input for RGMII I/O, MDC/MDIO and RSTn pad power
29	DVDD3V3	P		Digital I/O power input for non-RGMII I/O and switching regulator
30	REG_OUT	O		0.9V Regulator output
31	INTn/PMEn	OD		Interrupt output, Power Management Event of WOL output.
32	LED0/ENB_LDO	O/LI/PD	Internal IO LDO configuration	LED0
33	LED1/V_SEL0	O/LI/PD	RGMII I/O Voltage Selection[0]	LED1

Pin No.	Pin Name	Type	Strap	Description
34	LED2/V_SEL1	O/LI/PU	RGMII I/O Voltage Selection[1]	LED2
35	CLKOUT	O		1. 25/125MHz clock output, 2. SyncE UTP recovered clock output, 3. SyncE Fiber recovered clock output,
36	XI	I		25MHz Crystal input
37	XO	O		25MHz Crystal output
38	AVDDL	P		0.9V Analog power input
39	RBIAS	O		Constant voltage reference
40	AVDD3V3	P		3.3V Analog power input
41	EPAD	GND		Ground

3.3. JL2121(D) Pin Description

Table 2. Serial Management Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
MDC	13	I/PU	Management Data Clock: Synchronous clock to the TDO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 12.5 MHz with no minimum clock rate.
MDIO	14	I/O/PU	Management Data Input/ Output: Bi-directional management instruction/ data signal that may be sourced by the station management entity or the PHY. This pin is suggested to add an 1.5-10kΩ pullup resistor.
INTn/PMEn	31	OD	1.Interrupt output, active low. 2.Power Management Event of WOL output, active low.

Table 3. RGMII Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
TX_CTL	19	I/PD	RGMII Transmit Control. TX_EN is presented on the rising edge of TXC. A logcal derivative of TX_EN and TX_ER is presented on the falling edge of TXC.
TXC	20	I/PD	RGMII Transmit Clock. This reference clock is a 125MHz in 1000Mbps,25MHz in 100Mbps, or 2.5MHz in 10Mbps sourced from MAC.
TXD3	15	I/PD	RGMII Transmit Data. TXD[3:0] run at double data rate with bits[3:0] of each byte to be transmitted on the resing edge of TXC, and bits[7:4] presented on the falling edge of TXC. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TXC.
TXD2	16	I/PD	
TXD1	17	I/PD	
TXD0	18	I/PD	
RX_CTL	26	O/LI/PD	RGMII Receive Control. RX_DV is presented on the rising edge of RXC. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RXC.
RXC	27	O/LI/PD	RGMII Receive Clock provides a 125MHz in 1000Mbps,25MHz in 100Mbps, or 2.5MHz in 10Mbps reference clock.
RXD3	22	O/LI/PU	RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] of each byte received on the rising edge of RXC, and bits [7:4] presented on the falling edge of RXC. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RXC.
RXD2	23	O/LI/PD	
RXD1	24	O/LI/PD	
RXD0	25	O/LI/PU	

Table 4. Clock Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
CLKOUT	35	O	1. 25/125MHz Clock Output synchronized with the 25 MHz reference clock, 2. SyncE UTP recovered clock output, 3. SyncE Fiber recovered clock output,
XI	36	I	25MHz crystal input. If use external 25MHz oscillator or other drivers, connect this pin to external clock drvier output.

PIN NAME	PIN NO.	I/O	DESCRIPTION
XO	37	O	25MHz crystal output. if XI is drived by external 25MHz oscillator or other drivers, than XO should be floating.

Table 5. LED Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
LED0	32	O/LI/PD	LED output, the display mode can be programmed. The default mode: Output High if 10M Link and Blink if 10M Activity.
LED1	33	O/LI/PU	LED output, the display mode can be programmed. The default mode: Output Low if 100M Link and Blink if 100M Activity
LED2	34	O/LI/PD	LED output, the display mode can be programmed. The default mode: Output High if 1000M Link and Blink if 1000M Activity.

Table 6. Reset

PIN NAME	PIN NO.	I/O	DESCRIPTION
RSTn	12	I	Hardware reset, Active Low. The reset pin is on IODVDD power domain, if the reset external drive voltage does not equal the IODVDD voltage, for example, IODVDD is 1.8V and reset pin connect to 3.3V voltage driver, there must be 10k ohm isolation resistance between reset pin and driver circuit.

Table 7. Strap Option

PIN NAME	PIN NO.	I/O	DESCRIPTION
RXDLY	25	O/LI/PU	1: add 2ns delay to RXC 0: No additional delay
TXDLY	24	O/LI/PD	1: add 2ns delay to TXC 0: No additional delay
ADR2	26	O/LI/PD	Set the PHY address for the device.It supports the PHY address from 0x0 to 0x7. The 0x0 is a broadcast address on default. This function can be disabled by setting MDIO config.
ADR1	27	O/LI/PD	
ADR0	22	O/LI/PU	
ENB_LDO	32	O/LI/PD	Control of internal LDO for IO supply: 1: Disable internal LDO, IODVDD pin need to connect external power supply for the I/O pad. 0: Enable internal LDO, LDO output is determined by strap V_SEL[1:0], IODVDD need to connect at least 0.1uF capacitor.
V_SEL1	34	O/LI/PD	RGMII and SMI I/O Voltage Selection(V_SEL[1:0]): When enable internal LDO (ENB_LDO = 0). 00: Reserved; 01: 2.5V(default); 10: 1.8V. When disable internal LDO (ENB_LDO = 1). The configuration of these strap pins will be ignored.
V_SEL0	33	O/LI/PU	

Table 8. Media Dependent Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
MDI_A_P	1	I/O	Media Dependent Interface[A]. In 1000BASE-T mode , MDI_A_N/P are used to transmit and receive simultaneously.In MDI mode, MDI_A_N/P correspond to BI_DA±.In MDIX mode, MDI_A_N/P correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes, MDI_A_N/P are used for the transmit in MDI mode and are used for the receive pair in MDIX mode
MDI_A_N	2	I/O	
MDI_B_P	4	I/O	Media Dependent Interface[B]. In 1000BASE-T mode , MDI_B_N/P are used to transmit and receive simultaneously.In MDI mode, MDI_B_N/P correspond to BI_DB±.In MDIX mode, MDI_B_N/P correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes, MDI_B_N/P are used for the receive in MDI mode and are used for the transmit pair in MDIX mode
MDI_B_N	5	I/O	
MDI_C_P	6	I/O	Media Dependent Interface[C]. In 1000BASE-T mode , MDI_C_N/P are used to transmit and receive simultaneously.In MDI mode, MDI_C_N/P correspond to BI_DC±.In MDIX mode, MDI_C_N/P correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDI_C_N/P are not used.
MDI_C_N	7	I/O	
MDI_D_P	9	I/O	Media Dependent Interface[D]. In 1000BASE-T mode , MDI_D_N/P are used to transmit and receive simultaneously.In MDI mode, MDI_D_N/P correspond to BI_DC±.In MDIX mode, MDI_D_N/P correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDI_D_N/P are not used
MDI_D_N	10	I/O	

Table 9. Reference

PIN NAME	PIN NO.	I/O	DESCRIPTION
RBIAS	39	O	Constant voltage reference. External 2.49 kΩ 1% resistor connection to GND is required for this pin.

Table 10. Power Supply Pins

PIN NAME	PIN NO.	I/O	DESCRIPTION
AVDD3V3	11,40	P	3.3V Analog power input
AVDDL	3,8,38	P	0.9V Analog power input
DVDDL	21	P	0.9V Digital core power input
IODVDD	28	P	Digital I/O power input for RGMII I/O, MDC/MDIO and RSTn pad power. If pull high ENB_LDO pin to disable internal LDO, this pin should be connected to the external power source for 3.3/2.5/1.8V. If pull low or float ENB_LDO pin to enable internal LDO, this pin should be connected to at least 0.1uF capacitor, the IODVDD power value is according to V_SEL[1:0] configuration.
DVDD3V3	29	P	Digital I/O power input for non-RGMII I/O and switching regulator
REG_OUT	30	O	0.9V Switching regulator output(2121).
EPAD	41	GND	Ground

3.4. JL2121(D) Package Pin Assignments

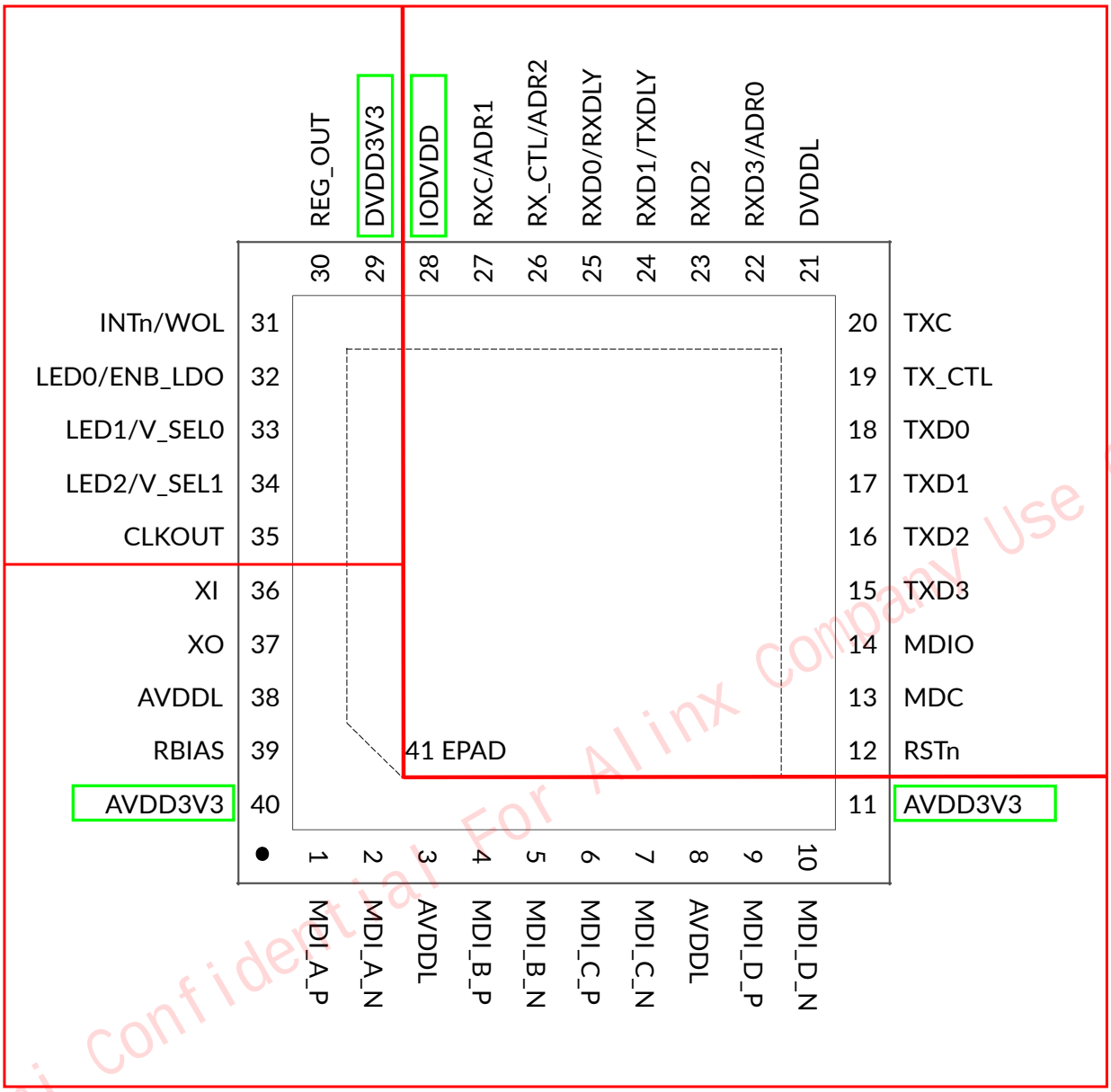


Figure 3. Power Domain Diagram

Chapter 4. Specifications

4.1. Absolute Maximum Ratings

Symbol	Description	MIN	MAX	UNIT
VDD3V3	3.3V Digital and analog supply voltage	-0.5	3.63	V
DVDDL	0.9V Digital core supply voltage	-0.3	1.05	V
AVDDL	0.9V Analog core supply Voltage	-0.3	1.2	V
V_{IO} (all pins)	DC input voltage	-0.5	3.63	V
$T_{Storage}$	Storage temperature		150	°C
$T_{Junction}$	Operating junction temperature	-40	125	°C
T_{Lead}	Lead temperature (soldering 10 seconds)		260	°C
T_{FL}	Floor Life (25°C/60% RH)		168	Hours

4.2. ESD Ratings

ESD Requirements	NOTE	VALUE	UNIT
HBM(ANSI/ESDA/JEDEC JS-001-2017)	For MDI Pins	> 8000	V
	For non-MDI Pins	2000	
CDM (ANSI/ESDA/JEDEC JS-002-2014)	/	500	

4.3. Recommended Operating Conditions

Symbol	Description	MIN	MAX	UNIT
VDD3V3	3.3V Digital and analog supply voltage	3.0	3.6	V
DVDDL	0.9V Digital core supply voltage	0.85	1.05	V
AVDDL	0.9V Analog supply Voltage	0.85	1.2	V
$T_{Operation}$ JL2121(D)-N040C	Ambient operating temperature	0	70	°C
$T_{Operation}$ JL2121(D)-N040I	Ambient operating temperature	-40	85	°C
$T_{Junction}$	Maximum junction temperature	-	125	°C

4.4. Thermal Information

Symbol	Description	TYP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.5	°C/W

4.5. Crystal Requirements

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
Crystal DC Characteristics						
F_{ref}	Crystal Reference Frequency		25		MHz	
FT	Crystal Frequency Tolerance			±50	ppm	Operational Temp
FS	Crystal Frequency Stability			±50	ppm	5 year aging
$T_{Rise/Fall}$	Rise/Fall Time			6	nsec	10% - 90%
J	Cycle to Cycle Jitter			500	ps	short term (peak to peak value)
J_{RMS}	RMS Jitter(1)			100	ps	long term (RMS value)
Symmetry	Duty Cycle	40%		60%		
V_{IH}	Crystal Output High Level	1.15			V	
V_{IL}	Crystal Output Low Level			0.25	V	

Note:

1. integrated range from 10kHz to 12.5MHz

4.6. Oscillator/External Clock Requirements

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
External Clock DC Characteristics						
F	Frequency		25		MHz	
FT	Frequency Tolerance			±50	ppm	Operational Temp
FS	Frequency Stability			±50	ppm	5 year aging
$T_{Rise/Fall}$	Rise/Fall Time			3	nsec	10% - 90%
J	Cycle to Cycle Jitter			500	ps	short term (peak to peak value)
J_{RMS}	RMS Jitter(1)			100	ps	long term (RMS value)
Symmetry	Duty Cycle	40%		60%		Duty Cycle
V_{IH}	Clock Driver Output High Level	1.15			V	
V_{IL}	Clock Driver Output Low Level			0.25	V	

Note:

1. integrated range from 10kHz to 12.5MHz

4.7. DC Specifications

4.7.1. MDI Interface

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
V_{PD_TX}	Transmit differential peak voltage	10BASE-T	2.2	2.5	2.8	V
		100BASE-TX	0.950	1.000	1.050	V
		1000BASE-T	0.67	0.75	0.82	V

4.7.2. RGMII Interface

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
IODVDD 3.3V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	2.8			V	I_{OH}=-20mA IODVDD=3.3V±10%
V_{OL}	Low Level Output Voltage			0.5	V	I_{OL}=20mA IODVDD=3.3V±10%
V_{IH}	High Level Input Voltage	2.0			V	IODVDD=3.3V±10%
V_{IL}	Low Level Input Voltage			0.8	V	IODVDD=3.3V±10%
I_{IH}	Input High Current	-150		150	μA	VIN=IODVDD
I_{IL}	Input Low Current	-150		150	μA	VIN=GND
V_{RGMII}	RGMII Supply Voltage (Include MDC/MDIO)	2.97	3.3	3.63	V	
IODVDD 2.5V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	2.0			V	I_{OH}=-20mA IODVDD=2.5V±5%
V_{OL}	Low Level Output Voltage			0.5	V	I_{OL}=20mA IODVDD=2.5V±5%
V_{IH}	High Level Input Voltage	1.7			V	IODVDD=2.5V±5%
V_{IL}	Low Level Input Voltage			0.7	V	IODVDD=2.5V±5%
I_{IH}	Input High Current	-100		100	μA	VIN=VDDIO
I_{IL}	Input Low Current	-100		100	μA	VIN=GND
V_{RGMII}	RGMII Supply Voltage (Include MDC/MDIO)	2.25	2.5	2.75	V	
IODVDD 1.8V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	1.5			V	I_{OH}=-10mA IODVDD=1.8V±5%
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL}=10mA IODVDD=1.8V±5%
V_{IH}	High Level Input Voltage	1.2			V	IODVDD=1.8V±5%
V_{IL}	Low Level Input Voltage			0.5	V	IODVDD=1.8V±5%
I_{IH}	Input High Current	-75		75	μA	VIN=IODVDD

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
I_{IL}	Input Low Current	-75		75	μA	VIN=GND
V_{RGMII}	RGMII Supply Voltage (Include MDC/MDIO)	1.62	1.8	1.98	V	

4.7.3. Power Consumption

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
JL2121(BUCK), AVDDL=0.9V, DVDDL=0.9V, AVDD3V3=3.3V, DVDD3V3=3.3V, IODVDD=3.3V					
1000BASE-T	RGMII, MDI Link-Up, No Traffic		518		mW
	RGMII, MDI Link-Up, 96-ns IPG (100% Utilization), 1518-byte Packets		653		mW
JL2121D(LDO), AVDDL=0.9V, DVDDL=0.9V, AVDD3V3=3.3V, DVDD3V3=3.3V, IODVDD=3.3V					
1000BASE-T	RGMII, MDI Link-Up, No Traffic		759		mW
	RGMII, MDI Link-Up, 96-ns IPG (100% Utilization), 1518-byte Packets		891		mW

4.8. AC Specifications

4.8.1. Power Up and Reset Timing

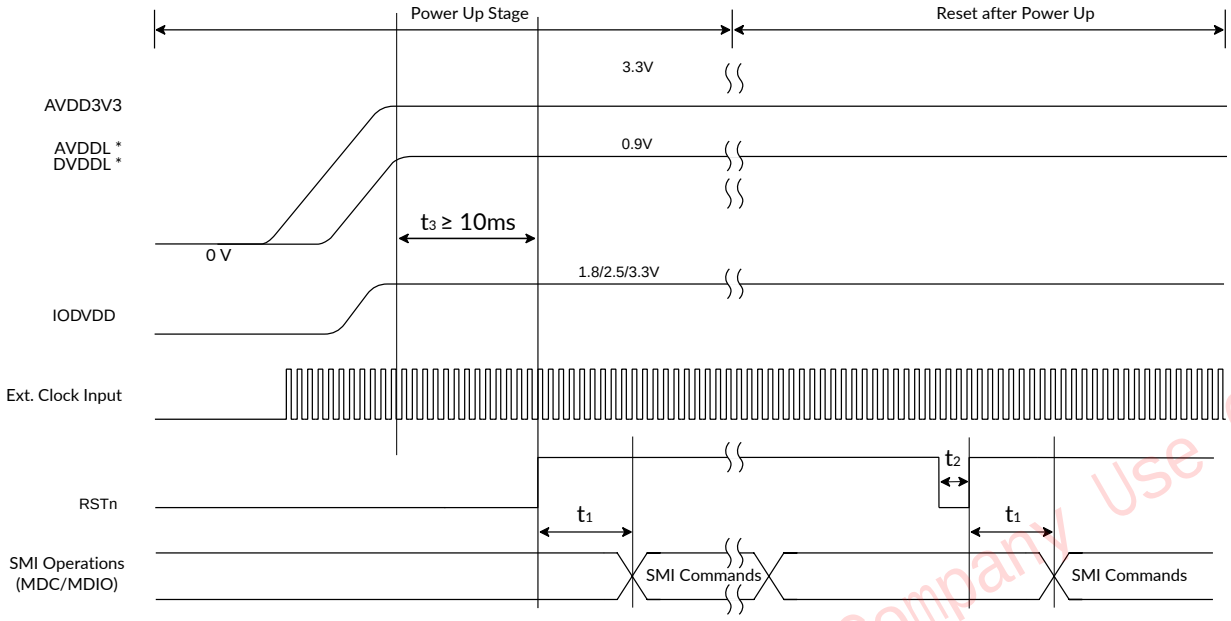


Figure 4. Power Up Sequence Timing

NOTE AVDDL and DVDDL sequence in this diagram only express when using external 0.9V power source condition, if we use REG_OUT pin to supply AVDDL and DVDDL, there is no necessary to consider AVDDL and DVDDL sequence which is under IC control.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	RSTn de-assert time after all powers are ready	10			ms
t_2	RSTn assert time	1			ms
t_3	RSTn hold time after powers are ready	10			ms

4.8.2. Serial Management Interface(SMI) Timing

DESCRIPTION	MIN	TYP	MAX	UNIT
MDC to MDIO (output) delay time	0		60	ns
MDIO (input) to MDC setup time	10			ns
MDIO (input) to MDC hold time	10			ns
MDC frequency			12.5	MHz

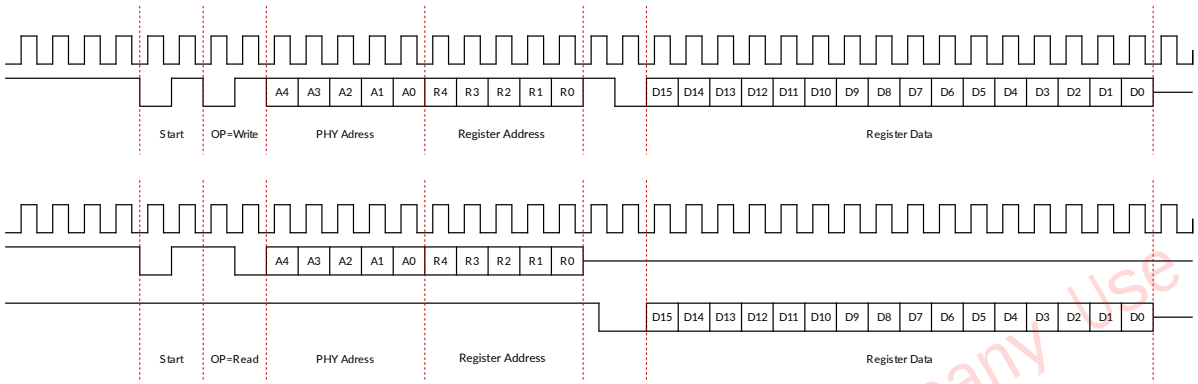


Figure 5. SMI Timing

4.8.3. RGMII Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	1		2.6	ns
T_{cyc}	Duty Cycle Duration	7.2	8	8.8	ns
$Duty_G$	Duty Cycle for Gigabit	45	50	55	%
$Duty_T$	Duty Cycle for 100Base-X/10Base-T	40	50	60	%
T_r/T_f	Rise/Fall Time (20-80%)			0.75	ns

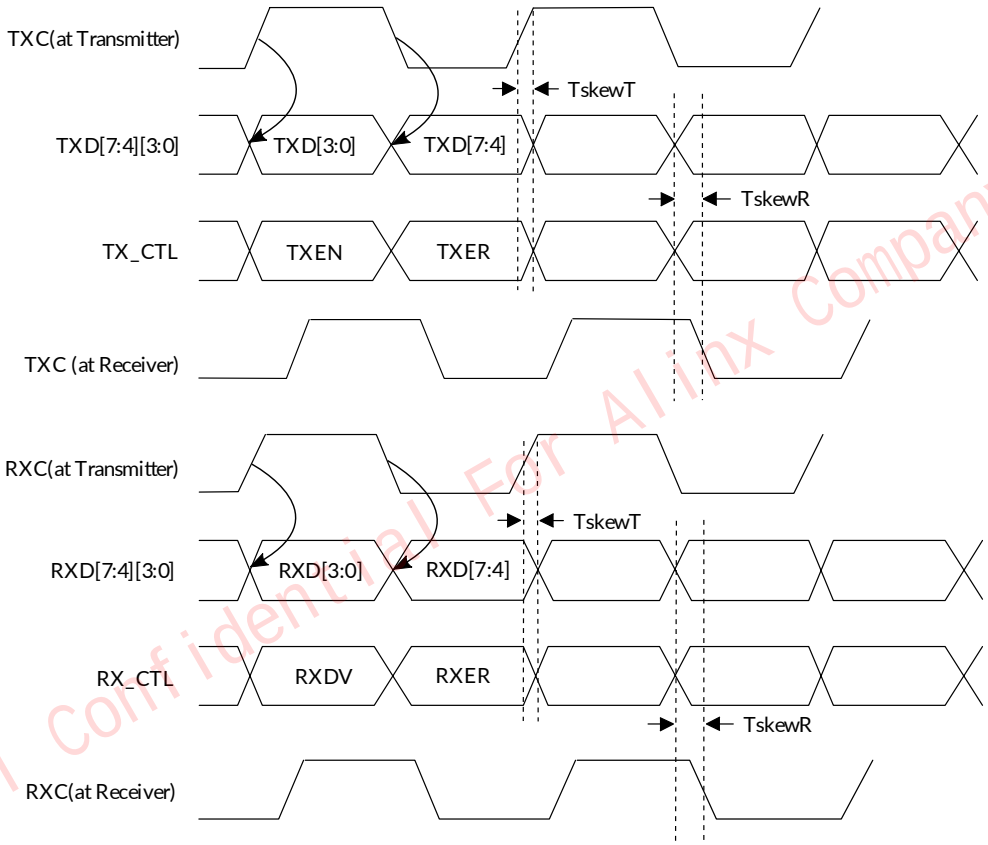


Figure 6. RGMII Timing

4.8.4. RGMII Timing With Delay Intergrated At Transmitter

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{setupT}	Data to Clock Output Setup Time (at Transmitter)	1.2	2		ns
T_{holdT}	Clock to Data Output Hold Time (at Transmitter)	1.2	2		ns
T_{setupR}	Data to Clock Input Setup Time (at Receiver)	1.0	2		ns
T_{holdR}	Clock to Data Input Hold Time (at Transmitter)	1.0	2		ns

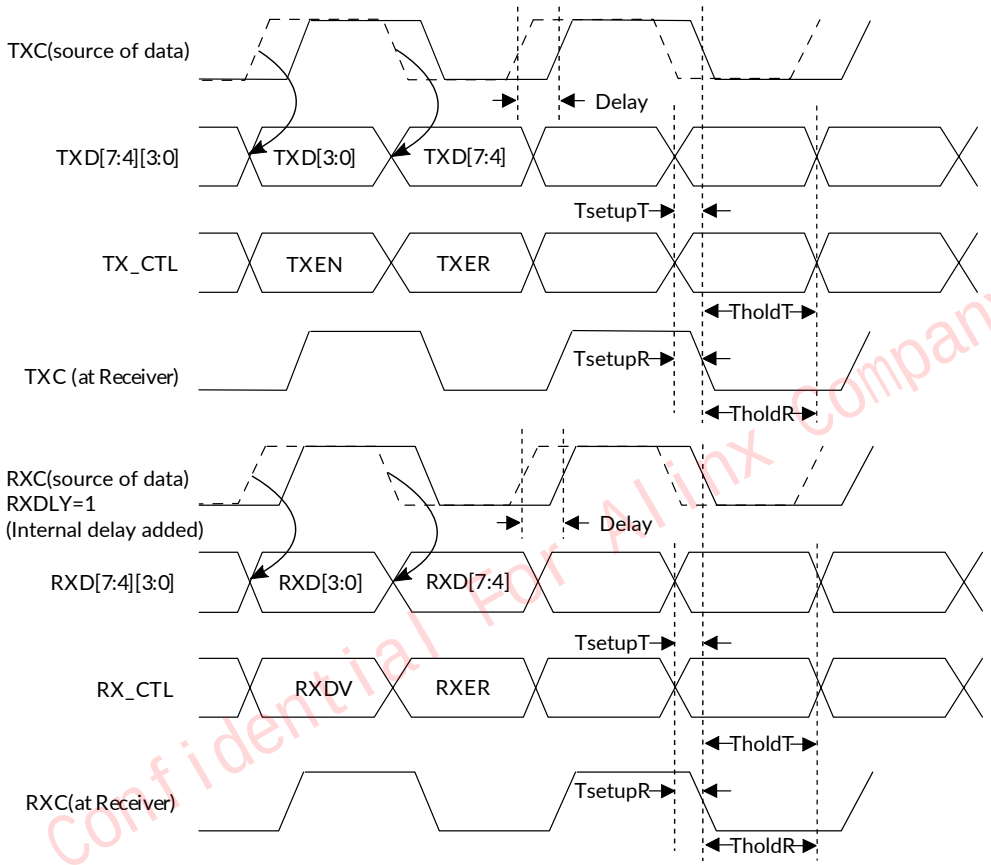


Figure 7. RGMII Timing With Delay Intergrated At Transmitter

Chapter 5. Functional Description

5.1. Functional Block Diagram

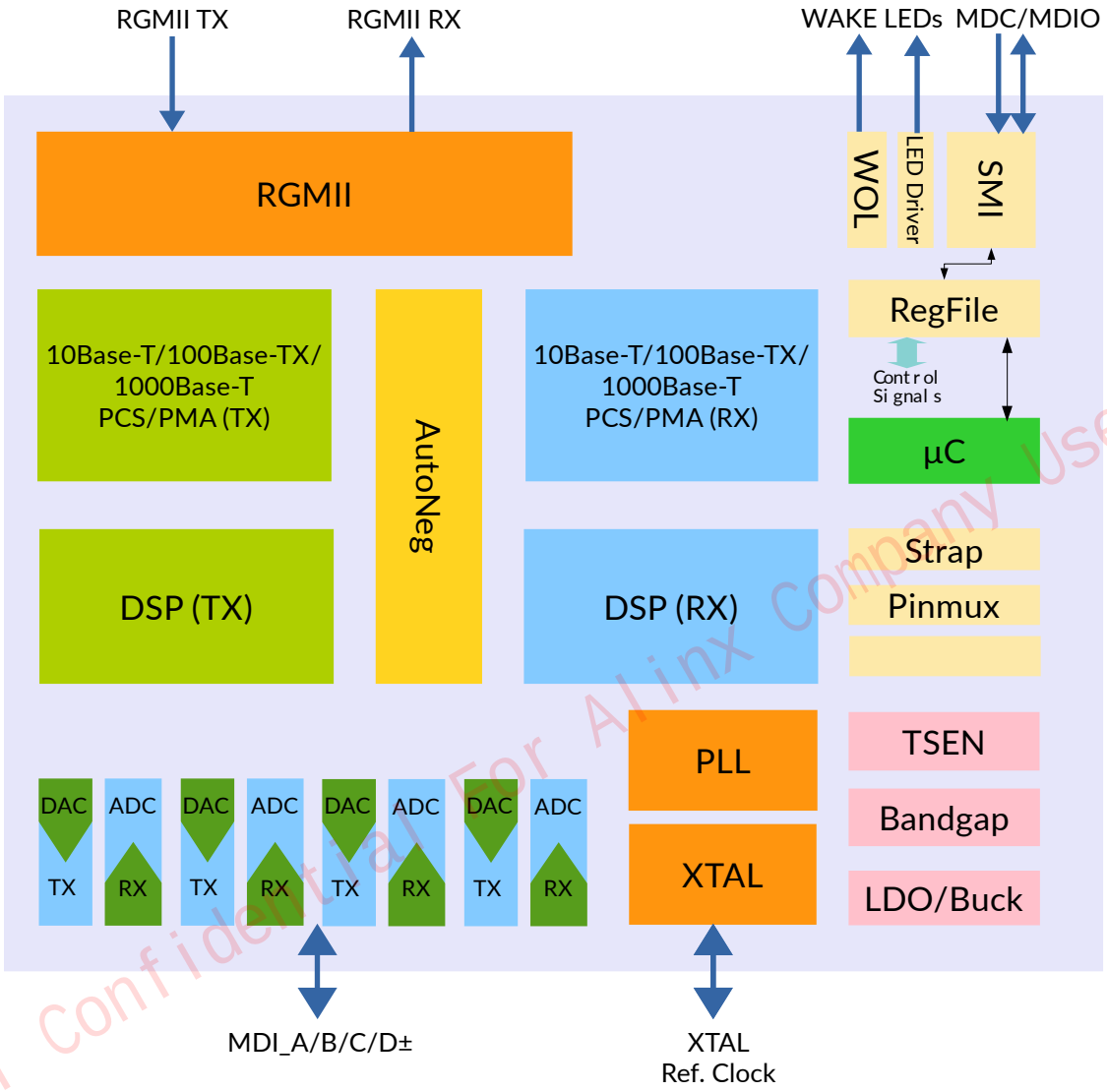


Figure 8. Functional Block Diagram

5.2. Feature Description

5.2.1. Transmitter (copper)

JL2121(D) utilizes D/A converter to transmit encoding digital signals onto the CAT.5 cable. An internal resistor termination provides good return loss performance and reduces BOM on PCB. Pulse shaping and slew rate control technology are used to eliminate EMI problem. The transmitted data are encoded in 4D-PAM5, 4B/5B and Manchester for 1000BASE-T, 100BASE-TX and 10BASE-T respectively.

5.2.2. Receiver (copper)

JL2121(D) utilizes a high speed and high-resolution A/D converter to receive channel signals, which guarantees far-beyond-standard receiving range. For 1000BASE-T, a hybrid analog front end is employed to reduce near-end echo, which allows transmitter and receiver to share one transformer. In digital domain, technologies as echo cancel, next cancel, baseline wander cancel and adaptive equalization are implemented.

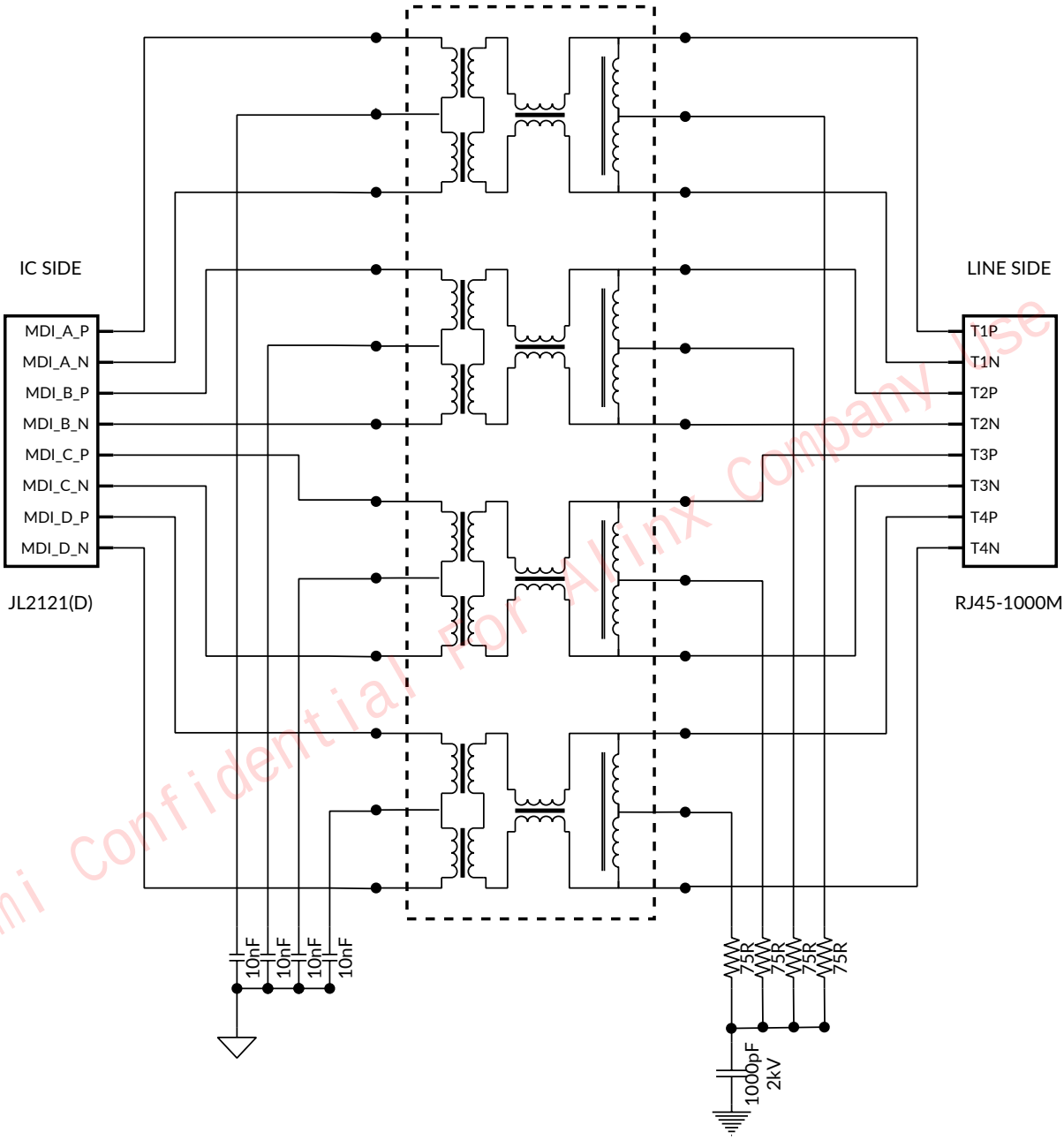


Figure 9. MDI Interface Reference Design

5.2.3. PTP

Precise Time Protocol (PTP) is used by IEEE specifications to determine the time of day for systems across a network. The IEEE specifications are IEEE 802.1AS, IEEE 1588 version 1, and IEEE 1588 version 2. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to time stamp the PTP frames with high precision as close to the physical wires as possible. As such, doing the time stamping in the PHY increases the accuracy compared to doing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

JL2121(D) supports Precision Time Protocol (PTP), which is defined in IEEE 802.1AS, IEEE 1588v1 and IEEE 1588v2.

The PTP core in the device consists of two sub-cores, namely the Packet Time Stamping and the Time Application Interface (TAI). The time stamping core supports time stamping of frame formats as defined in IEEE 802.1AS, IEEE 1588v1, and IEEE1588v2 frames.

For further details, refer to the "AN201-IEEE-1588-Functional" application notes.

PTP Control

To support the PTP Time Stamping function, the device has four pins that are global to the entire PHY.

- Interrupt pin (The PIN31_INTn is used for this purpose)

Time Application Interface (TAI)

The "Timing Interface Block" of TAI use two signals to offer various services, such as transport best clock information to whole PTP network point by PTP protocl. One signal is called EventRequest input signal and the second is called TriggerGenerate output signal.

Using the above signals there are several functions that this block supports:

- An event pulse capture function.
- Multiple event counter function.
- A trigger pulse generate function with pulse width control.
- A trigger clock generate function with digital clock compensation.
- A PTP global time increment and/or decrement function.
- A multi-ptp device time sync function.

Packet Time Stamping

JL2121(D) provides PTP packet parser which monitors transmit/received packet streams. When PTP event message packet is detected in the receiving path, PTP timestamp will be recorded. When PTP event message packet is detected in the transmitting path, PTP timestamp will be inserted in the packet.

ReadPlus Command

The PTP Global Time Registers are used as 32-bit global timer value that is running off of the free running PHY clock. A Read from the PTP Global Time Registers must be done with ReadPlus command. A Read directly to the PTP Global Time Registers without using ReadPlus command will return 0. The PTP Global Time Registers value can be loaded directly by writing back-to-back to the PTP Global Time 1 Register and PTP Colbal Time 0 Register.

5.2.4. WOL

Wake-On-LAN provides a mechanism to detect specific frames and notify the connected MAC through either a register status change or external pin level indication. Wake-on-LAN is implemented using a specially designed frame called a magic packet. When a qualifying WOL frame is received, the JL2121(D) WOL logic circuit is able to generate a user-defined event through external pins or a status interrupt flag to inform a connected controller that a wake event has occurred.

The Power Manange Event of WOL output pin (PIN31 INTn/PMEn) is an open drain output pin, so this pin needs to be connected with a 4.7kohm resistor and pulled up to 3.3V. When wakeup frame or magic packet is received, it will be pulled low by PHY to notify the system to wake up.

Magic Packet Structure

When configured for Wake-On-LAN mode, the JL2121(D) will check all incoming frames for identifying the Magic Packet frame. A Magic Packet frame must also meet the basic requirements for the Ethernet Frame.The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh.

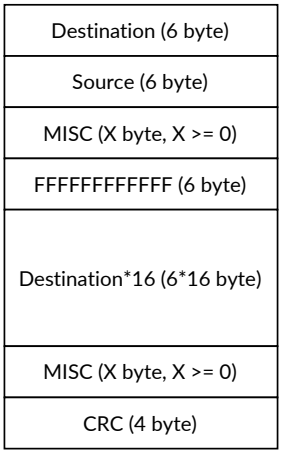


Figure 10. Magic Packet Structure

Register Mapping

Table 11. WOL Function Control Register (Page 0x12, Register 0x15)

Bits	Name	Type	Default	Description
[6]	WOL Function Enable	RW	0x0	WOL function golbal enable 1: Enable 0: Disable

Table 12. WOL Magic Packet Destination Address 2 (Page 0x1200, Register 0x11)

Bits	Name	Type	Default	Description
[15:0]	UNI PHY Addr 2	RW	0xFFFF	MAC_Address_DA[47:32]

Table 13. WOL Magic Packet Destination Address 1 (Page 0x1200, Register 0x12)

Bits	Name	Type	Default	Description
[15:0]	UNI PHY Addr 1	RW	0xFFFF	MAC_Address_DA[31:16]

Table 14. WOL Magic Packet Destination Address 0 (Page 0x1200, Register 0x13)

Bits	Name	Type	Default	Description
[15:0]	UNI PHY Addr 0	RW	0xFFFF	MAC_Address_DA[15:0]

Table 15. WOL Control and Status (Page 0x1200, Register 0x10)

Bits	Name	Type	Default	Description
[15]	WOL Disable	RW	0x1	WOL Control 1: Disable WOL 0: Enable WOL
[1]	WOL Level Clear	RW	0x0	WOL magic packet received event clear Write 1 and then 0 will clear this event
[0]	WOL Magic Packet Received	RO	0x0	WOL magic packet received event indicate

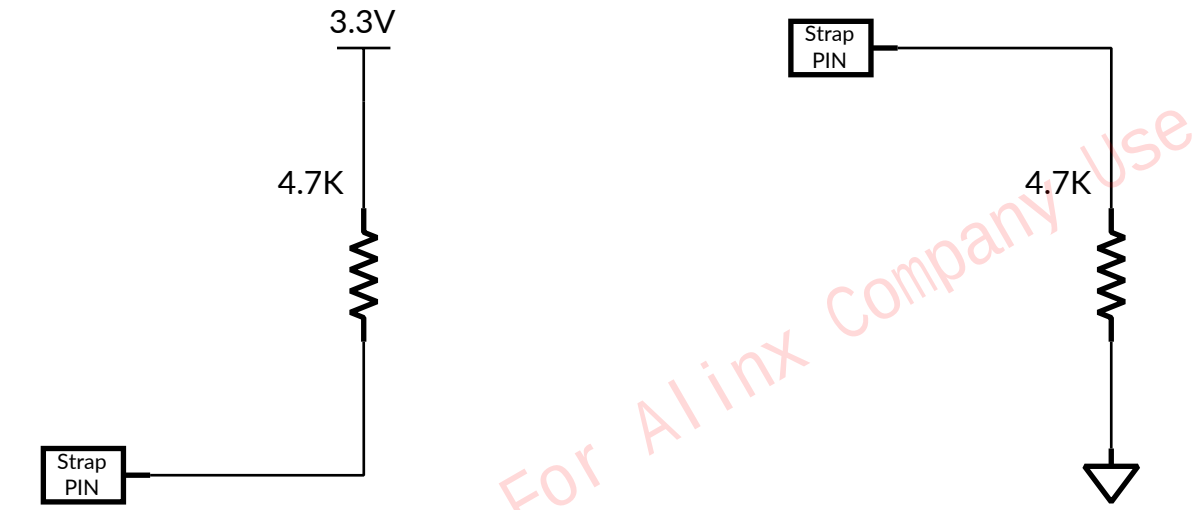
5.2.5. Hardware Configuration

JL2121(D) could be configured through hardware setting. These configurations are setup through pullup/pulldown resistor with dedicated IO pad. When power on reset is de-asserted, the hardware circuit will sample values on these dedicated IO. Those values will be used as hardware setting.

Table 16. JL2121(D) Hardware Config

Strap	Description
RXDLY	RGMII rx clock delay setting. 1: add 2ns delay to rgmii RX_CLK 0: no delay
TXDLY	RGMII tx clock delay setting. 1: add 2ns delay to rgmii TX_CLK 0: no delay

Strap	Description
ADR[2:0]	Set the PHY address for the device. It supports the PHY address from 0x0 to 0x7. The 0x0 is a broadcast address on default. This function can be disabled by setting MDIO config.
ENB_LDO	Control of internal LDO for IO supply: 1: disable internal LDO, external power supply is need. 0: enable internal LDO, LDO output is determined by strap V_SEL[1:0] (default).
V_SEL[1:0]	RGMII I/O Voltage selection: 00: external 3.3V 01: 2.5V 10: 1.8V(default)



Hardware configuration: Logic 1 Hardware configuration: Logic 0

Figure 11. Hardware Configuration Reference Design

5.2.6. Loopback

JL2121(D) supports various different loopback paths.

1000BASE-T/100BASE-TX/10BASE-T PCS Loopback

When BMCR (Page 0x0, Reg 0x0) bit[14] Loopback is set to 1, data sent through RGMII will route to PCS TX path. Then these data will route back to RGMII RX pad through PCS RX path.

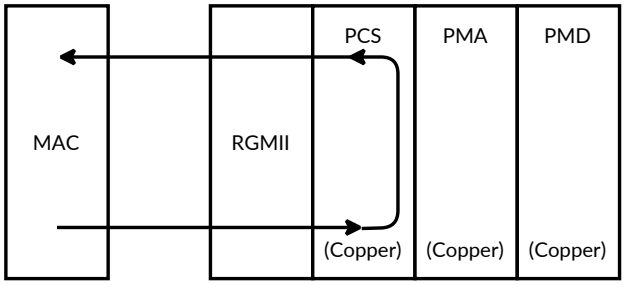


Figure 12. PCS Loopback

1000BASE-T/100BASE-TX/10BASE-T External Loopback

For production testing, an external loopback stub allows testing of the complete data path without the need of a link partner. For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, the given register configurations must be followed to enter the external loopback mode. All copper modes require an external loopback stub. The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in following Figures

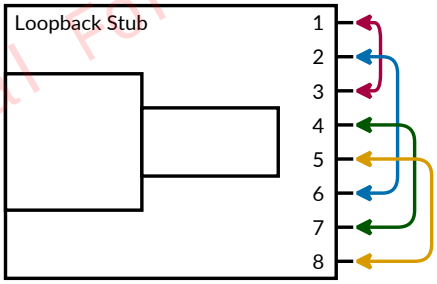


Figure 13. External Loopback Stub

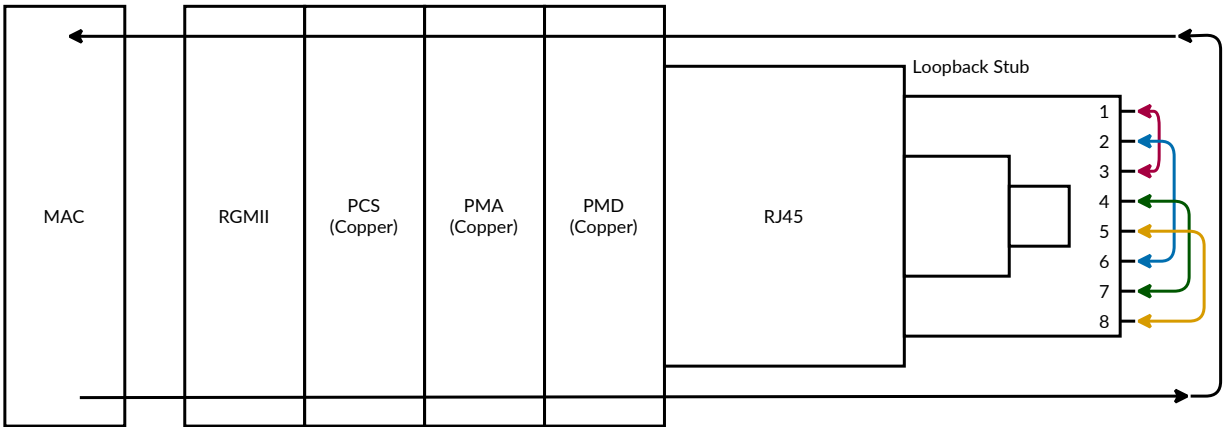


Figure 14. External Loopback Path

1000BASE-T PMD Loopback

PMD Loopback only support in 1000Base-T mode. It's allows testing of the complete data path without the need of a link partner and external loopback stub.

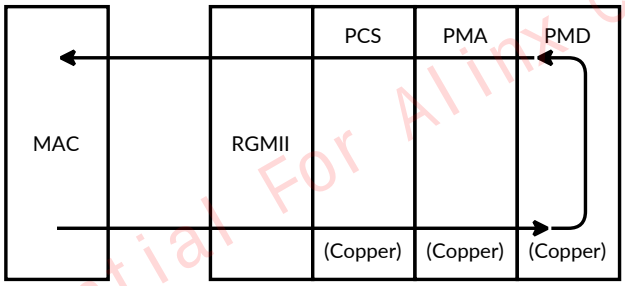


Figure 15. PMD Loopback

Register Mapping

Table 17. Basic Mode Control Register (Page 0x00, Register 0x00)

Bits	Name	Type	Default	Description
[14]	Loopback	RW	0x0	PCS Loopback Mode 1: Enable loopback mode 0: Disable loopback mode

Table 18. External/PMD Loopback for 1000BASE-T (Page 0x00, Register 0x14)

Bits	Name	Type	Default	Description
[2:1]	1000BASE-T Special Loopback Mode Select	RW	0x0	1000BASE-T External/PMD Loopback Mode Select 1: External stub loopback 0: PMD loopback

5.2.7. MAC/PHY interface

There are two different interfaces for MAC/PHY interface.

RGMII interface

JL2121(D) provides rgmii interface which compliant to RGMII 2.0. The interface provides 6 pads for TX path (i.e. txclk, tx_ctrl, txdata[3:0]) and 6 pads for RX path (i.e. rxclk, rx_ctrl, rx_data[3:0]). The interface works with 125MHz clock in 1000BaseT, or 25MHz in 100BaseTX or 2.5MHz in 10BaseT.

Figure 16. RGMII Interface Reference Design

5.2.8. Auto-Negotiation

JL2121(D) supports AN function which is definde in 802.3. The AN function implements crossover detection automatically for MDI/MDIX cables which easies connection process. The JL2121(D) also implements polarity auto correction when cable happens to have wrong polarity connected.

5.2.9. LED

JL2121(D) provides three LED pins for indicators. We can configure these pins to achieve several possible actions.

Duplex with Strap Pin

In order to reduce pin count, these LED pins LED[2:0] are also used as strap pin during power on reset, JL2121(D) will read these pins' strap value to determine RGMII IO Voltage. So we must select Pull-up or Pull-down for these pins according to the actual situation.

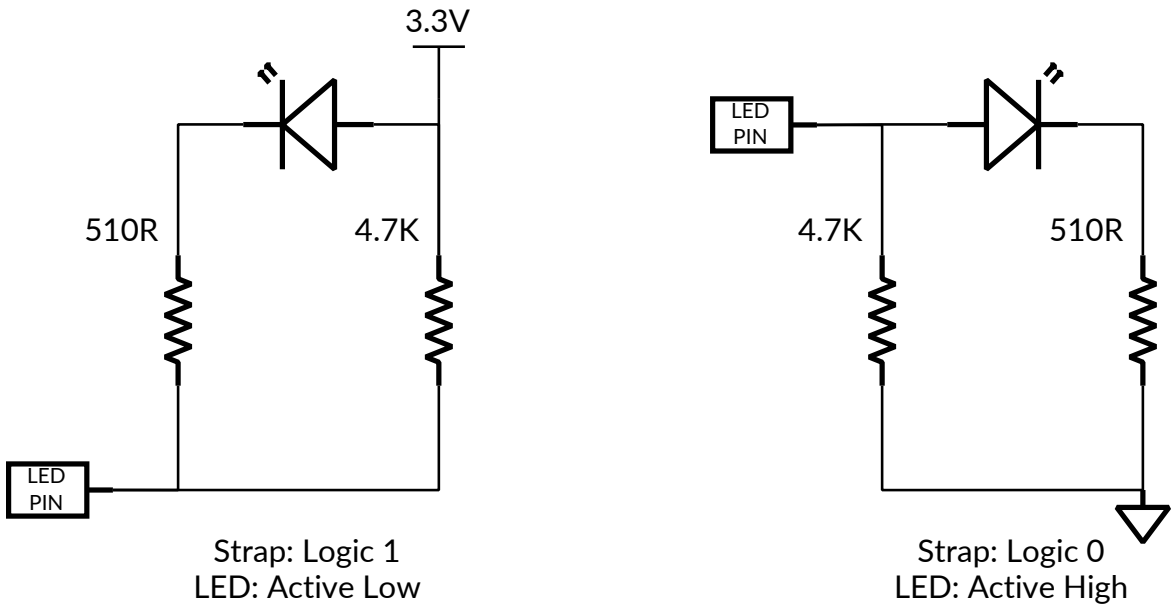


Figure 17. LED Duplex with Strap Reference Design

LED Mode Select Register

JL2121(D) provieds two mode, A mode and B mode, to select. Config LED Control Register bit 15 as 0(default) to select A mode, config bit 15 as 1 to select B mode.

LED Control Register

Each LED pin has its corresponding act and 10/100/1000 link configure registers.

Table 19. LED Control Register (Page 0xD04, Register 0x10, LCR)

Bits	Name	Default	Description
15	LED_MODE	0	0: LED Mode A is selected 1: LED Mode B is selected
14	LED2 Active	1	LED2 as active indication
13	LED2_LINK_1000	1	LED2 as link 1000Mbps indication
12	Reserved	0	Reserved
11	LED2_LINK_100	0	LED2 as link 100Mbps indication
10	LED2_LINK_10	0	LED2 as link 10Mbps indication
9	LED1 Active	1	LED1 as active indication
8	LED1_LINK_1000	0	LED1 as link 1000Mbps indication
7	Reserved	0	Reserved
6	LED1_LINK_100	1	LED1 as link 100Mbps indication
5	LED1_LINK_10	0	LED1 as link 10Mbps indication
4	LED0 Active	1	LED0 as active indication
3	LED0_LINK_1000	0	LED0 as link 1000Mbps indication

Bits	Name	Default	Description
2	Reserved	0	Reserved
1	LED0_LINK_100	0	LED0 as link 100Mbps indication
0	LED0_LINK_10	1	LED0 as link 10Mbps indication

LED Pin Application

Through configure LED Mode Select Register, we can customize these LED pins on A mode or B mode. Then through configure LED Control Register, we can customize each pin to indicate various link and active status.

Table 20. LED Mode A

Link_10	Link_100	Link_1000	Active	Description
0	0	0	0	Does not work
0	0	0	1	Does not work
0	0	1	0	Indicate link 1000Mbps
0	0	1	1	Indicate link 1000Mbps and active 1000Mbps
0	1	0	0	Indicate link 100Mbps
0	1	0	1	Indicate link 100Mbps and active 100Mbps
0	1	1	0	Indicate link 100Mbps or 1000Mbps
0	1	1	1	Indicate link 100Mbps or 1000Mbps and active 100Mbps or 1000Mbps
1	0	0	0	Indicate link 10Mbps
1	0	0	1	Indicate link 10Mbps and active 10Mbps
1	0	1	0	Indicate link 10Mbps or 1000Mbps
1	0	1	1	Indicate link 10Mbps or 1000Mbps and active 10Mbps or 1000Mbps
1	1	0	0	Indicate link 10Mbps or 100Mbps
1	1	0	1	Indicate link 10Mbps or 100Mbps and active 10Mbps or 100Mbps
1	1	1	0	Indicate link 10Mbps or 100Mbps or 1000Mbps
1	1	1	1	Indicate link 10Mbps or 100Mbps or 1000Mbps and active 10Mbps or 100Mbps or 1000Mbps

Table 21. LED Mode B

Link_10	Link_100	Link_1000	Active	Description
0	0	0	0	Does not work
0	0	0	1	Indicate active 10Mbps or 100Mbps or 1000Mbps
0	0	1	0	Indicate link 1000Mbps
0	0	1	1	Indicate link 1000Mbps and active 10Mpbs or 100Mbps or 1000Mbps
0	1	0	0	Indicate link 100Mbps
0	1	0	1	Indicate link 100Mbps and active 10Mpbs or 100Mbps or 1000Mbps
0	1	1	0	Indicate link 100Mbps or 1000Mbps

Link_10	Link_100	Link_1000	Active	Description
0	1	1	1	Indicate link 100Mbps or 1000Mbps and active 10Mpbs or 100Mbps or 1000Mbps
1	0	0	0	Indicate link 10Mbps
1	0	0	1	Indicate link 10Mbps and active 10Mpbs or 100Mbps or 1000Mbps
1	0	1	0	Indicate link 10Mbps or 1000Mbps
1	0	1	1	Indicate link 10Mbps or 1000Mbps and active 10Mpbs or 100Mbps or 1000Mbps
1	1	0	0	Indicate link 10Mbps or 100Mbps
1	1	0	1	Indicate link 10Mbps or 100Mbps and active 10Mpbs or 100Mbps or 1000Mbps
1	1	1	0	Indicate link 10Mbps or 100Mbps or 1000Mbps
1	1	1	1	Indicate link 10Mbps or 100Mbps or 1000Mbps and active 10Mbps or 100Mbps or 1000Mbps

5.2.10. Impedance calibration

RGMII interface IOs output impedance can be calibrated manually or automatically to further minimize PCB EMI.

5.2.11. Temperature sensor

JL2121(D) integrated a high-resolution internal temperature sensor.

5.2.12. Power

JL2121(D) supports both internal switching regulator and linear regulator. A 3.3V@1A steady power source is needed for IC normal working. To save power, JL2121 is preferred. To have better EMI performance, JL2121D is preferred.

The device supports 3.3/2.5(default)/1.8V IO voltage, which all can be supplied from either external or internal. If pull high ENB_LDO pin to disable internal LDO, IODVDD pin should be connected to the external power source for 3.3/2.5/1.8V. If pull low or float ENB_LDO pin to enable internal LDO, IODVDD pin should be connected to at least 0.1uF capacitor to GND, the IODVDD power value is according to V_SEL[1:0] configuration.

If V_SEL pin is floating, the V_SEL[1:0]=0b01 is the default value, the voltage of IODVDD would be equal 2.5V.

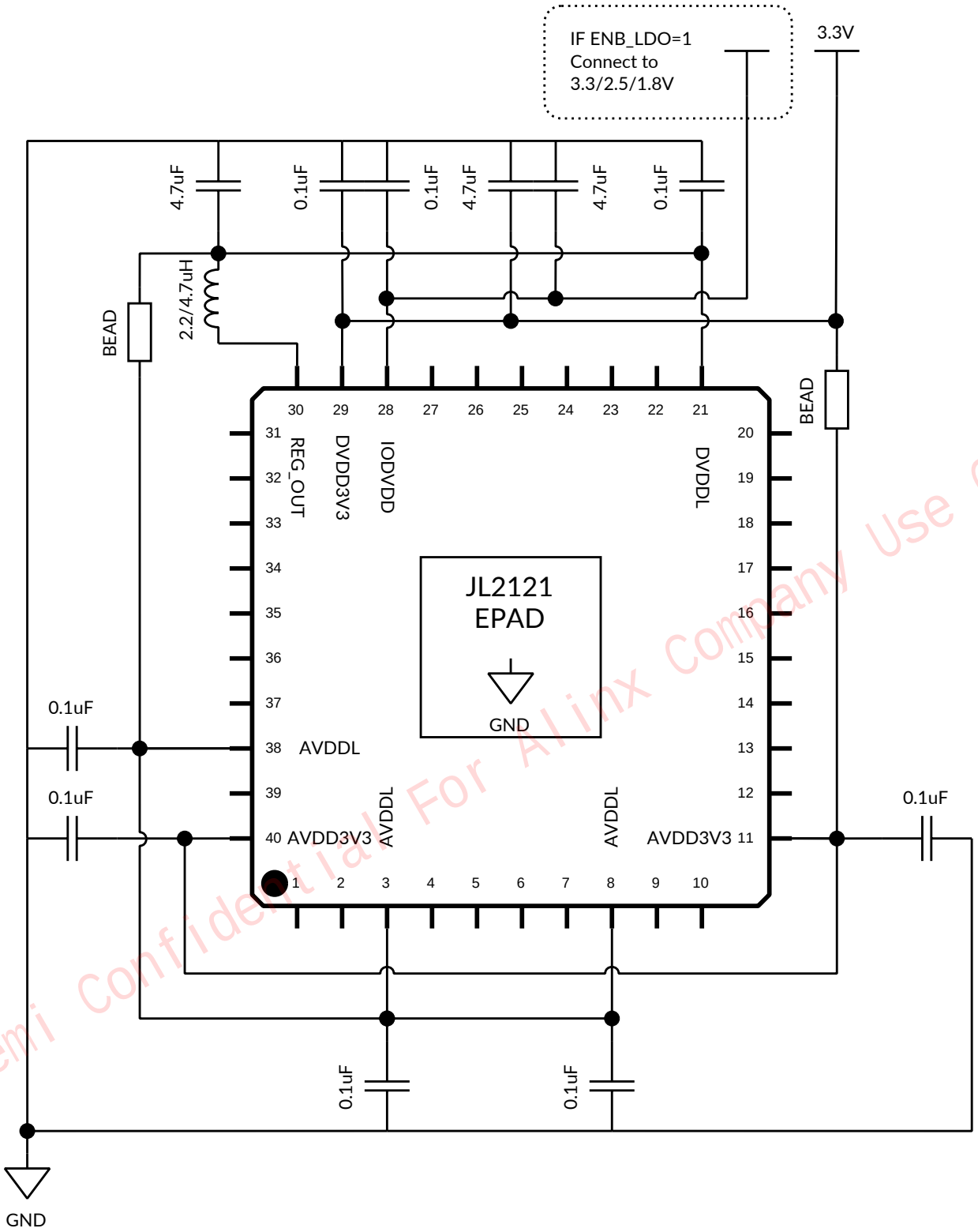


Figure 18. JL2121 Power Interface Reference Design

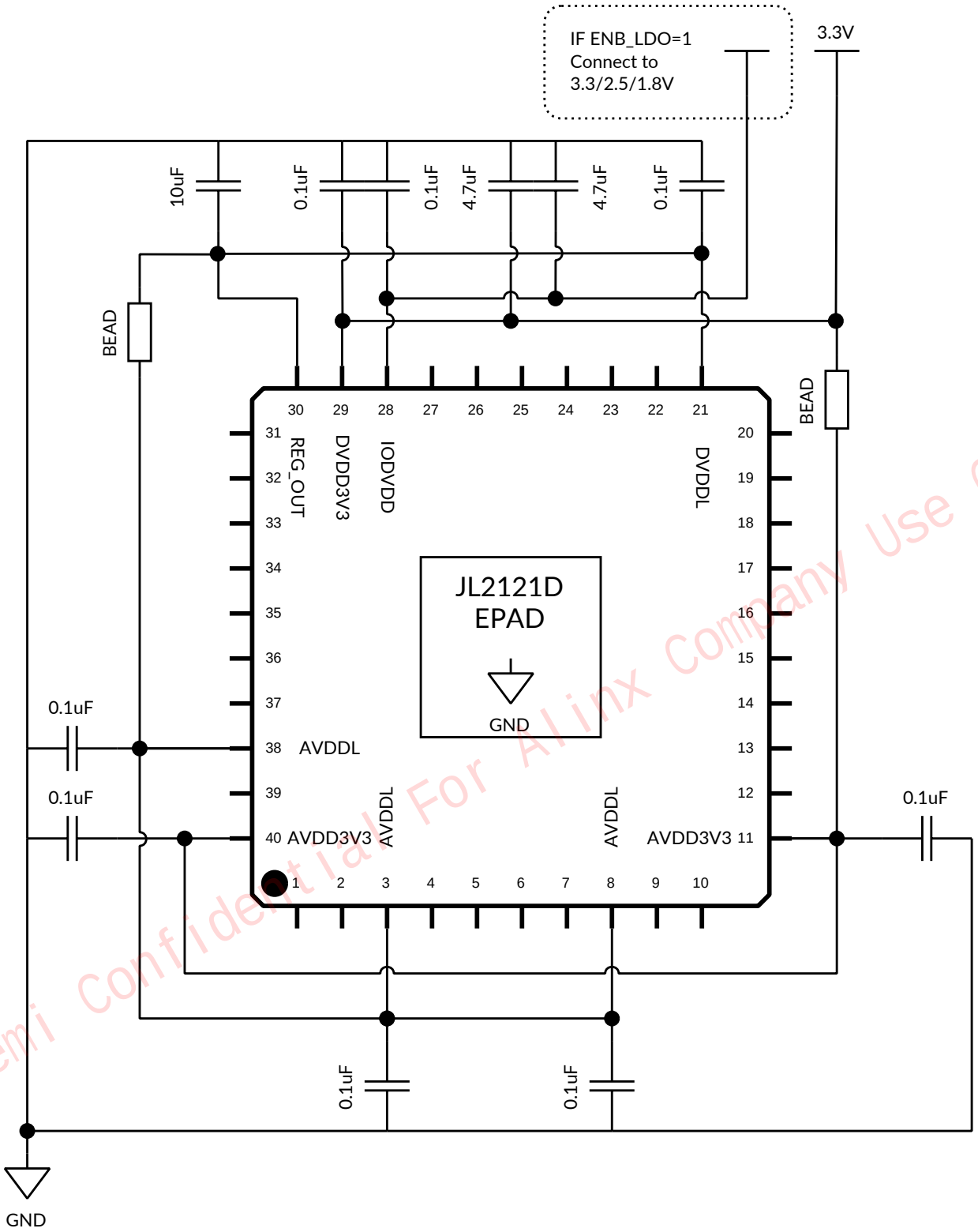


Figure 19. JL2121D Power Interface Reference Design

5.2.13. Clock

JL2121(D) can use crystal or oscillator as clock reference input. If use crystal, 25-MHz, parallel, 20pF load crystal is recommended. A typical connection diagram is shown below. The load capacitor values will vary with the crystal vendors for the recommended loads.

If use oscillator or other clock sources, according to the diagram, Left the XO pin floating if using XI as clock input pin.

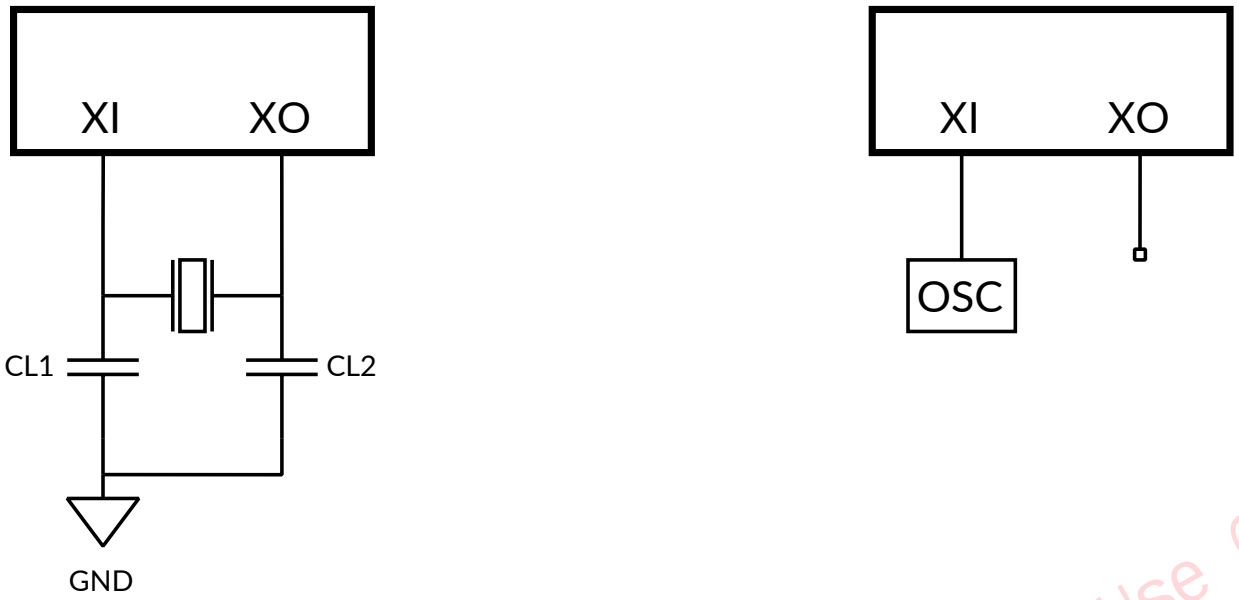


Figure 20. Clock Interface Reference Design

SyncE

JL2121(D) supports SyncE function. When this function is enabled, recovered 125MHz clock will be output through PIN35_CLOCKOUT pad.

5.2.14. Downshift

Sometimes there are existing cables that only have two-pairs, which are used to connect 10Mbps and 100Mbps ethernet PHYs, Gigabit link partners can auto-negotiate to 1000Mbps on this kinds of cable with only pairs 1-2 and pairs 3-6, but fail to link. Without "downshift" feature, the gigabit PHY will repeatedly pass auto-negotiate process and fail 1000Mbps link, never try to link at 10Mbps or 100Mbps.

With "downshift" feature, on this condition, JL2121(D) is able to auto-negotiate with another gigabit link partner by downshift and link at 10Mbps or 100Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In another cases, the cable is too terrible to work at 1000Mbps, PHY captures error bits continually, the "downshift" feature will also be effective as two-pair cables condition.

By default, the downshift feature is turned off. Refer to PHY_CTRL_1 register on page=0x00 reg=0x11 which describe how to enable and control the downshift feature.

To enable the downshift feature, the following registers must be set:

- PHY_CTRL_1[13] = 1 to enable smart downshift, recommend to always enable this feature with downshift global enable together
- PHY_CTRL_1[14] = 1 to enable two wire detection, if want to downshift on using two-wire cable condition

- PHY_CTRL_1[15] = 1 to enable an error detection, if want to downshift on using terrible cable condition
- PHY_CTRL_1[9:5] = 12 to determine downshift silent counter this value means the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed.
- PHY_CTRL_1[4:0] = 3 to determine downshift an error counter this value means the number of error times captured by PHY before the PHY downshifts to the next highest speed.
- PHY_CTRL_1[12] = 1 to globle enable downshift featuer after all of above registers is ready

Chapter 6. Register Descriptions

6.1. Register Type

RW:	Read and Write	SC:	Software Reset Clear
RO:	Read Only	RC:	Read Clear

6.2. Register Map

Table 22. Register Map

Page	Register	Tag	Desc
0x0	0x0	BMCR	Basic Mode Control Register (Page 0x00, Register 0x00, BMCR)
0x0	0x1	BMSR	Basic Mode Status Register (Page 0x00, Register 0x01, BMSR)
0x0	0x2	PHYID1	PHY Identifier Register 1 (Page 0x00, Register 0x02, PHYID1)
0x0	0x3	PHYID2	PHY Identifier Register 2 (Page 0x00, Register 0x03, PHYID2)
0x0	0x4	ANAR	Auto-Negotiation Advertisement Register (Page 0x00, Register 0x04, ANAR)
0x0	0x5	ANLPAR	Auto-Negotiation Link Partner Ability Register (Page 0x00, Register 0x05, ANLPAR)
0x0	0x6	ANER	Auto-Negotiation Expansion Register (Page 0x00, Register 0x06, ANER)
0x0	0x7	ANNPTR	Auto-Negotiation Next Page Transmit Register (Page 0x00, Register 0x07, ANNPTR)
0x0	0x8	ANNPRR	IEEE Auto-Negotiation Next Page Receive Register (Page 0x00, Register 0x08, ANNPRR)
0x0	0x9	GBCR	1000BASE-T Control Register (Page 0x00, Register 0x09, GBCR)
0x0	0xA	GBSR	1000BASE-T Status Register (Page 0x00, Register 0x0A, GBSR)
0x0	0xF	GBESR	1000BASE-T Extended Status Register (Page 0x00, Register 0x0F, GBESR)
0x0	0x11	PHY_CTRL_1	PHY Control Register 1 (Page 0x00, Register 0x11, PHY_CTRL_1)
0xA43	0x18	PHYCR1	PHY Specific Control Register 1 (Page 0xA43, Register 0x18, PHYCR1)
0xA43	0x19	PHYCR2	PHY Specific Control Register 2 (Page 0xA43, Register 0x19, PHYCR2)
0xA43	0x1A	PHYSR	PHY Specific Status Register (Page 0xA43, Register 0x1A, PHYSR)
0xD04	0x10	LCR	LED Control Register (Page 0xD04, Register 0x10, LCR)
0x0	0x1F	PAGSR	Page Select Register (Register 0x1F, PAGSR)

6.3. Basic Mode Control Register (Page 0x00, Register 0x00, BMCR)

Bits	Name	Type	Default	Description
15	Reset	RW, SC	0	Reset. 1: PHY reset 0: Normal operation This bit is SC (self clear) type, after a software reset this bit will restore to 0. Register 0 (BMCR) and register 1 (BMSR) will restore to default values after a software reset (set Bit15 to 1). This action may change the internal PHY state and the state of the physical link associated with the PHY. After software reset, need to delay 10ms de-assert time for chip steady.
14	Loopback	RW	0	Loopback Mode. 1: Enable loopback mode 0: Disable loopback mode
13	Speed Selection (LSB)	RW	0	Speed Select Bit 0. In forced mode, when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection. Speed[1] Speed[0]: Speed Enabled 1 1: Reserved 1 0: 1000Mbps 0 1: 100Mbps 0 0: 10Mbps
12	Auto-Negotiation Enable	RW	1	Auto-Negotiation Enable. 1: Enable Auto-Negotiation process 0: Disable Auto-Negotiation process
11	Power Down	RW	0	Power Down. 1: Power down (only Management Interface and logic are active; link is down) 0: Normal operation
10	Isolate	RW	0	Isolate. 1: Electrically isolate PHY from MII or GMII; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, PHY ignores TXD[7:0], and TXCLT inputs, and presents a high impedance on TXC, RXC, RXCLT, RXD[7:0]. 0: Normal operation
9	Restart Auto-Negotiation	RW, SC	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation process 0: Normal operation This bit is SC (self clear) type, after a auto-negotiation restart this bit will restore to 0.
8	Duplex Mode	RW	1	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode, i.e., NWay is disabled.
7	Collision Test	RW	0	Collision Test. 1: Enable COL signal test 0: Disable COL signal test

Bits	Name	Type	Default	Description
6	Speed Selection (MSB)	RW	1	Speed Select Bit 1. In forced mode, when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection. Speed[1] Speed[0]: Speed Enabled 1 1: Reserved 1 0: 1000Mbps 0 1: 100Mbps 0 0: 10Mbps
5:0	Reserved	RW	0b000000	Reserved.

6.4. Basic Mode Status Register (Page 0x00, Register 0x01, BMSR)

Bits	Name	Type	Default	Description
15	100BASE-T4	RO	0	100BASE-T4 Capability. 1: PHY able to perform 100BASE-T4 0: PHY not able to perform 100BASE-T4 This bit should always be 0.
14	100BASE-X Full Duplex	RO	1	100BASE-X Full Duplex Capability. 1: PHY able to perform full duplex 100BASE-X 0: PHY not able to perform full duplex 100BASE-X This bit should always be 1.
13	100BASE-X Half Duplex	RO	1	100BASE-X Half Duplex Capability. 1: PHY able to perform half duplex 100BASE-X 0: PHY not able to perform half duplex 100BASE-X This bit should always be 1.
12	10BASE-T Full Duplex	RO	1	10BASE-T Full Duplex Capability. 1: PHY able to operate at 10BASE-T in full duplex mode 0: PHY not able to operate at 10BASE-T in full duplex mode This bit should always be 1.
11	10BASE-T Half Duplex	RO	1	10BASE-T Half Duplex Capability. 1: PHY able to operate at 10BASE-T in half duplex mode 0: PHY not able to operate at 10BASE-T in half duplex mode This bit should always be 1.
10	100BASE-T2 Full Duplex	RO	0	10Base-T2 Full Duplex Capability. 1: PHY able to perform full duplex 100BASE-T2 0: PHY not able to perform full duplex 100BASE-T2 This bit should always be 0.
9	100BASE-T2 Half Duplex	RO	0	10Base-T2 Half Duplex Capability. 1: PHY able to perform half duplex 100BASE-T2 0: PHY not able to perform half duplex 100BASE-T2 This bit should always be 0.
8	Extended Status	RO	1	1000Base-T Extended Status Register. 1: Extended status information in Register 0x0F (15) 0: No extended status information in Register 0x0F (15) This bit should always be 1.
7	Reserved	RO	0	Reserved.

Bits	Name	Type	Default	Description
6	MF Preamble Suppression	RO	1	Preamble Suppression Capability (Permanently On). 1: PHY will accept management frames with preamble suppressed 0: PHY will not accept management frames with preamble suppressed This bit should always be 1.
5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
4	Remote Fault	RC	0	Remote Fault. 1: Remote fault condition detected 0: No remote fault condition detected
3	Auto-Negotiation Ability	RO	1	Auto-Negotiation Ability. 1: PHY is able to perform Auto-Negotiation 0: PHY is not able to perform Auto-Negotiation This bit should always be 1.
2	Link Status	RO	0	Link Status. 1: Link is up 0: Link is down
1	Jabber Detect	RO	0	Jabber Detect. 1: Jabber condition detected 0: No jabber condition detected
0	Extended Capability	RO	1	Extended Capability. 1: Extended register capabilities 0: Basic register set capabilities only This bit should always be 1.

6.5. PHY Identifier Register 1 (Page 0x00, Register 0x02, PHYID1)

Bits	Name	Type	Default	Description
15:0	OUI (MSB)	RO	0x937c	Organizationally Unique Identifier bits 3:18. JLSemi OUI is 0x24DF10 0010 0100 1101 1111 0001 0000 bit1.....bit24 Register 2.[15:0] show bits 3 to 18 of OUI 1001 0011 0111 1100 bit3.....bit18

6.6. PHY Identifier Register 2 (Page 0x00, Register 0x03, PHYID2)

Bits	Name	Type	Default	Description
15:10	OUI (LSB)	RO	Always 010000	Organizationally Unique Identifier bits 19:24. 01 0000 bit19...bit24
9:4	Model Number	RO	Always 000011	Manufacture's model number
3:0	Revision Number	RO	See Description	Contact JLSemi FAEs for information on the device revision number

6.7. Auto-Negotiation Advertisement Register (Page 0x00, Register 0x04, ANAR)

Bits	Name	Type	Default	Description
15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
14	Reserved	RW	0	Reserved
13	Remote Fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
12	Reserved	RW	0	Reserved
11	Asymmetric PAUSE	RW	0	1: Advertise asymmetric pause support 0: No support of asymmetric pause
10	Pause	RW	1	1: Advertise support of pause frames 0: No support of pause frames
9	100BASE-T4	RW	0	1: 100BASE-T4 is supported by local node 0: 100BASE-T4 not supported by local node
8	100BASE-TX Full Duplex	RW	1	1: 100BASE-TX full duplex is supported by local node 0: 100BASE-TX full duplex not supported by local node
7	100BASE-TX Half Duplex	RW	1	1: 100BASE-TX half duplex is supported by local node 0: 100BASE-TX half duplex not supported by local node
6	10BASE-T Full Duplex	RW	1	1: 10BASE-T full duplex is supported by local node 0: 10BASE-T full duplex not supported by local node
5	10BASE-T Half Duplex	RW	1	1: 10BASE-T half duplex is supported by local node 0: 10BASE-T half duplex not supported by local node
4:0	Selector Field	RO	0b00001	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.

6.8. Auto-Negotiation Link Partner Ability Register (Page 0x00, Register 0x05, ANLPAR)

Bits	Name	Type	Default	Description
15	Next Page	RO	0	Next Page Indication.
14	ACK	RO	0	Acknowledge.
13	Remote Fault	RO	0	Remote Fault indicated by Link Partner.
12	Reserved	RO	0	Reserved.
11:5	Technology Ability Field	RO	0b0000000	
4:0	Selector Field	RO	0b00000	

6.9. Auto-Negotiation Expansion Register (Page 0x00, Register 0x06, ANER)

Bits	Name	Type	Default	Description
15:5	Reserved	RW	0b0000000000	Reserved.
4	Parallel Detection Fault	RC	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function

Bits	Name	Type	Default	Description
3	Link Partner Next Pageable	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
2	Local Next Pageable	RO	1	1: Local Device is able to send Next Page This bit should always be 1.
1	Page Received	RC	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
0	Link Partner Auto-Negotiation capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

6.10. Auto-Negotiation Next Page Transmit Register (Page 0x00, Register 0x07, ANNPTR)

Bits	Name	Type	Default	Description
15	Next Page	RW	0	Next Page Indication. 1: More next pages to send 0: No more next pages to send Transmit Code Word Bit 15.
14	Reserved	RO	0	Reserved.
13	Message Page	RW	1	Message Page. 1: Message Page 0: Unformatted Page Transmit Code Word Bit 13.
12	Acknowledge 2	RW	0	Acknowledge2. 1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received Transmit Code Word Bit 12.
11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
10:0	Message/Unformatted Field	RW	0b00000000001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

6.11. IEEE Auto-Negotiation Next Page Receive Register (Page 0x00, Register 0x08, ANNPRR)

Bits	Name	Type	Default	Description
15	Next Page	RO	0	Received Link Code Word Bit 15.
14	Acknowledge	RO	0	Received Link Code Word Bit 14.
13	Message Page	RO	0	Received Link Code Word Bit 13.
12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
11	Toggle	RO	0	Received Link Code Word Bit 11.
10:0	Message/Unformatted Field	RO	0b00000000001	Received Link Code Word Bit 10:0.

6.12. 1000BASE-T Control Register (Page 0x00, Register 0x09, GBCR)

Bits	Name	Type	Default	Description
15:13	Test Mode	RW	0b000	Test Mode Select. 000: Normal Mode 001: Test Mode 1 - Transmit Jitter Test 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved
12	MASTER/SLAVE Manual Configuration Enable	RW	0	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
10	Port Type	RW	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)
9	1000BASE-T Full Duplex	RW	1	Advertise 1000BASE-T Full-Duplex Capability. 1: Advertise 0: Do not advertise
8	Reserved	RW	0	Reserved.
7:0	Reserved	RW	0x00	Reserved.

6.13. 1000BASE-T Status Register (Page 0x00, Register 0x0A, GBSR)

Bits	Name	Type	Default	Description
15	MASTER/SLAVE Configuration Fault	RC	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
13:12	Reserved	RO	0b00	Reserved.
11	Link Partner 1000BASE-T Full Duplex Capability	RO	0	Link Partner 1000BASE-T Full Duplex Capability. 1: Link Partner is capable of 1000BASE-T full duplex 0: Link Partner is not capable of 1000BASE-T full duplex
10	Link Partner 1000BASE-T Half Duplex Capability	RO	0	Link Partner 1000BASE-T Half Duplex Capability. 1: Link Partner is capable of 1000BASE-T half duplex 0: Link Partner is not capable of 1000BASE-T half duplex
9:8	Reserved	RO	0b00	Reserved.
7:0	Reserved	RO	0x00	Reserved

6.14. 1000BASE-T Extended Status Register (Page 0x00, Register 0x0F, GBESR)

Bits	Name	Type	Default	Description
15	1000BASE-X Full Duplex	RO	0	1: PHY able to perform full duplex 1000BASE-X 0: PHY not able to perform full duplex 1000BASE-X
14	1000BASE-X Half Duplex	RO	0	1: PHY able to perform half duplex 1000BASE-X 0: PHY not able to perform half duplex 1000BASE-X
13	1000BASE-T Full Duplex	RO	1	1: PHY able to perform full duplex 1000BASE-T 0: PHY not able to perform full duplex 1000BASE-T
12	1000BASE-T Half Duplex	RO	1	1: PHY able to perform half duplex 1000BASE-T 0: PHY not able to perform half duplex 1000BASE-T
11:0	Reserved	RO	0x000	Reserved.

6.15. PHY Control Register 1 (Page 0x00, Register 0x11, PHY_CTRL_1)

Bits	Name	Type	Default	Description
15	Downshift An Error Detection	RW	0	Turn on an error detection. 1: Enable an error detection 0: Disable an error detection
14	Downshift Two Wire Detection	RW	0	Turn on two wire detection. 1: Enable two wire detection 0: Disable two wire detection
13	Downshift Smart Enable	RW	0	Turn on smart donwshift, recommend always turn on this feature. 1: Enable smart downshift 0: Disable smart downshift
12	Downshift Enable	RW	0	Turn on downshift, global control. 1: Enable downshift 0: Disable downshift
11		RW	0	
10		RW	0	
9:5	Downshift Silent Counter	RW	0b00000	This value is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. Typicall, this value should not less than 11.
4:0	Downshift An Error Counter	RW	0b00000	This value is the number of error times captured by PHY before the PHY downshifts to the next highest speed. Legal value is from 1 to 31.

6.16. PHY Specific Control Register 1 (Page 0xA43, Register 0x18, PHYCR1)

Bits	Name	Type	Default	Description
15:14	Reserved	RO	0b00	Reserved
13:10	Reserved	RO	0x0	Reserved
9	MDI Mode Manual Configuration Enable	RW	0	1: Enable MDI mode manual configuration 0: Disable MDI mode manual configuration

Bits	Name	Type	Default	Description
8	MDI Mode	RW	0	Select MDI or MDIX mode 1: MDI 0: MDIX This bit is valid only when MID mode manual configuration is enable (Set the PHYCR1[9] to 1)
7:0	Reserved	RO	0x00	Reserved

6.17. PHY Specific Control Register 2 (Page 0xA43, Register 0x19, PHYCR2)

Bits	Name	Type	Default	Description
15:14	Reserved	RO	0b00	Reserved.
13:12	CLKOUT Source	RW	0b00	Select the clock source for CLKOUT pin output 00: Generated from internal PLL 01: Recovery from UTP receive clock for sync ethernet (Valid olny in UTP mode) Need assert a software reset (set BMCR[0] to 1) to effect the change of clock source.
11	CLKOUT Frequency Select	RW	0	Select the clock frequency for CLKOUT pin output 1: 125MHz 0: 25MHz
4:10	Reserved	RO	0b0000000	Reserved.
3	SYSCLK SSC Enable	RW	0	1: Enable SSC on system clock 0: Disable SSC on system clock SSC is Spread Spectrum Clocking function to reduce EMI radio
2:1	Reserved	RW	0b00	Reserved.
0	CLKOUT Enable	RW	1	1: Enable CLKOUT pin to output clock 0: Disable CLKOUT pin to output clock

6.18. PHY Specific Status Register (Page 0xA43, Register 0x1A, PHYSR)

Bits	Name	Type	Default	Description
15:13	Reserved	RO	0b000	Reserved.
12	Nway Enable	RO	0	1: Auto-Negotiation (NWay) is enabled 0: Auto-Negotiation (NWay) is disabled
11	Master Enable	RO	0	1: Device is in Master Mode 0: Device is in Slave Mode
6:10	Reserved	RO	0b00000	Reserved.
5:4	Speed Status	RO	0b00	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
3	Duplex Status	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex

Bits	Name	Type	Default	Description
2	Link Status	RO	0	Real Time Link Status. 1: Link OK 0: Link not OK
1	MDI Crossover Status	RO	0	MDI/MDI Crossover Status. 1: MDI 0: MDI Crossover
0	Reserved	RO	0	Reserved.

6.19. LED Control Register (Page 0xD04, Register 0x10, LCR)

Bits	Name	Type	Default	Description
15	LED_MODE	RW	0	0: LED Mode A is selected 1: LED Mode B is selected
14	LED2 Active	RW	1	LED2 active indication
13	LED2_LINK_1000	RW	1	1000Mbps LED2 link indication
12	Reserved	RO	0	Reserved.
11	LED2_LINK_100	RW	0	100Mbps LED2 link indication
10	LED2_LINK_10	RW	0	10Mbps LED2 link indication
9	LED1 Active	RW	1	LED1 active indication
8	LED1_LINK_1000	RW	0	1000Mbps LED1 link indication
7	Reserved	RO	0	Reserved.
6	LED1_LINK_100	RW	1	100Mbps LED1 link indication
5	LED1_LINK_10	RW	0	10Mbps LED1 link indication
4	LED0 Active	RW	1	LED0 active indication
3	led0_link_1000	RW	0	1000Mbps LED0 link indication
2	Reserved	RO	0	Reserved.
1	led0_link_100	RW	0	100Mbps LED0 link indication
0	led0_link_10	RW	1	10Mbps LED0 link indication

6.20. Page Select Register (Register 0x1F, PAGSR)

Bits	Name	Type	Default	Description
15:0	PageSel	RW	0x0000	Page select (HEX)

Chapter 7. Design Guide

7.1. Layout Guide

7.1.1. Stack-up

In order to reduce the reflection of high speed signals, the impedance of the signal trace routed in PCB should be matched from source to sink. To meet this requirement, at least Four-Layer PCB is recommended. Below stack-up is for reference.

Stackup(4 Layer)	
soldermask	20um
L1(High Speed Signal)	43um
PP	112um
GND02	18um
CORE	1180um
Power03	18um
PP	112um
L4(High Speed Signal)	43um
soldermask	20um
Total: 1600um	

In this stack-up, high speed signal is preferential to route in top Layer compared to bottom layer for the signal have a direct reference to the ground layer. If it is desirable to route high speed signal in bottom layer, Layout engineer can swap the usage of ground and power on layer 2 and 3.

7.1.2. Power Supply

REG_OUT pin is the output power pin of JL2121.Trace from it should be as wide as possible, and the length of the trace should be less than 200mil.

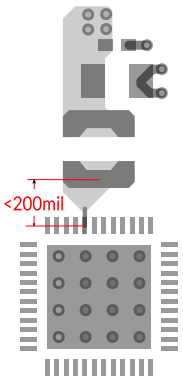


Figure 21. REG_OUT Pin PCB Design

For each power supply pin of IC, it is better to place a individual bypass capacitor as close as possible. Keep the trace short and wide. It is preferable that the current first passes the bypass capacitor and then enters the supply pin. The value of decoupling capacitors are suggested to be 0.1uF for each power pin, and one 4.7uF capacitor for whole chip.

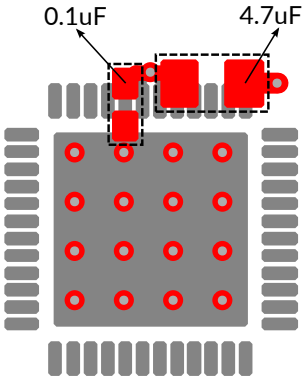


Figure 22. Power Decouple Design

Pay attention to the integrity of power and ground planes. Sometimes, the voids signal vias caused in these planes may lead to current density increasing. These areas are also called hot spots. It is important to arrange the place of the vias to avoid these hot spots. Often a good approach is to place the vias in a grid that leaves enough space between the vias for the power plane to pass.

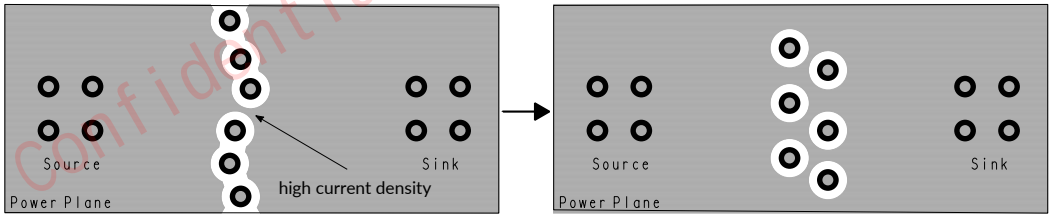


Figure 23. Avoid Copper Plane Hot Spots

7.1.3. Signal Trace

RGMII Signals

RGMII traces impedance need to be controlled to 50ohm. RXC and TXC traces which transmit 125MHZ signals should follow 3W standard, space of wire more than triple wire width. Traces length of RX signals group should be matched within +/-100mils, TX signals group is also like this. All the RGMII signals must refer to an complete plane.

7.1.4. General Guidlines of Routing

Impedance

High speed signal traces are required to control impedance. The value is 50Ω for single-ended and 100Ω for differential, without specially mentioned. Impedance discontinuities will cause reflection leading to emissions and signal integrity issues, for example, crosstalk, ringing...

Recording to the result of simulation with 3D field tools, via introduce a huge discontinuity of impedance. So reduce the amount of placed vias as possible.

Return Path

The return path of current will always follow the least impedance path. In lower frequency conditions, this means the path is least resistance path; in high frequency conditions, this means the path is least inductance path. The least inductance path is in the plane directly underneath the signal trace, since the area of the signal travel loop is smallest.So a solid unbroken reference plane is vital for meeting the requirements for signal transmission. Without a complete reference plane design,the current loop as shown in below figure will cause serious problems of signal integrity and EMC, EMI. This loop will generate unwanted emissions which transmit cross-talk to other signal traces, this condition maybe cause logic error.

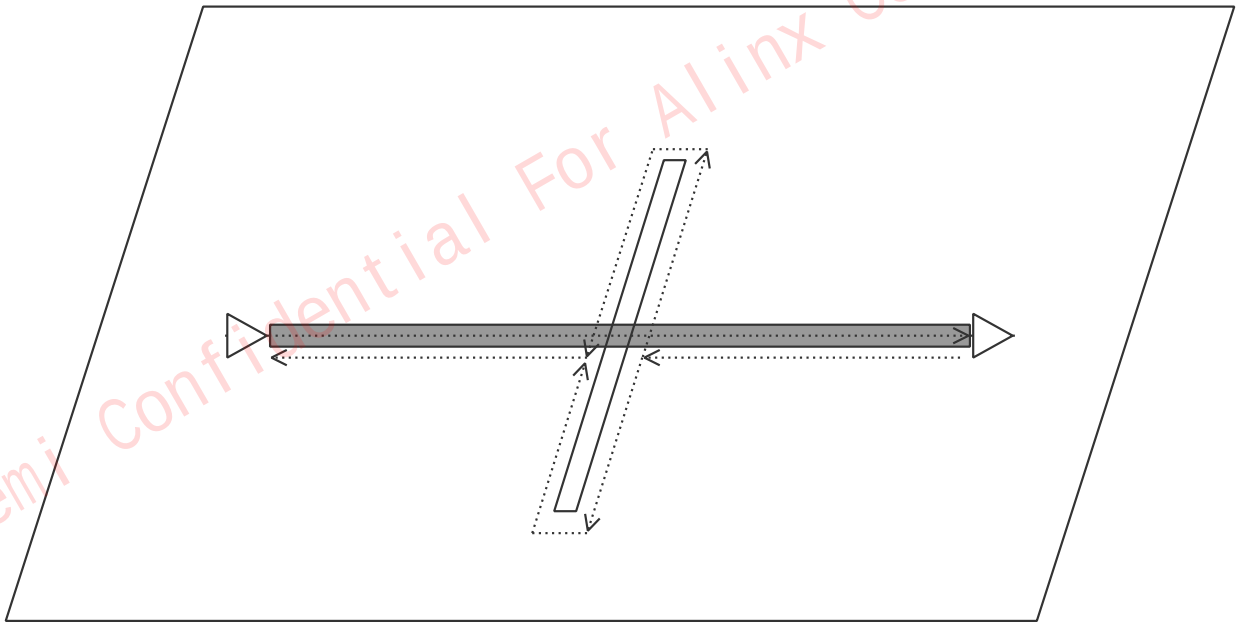


Figure 24. Slot in Reference Plane

Stub

Long stub traces can act as antennas and therefore increase problems complying with EMC standards. Stub traces can also produce reflections which negatively impacts signal integrity. Common sources for stubs are pull-up or pull-down resistors on high speed signals. If such resistors are required, route the signals as a daisy chain.

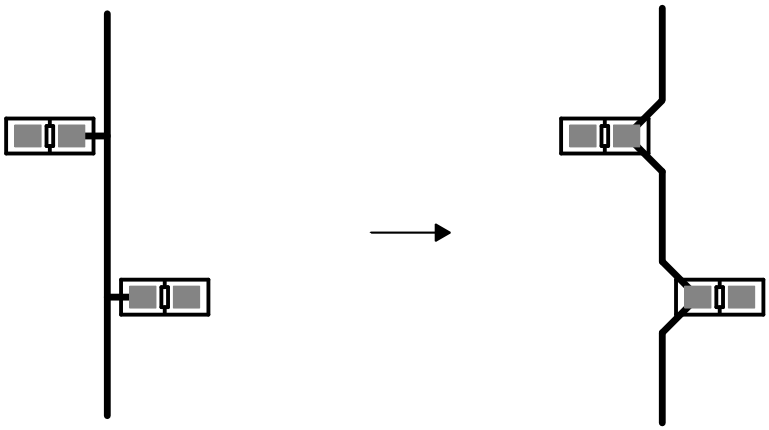


Figure 25. Avoid Stub Traces by Daisy Chain Routing

Length match

High speed interface need to match the length of signal trace. For example, in a high speed parallel bus, all data signals need to arrive within a time period in order to meet the setup and hold time requirements of the receiver. Length matching is also important for MAC interface (MII,RMII,GMII,RGMII..) connections. All transmit signal traces should be length matched to each other and all receive signal traces should be length matched to each other.

Differential pairs

Differential pair signals need to be routed in parallel with a same width and a same specific, constant distance between the two traces. This width and distance is required in order to obtain the specified differential impedance. Differential pair signals often require a very tight delay skew between the positive and negative signal traces. In other word, the length of positive and negative signal traces need to be matched. When using serpentine to compensate length differences, it is better to choose starting in the place which differences occur.

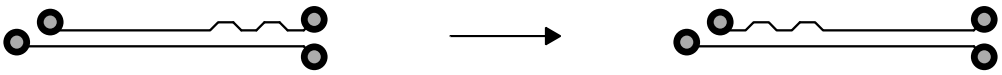
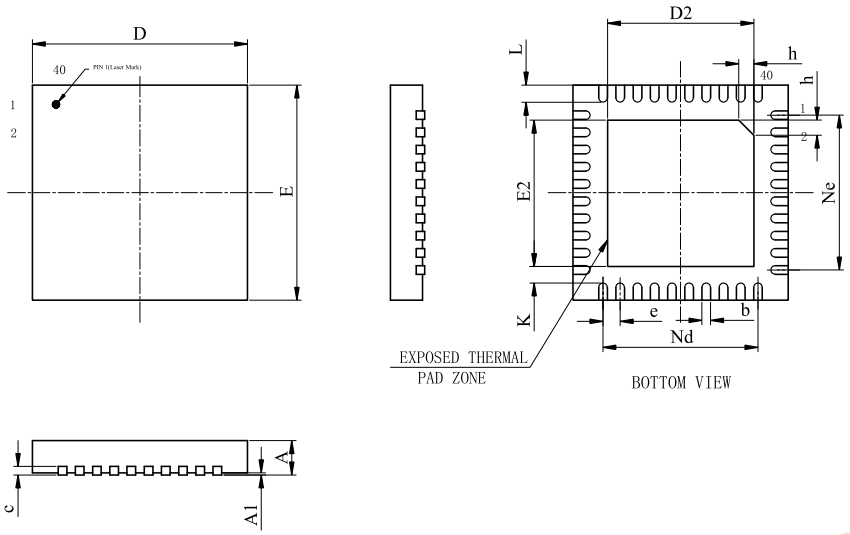


Figure 26. Differential pair

Chapter 8. Mechanical, Packaging

8.1. Packaging Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.20	3.50	3.80
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.20	3.50	3.80
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F (mil)	150*150		

Figure 27. JL2121(D), QFN 40 5mm x 5mm

Chapter 9. Order Information and Support

Table 23. Ordering Guide

Model	Temperature Range	Package Description
JL2121-N040C	0 ~ 70°C	40-Pin QFN (RoHS 2.0 Compliant)
JL2121D-N040C	0 ~ 70°C	40-Pin QFN (RoHS 2.0 Compliant)
JL2121-N040I	-40°C ~ 85°C	40-Pin QFN (RoHS 2.0 Compliant)
JL2121D-N040I	-40°C ~ 85°C	40-Pin QFN (RoHS 2.0 Compliant)

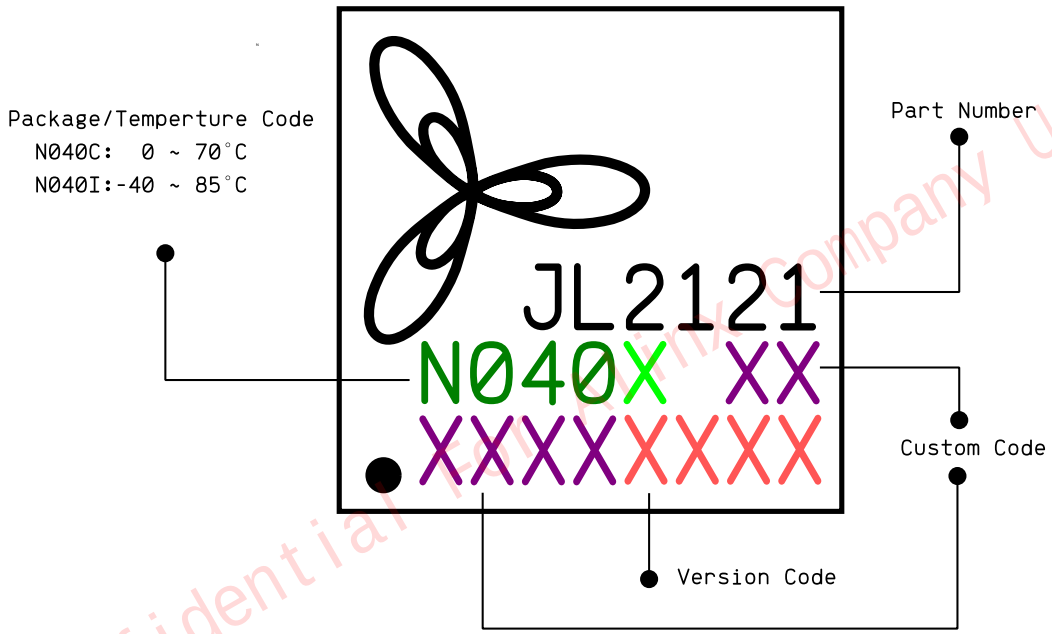


Figure 28. Part Description