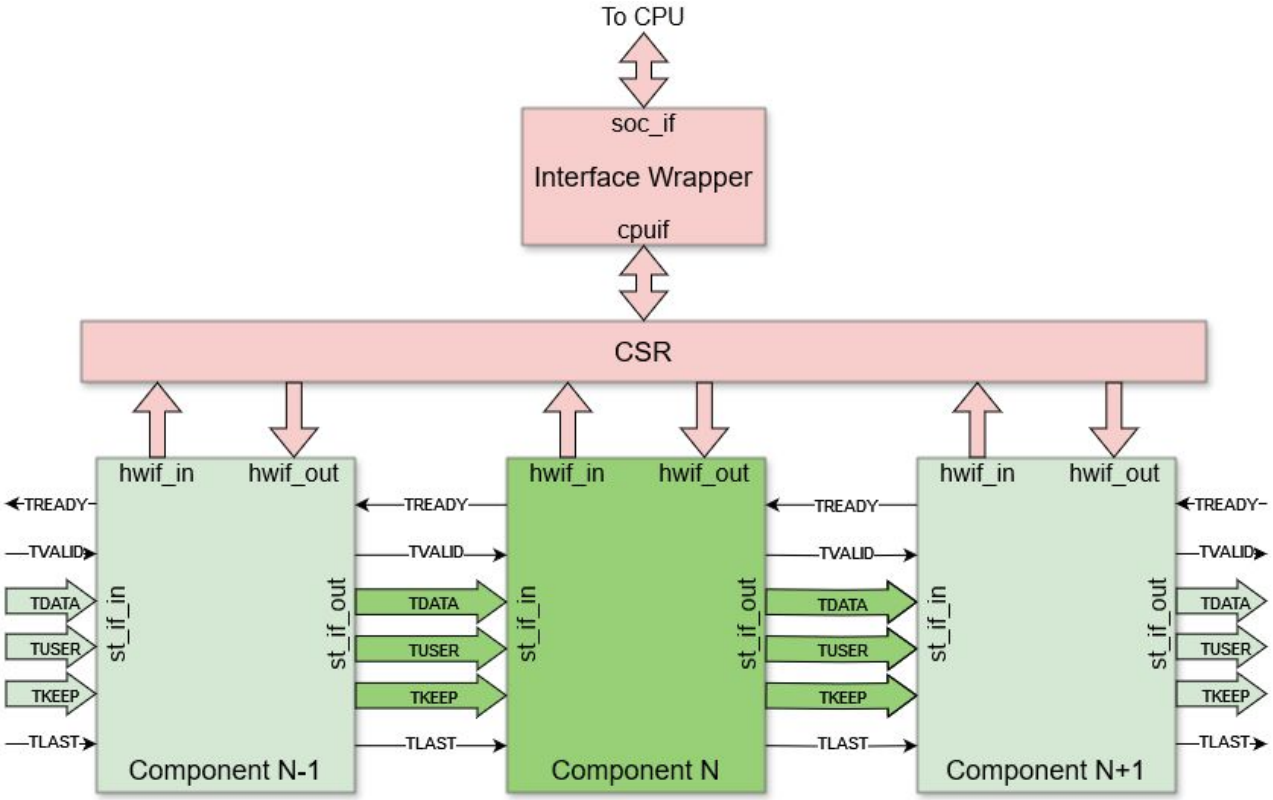
Data Plane Engine Interconnect & Atomic CSR Updates Meeting

11/19/2024

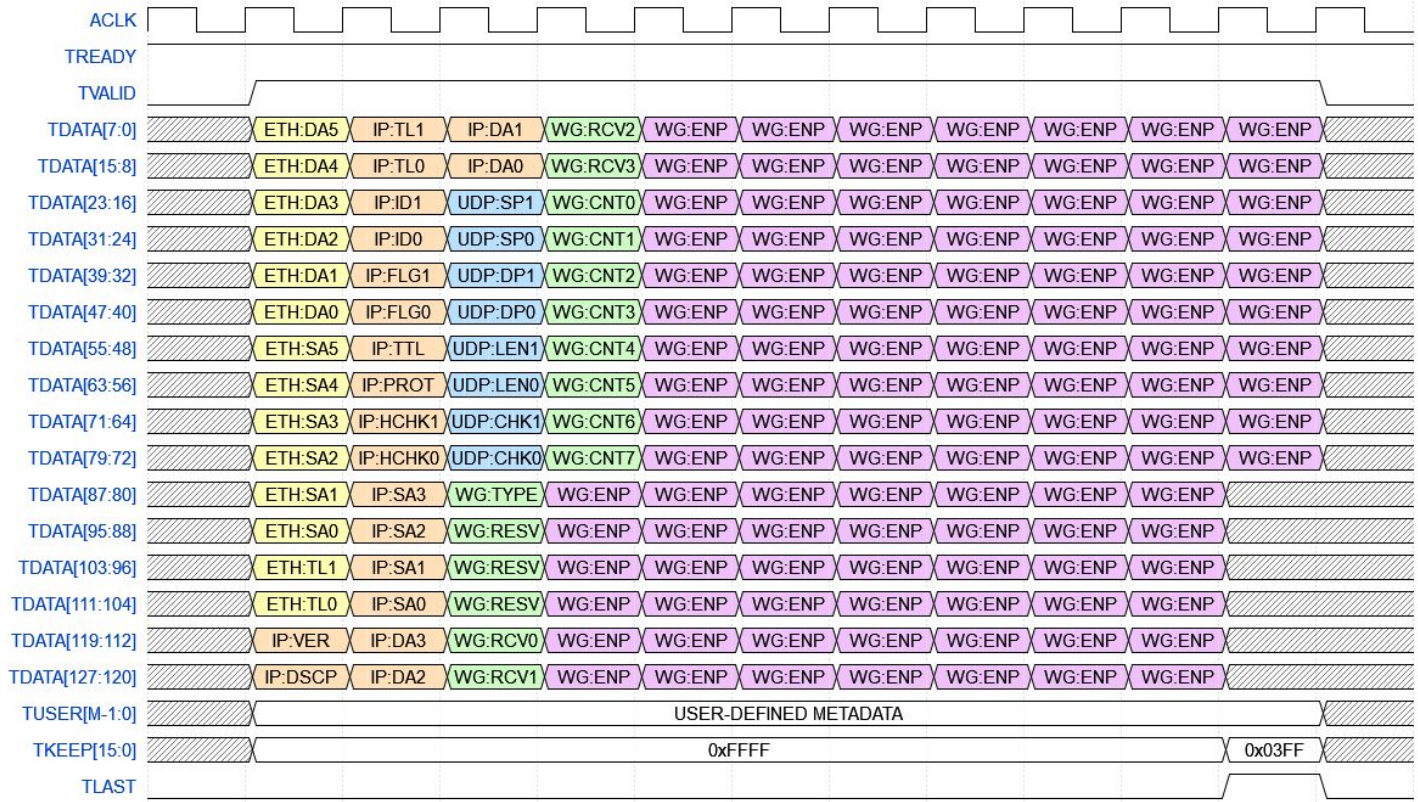
Outline

- Data Plane Engine Interconnect
  - DPE AXI4-Stream Interface
  - DPE Flow Control
- Atomic CSR Updates
  - CSR Flow Control
  - CSR Update Latency

Data Plane Engine Interconnect

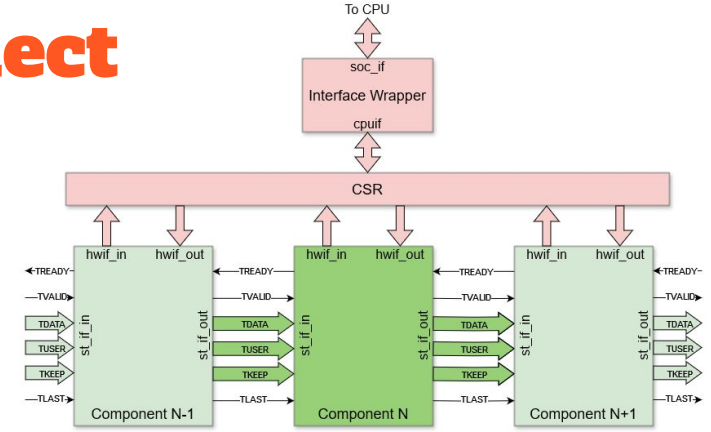


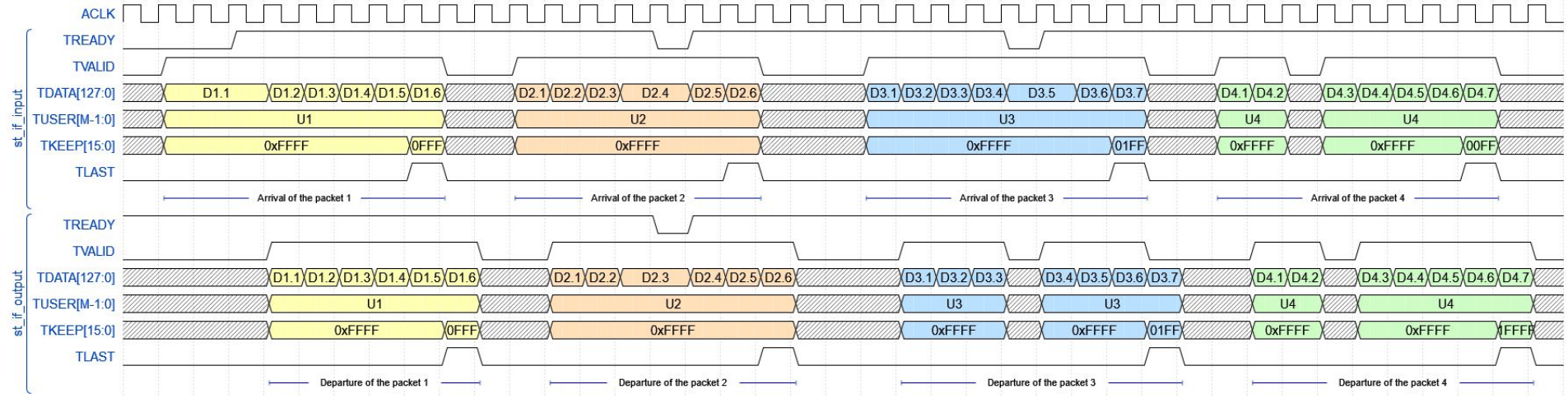
Data Plane Engine Interconnect



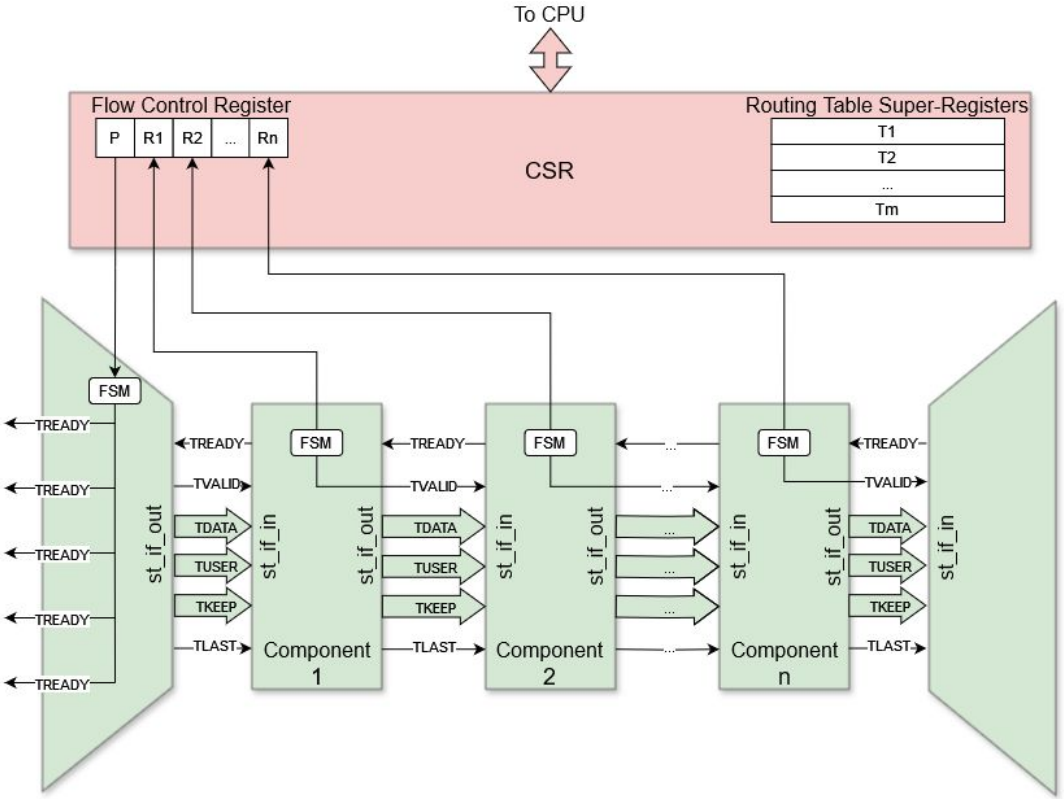
Data Plane Engine Interconnect

- Forward Flow Control (TVALID)
- Backward Flow Control (TREADY)





Atomic CSR Updates



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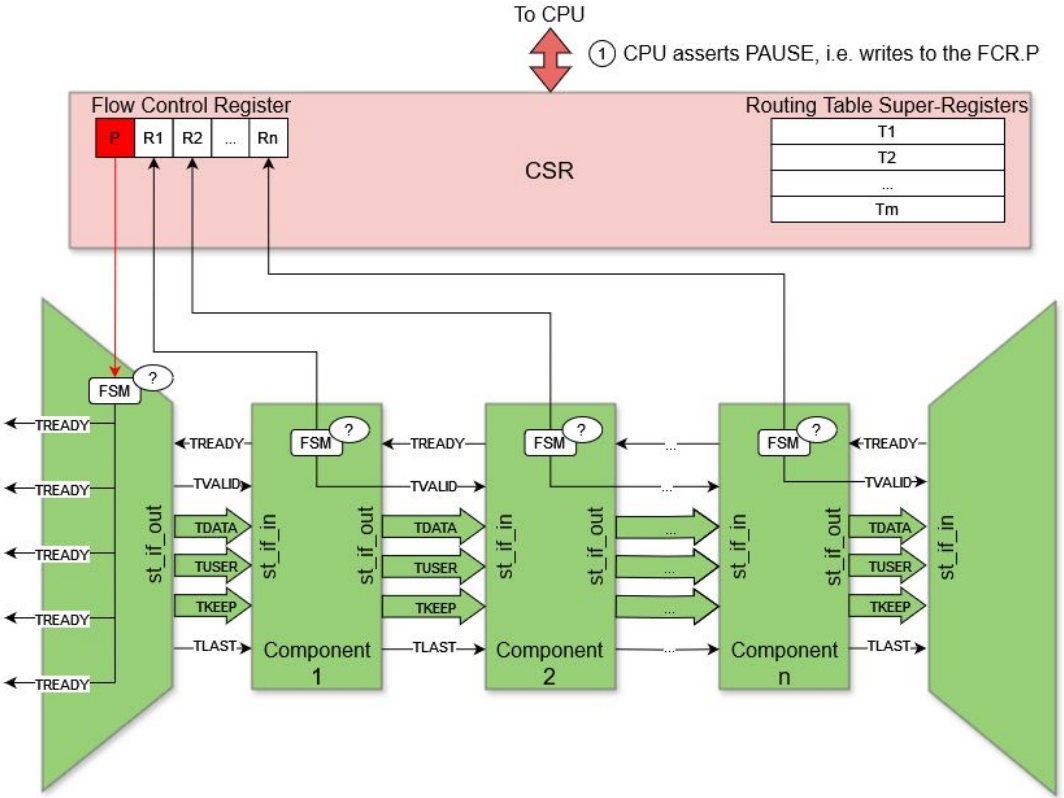

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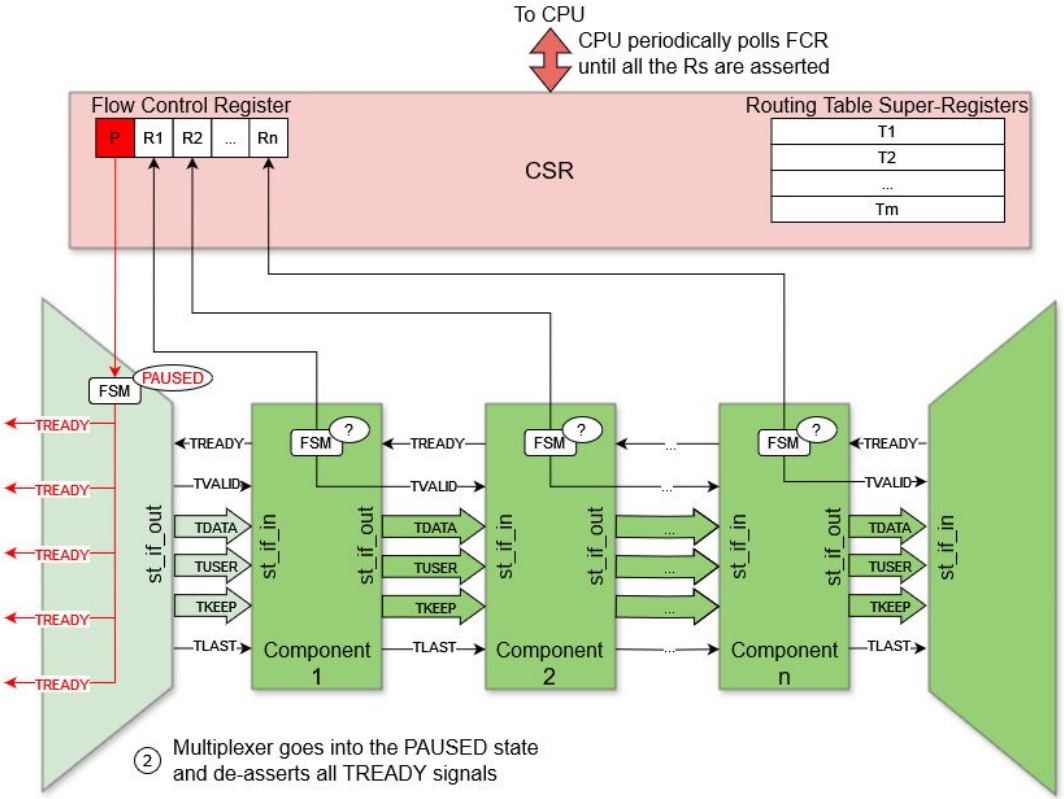

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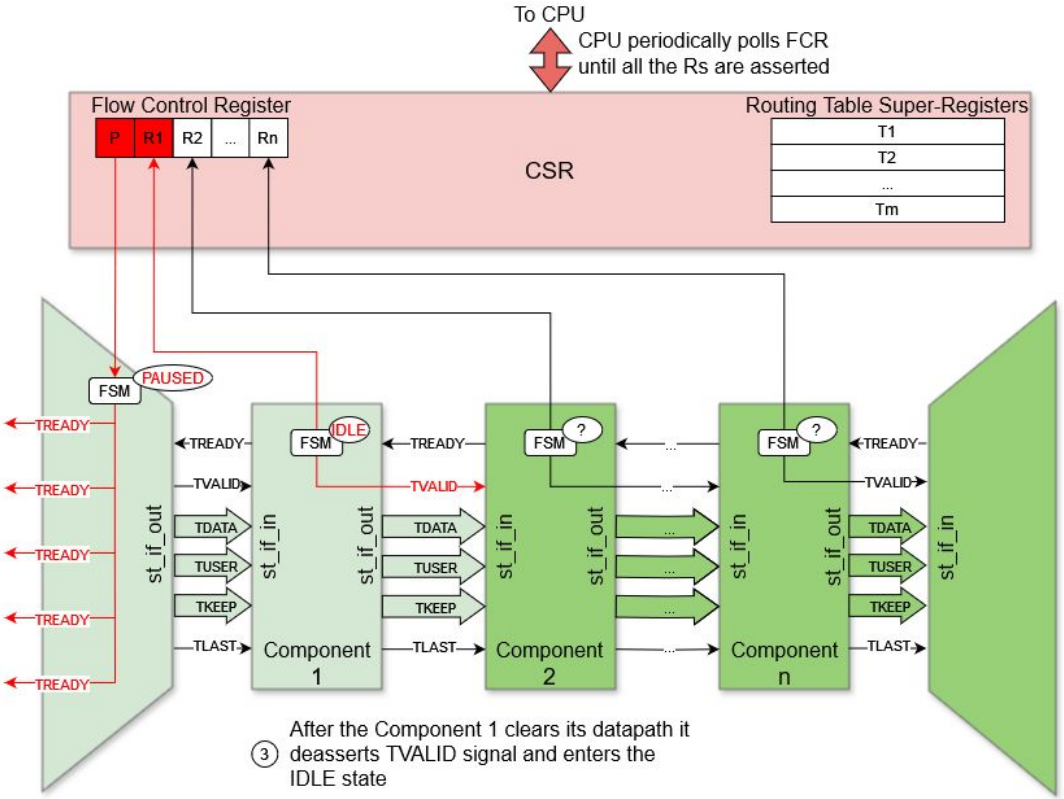

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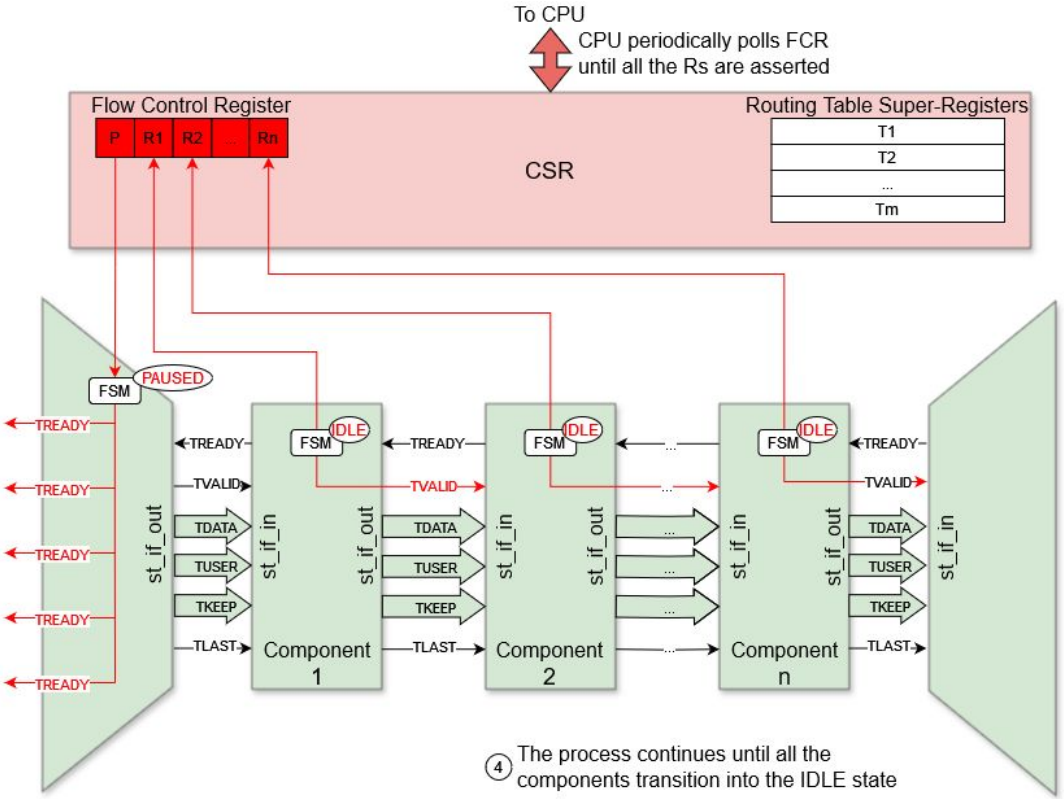

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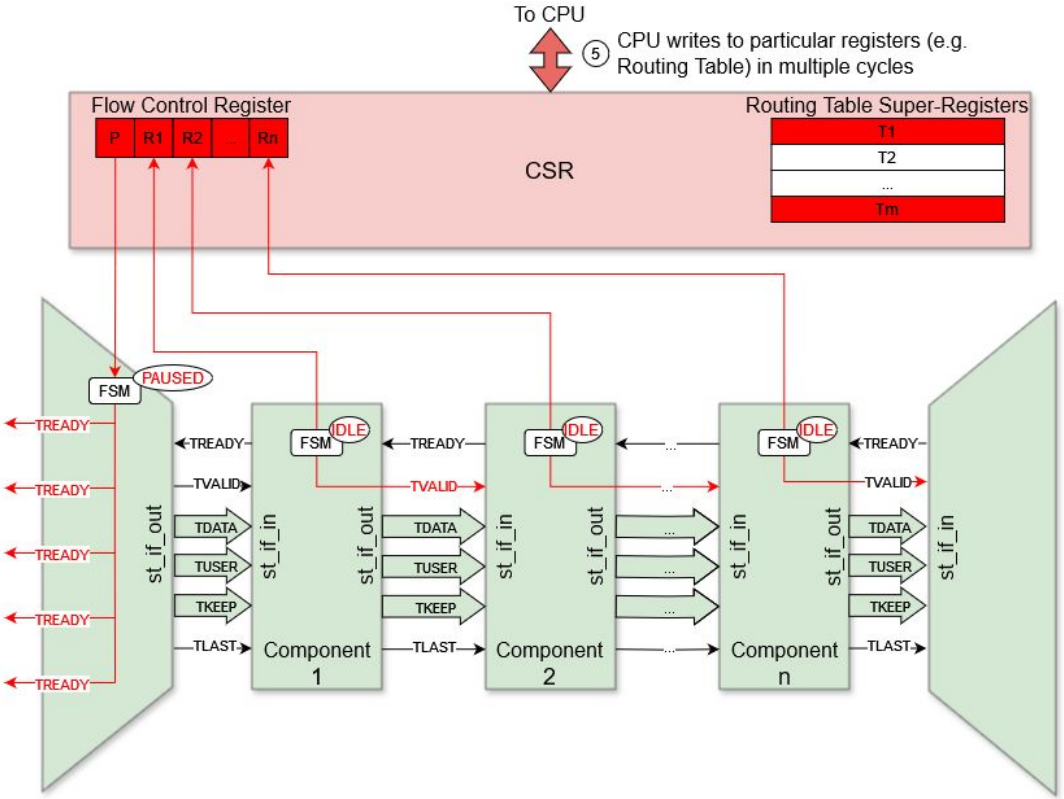

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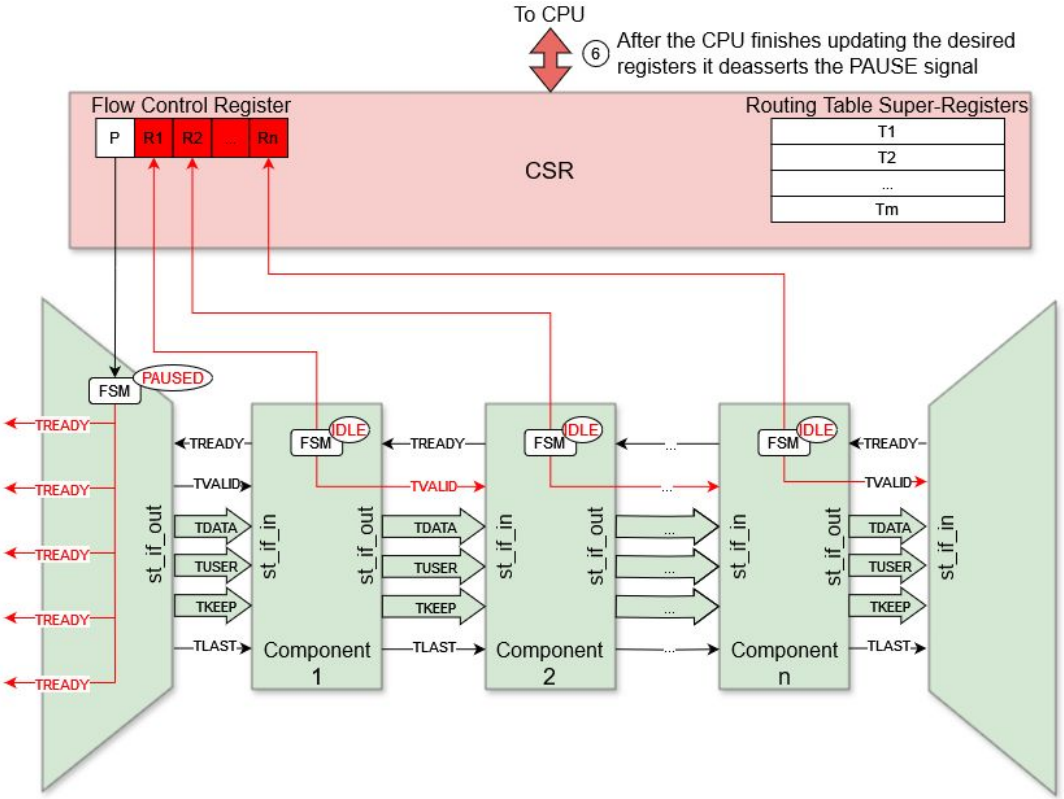

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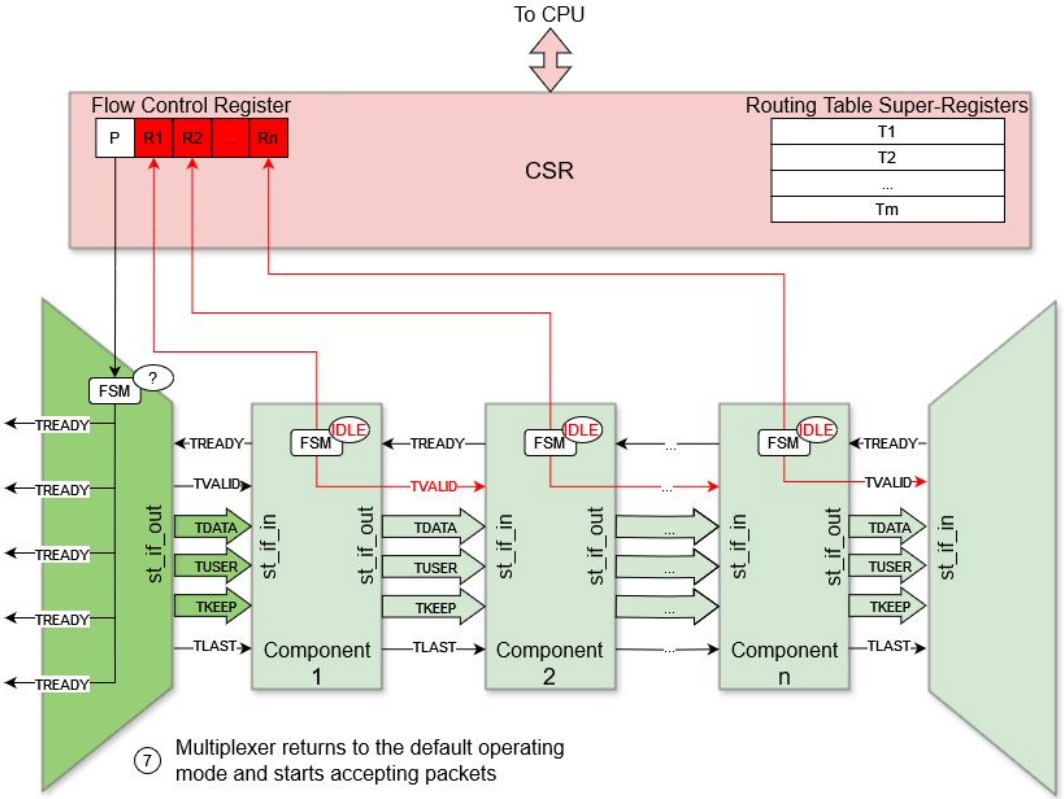

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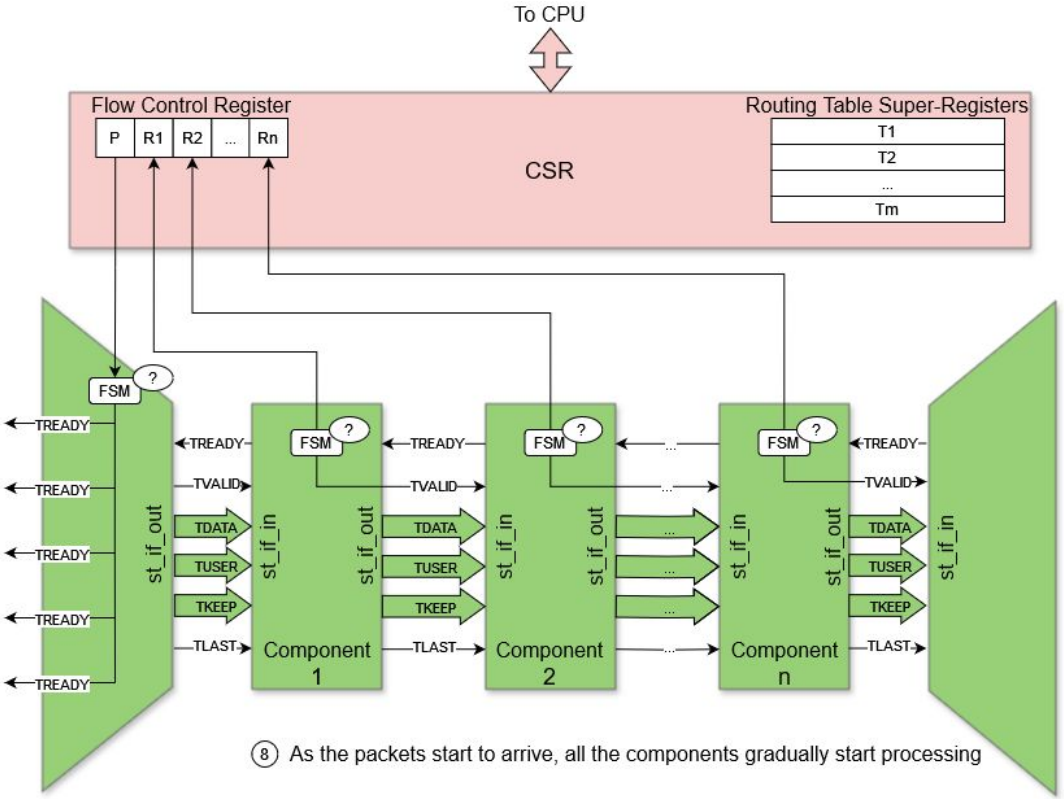

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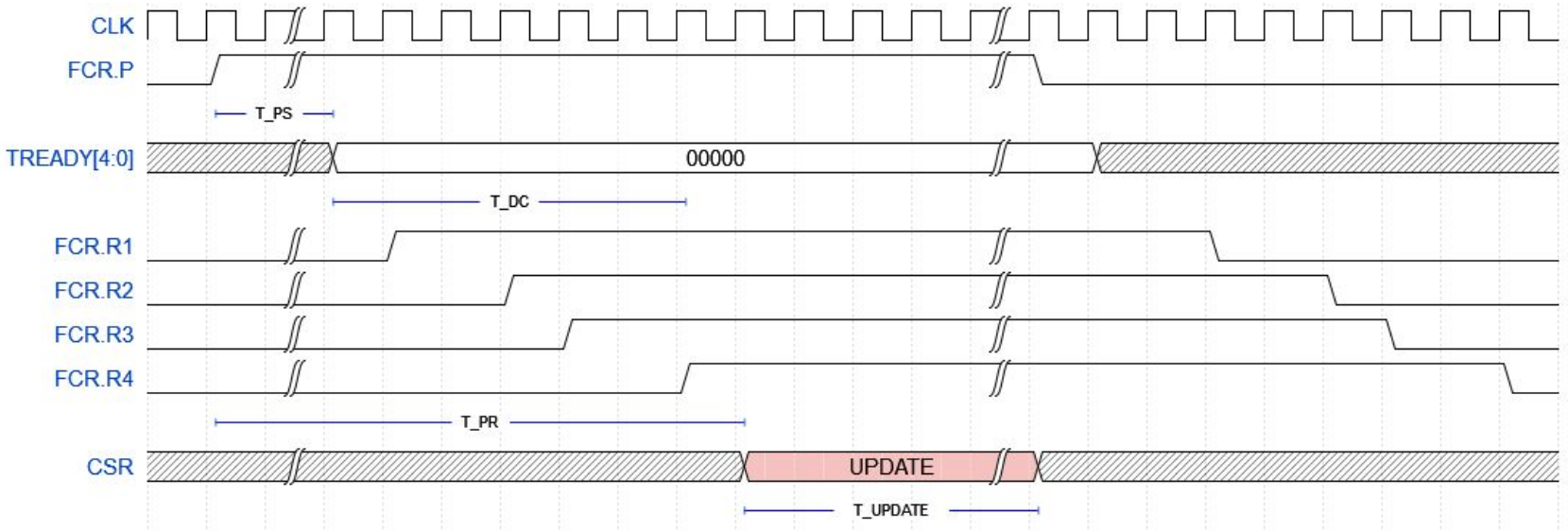

Atomic CSR Updates

If we assume that the DPE just started processing a 1500B frame, PAUSE setup latency at multiplexer can be expressed as:

- T_PS = T_CLK + (1500/16)*T_CLK = 95*T_CLK

Furthermore, PAUSE to READY latency can be expressed as:

- T_PR = T_PS + T_DC + T_CLK

where T_DC is a data path clearing latency.

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For the cut-through pipeline:

- T_DC1 (Header Parser) = 4*T_CLK
- T_DC2 (WireGuard Assembler/Disassembler) = 4*T_CLK
- T_DC3 (WireGuard Encryptor/Decryptor) = 4*T_CLK
- T_DC4 (IP Lookup Engine) = 2*T_CLK

- T_DC = T_DC1 + T_DC2 + T_DC3 + T_DC4 = 14*T_CLK

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For the store-and-forward DPE (worst-case scenario):

- T_DC1 (Header Parser) = (1500/16)*T_CLK = 95*T_CLK
- T_DC2 (WireGuard Assembler/Disassembler) = (1500/16)*T_CLK = 95*T_CLK
- T_DC3 (WireGuard Encryptor/Decryptor) = (1500/16)*T_CLK = 95*T_CLK
- T_DC4 (IP Lookup Engine) = (1500/16)*T_CLK = 95*T_CLK

- T_DC = T_DC1 + T_DC2 + T_DC3 + T_DC4 = 380*T_CLK

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Hence, PAUSE to READY latency can be calculated as follows:

- T_PR = 95*T_CLK + 14*T_CLK + T_CLK = 110*T_CLK (or 476*T_CLK for S&F DPE)

Update latency per byte of written CSR data if 32-bit bus is used:

- T_CSR = (1/4) * T_CLK

Given that the Routing Table contains 16 entries of 300 bytes each, the update latency can be calculated as follows:

- T_UPDATE = 16*300*T_CSR = 1200*T_CLK

Atomic CSR Updates

Finally, total CSR update latency can be calculated as follows:

- T = T_PR + T_UPDATE = 1310*T_CLK = approx. 16us (or 21us for S&F DPE)

Since no packets are received in the DPE during the FCR handshake procedure, from the establishment of the pause until the completion of the CSR update, it is necessary to size the input FIFOs to at least:

- C_FIFO = T * R = 16us * 1Gbps = approx. 2000 bytes (or 2625 bytes for S&F DPE)

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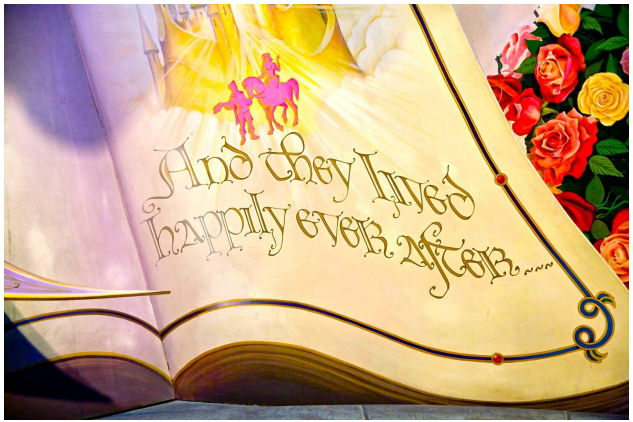
Given that there are four Rx FIFOs connected to 1GbE interfaces, the total required capacity is equal to:

- C_TOTAL = 4*C_FIFO = 8000 bytes (or 10500 bytes for S&F DPE)

As the CSR update latency has the biggest contribution to the total latency, we can conclude that the additional consumption of BRAM (needed for Rx FIFOs) is approximately equal to 2 bytes of memory for each byte of written CSR data.

If we want to support Jumbo frames, then each Rx FIFO must be at least 9000 bytes in size, which gives us a huge margin for CSR update latency (4-5 times more than needed).



Thank you!